Physikalisches Institut, Heidelberg University

The MightyPix HV-CMOS sensor for LHCb Upgrade 2

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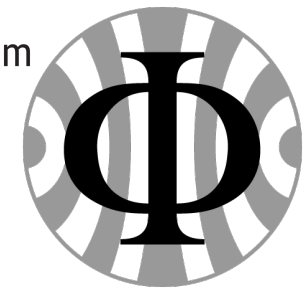
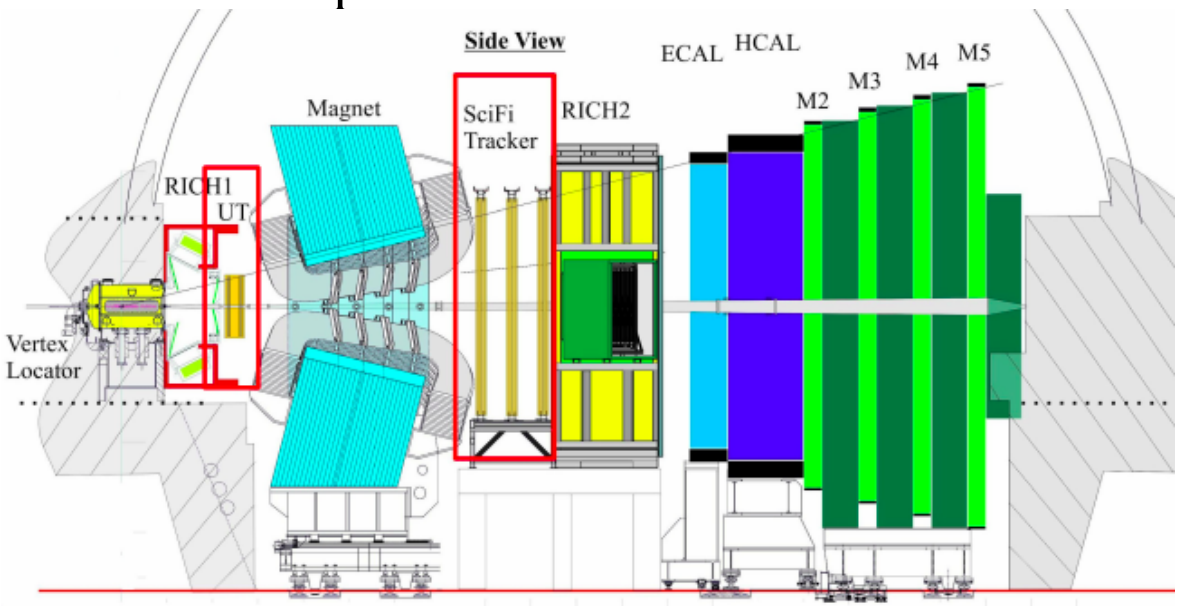


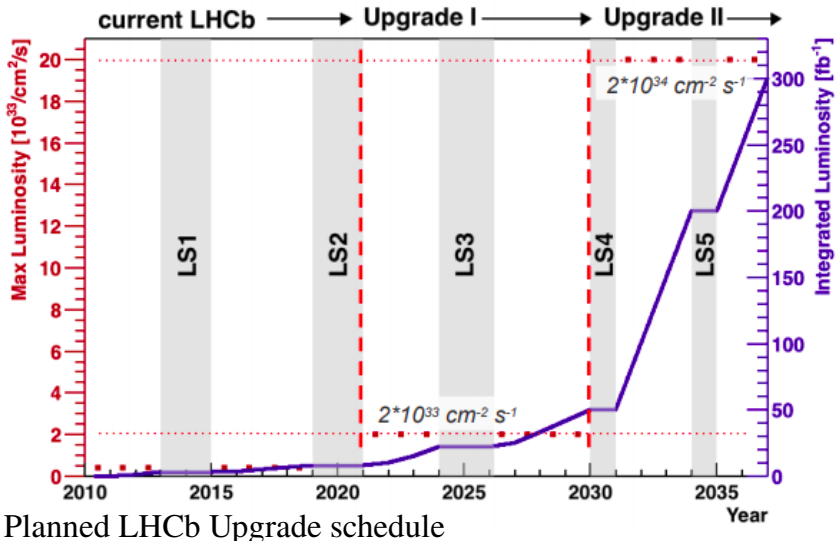
LHCb Detector at the Large Hadron Collider

- Single arm spectrometer
- Designed for precision measurements of the decay of particles containing heavy quarks
- Fully instrumented in the forward region ($2 < \eta < 5$)
- Excellent vertex and momentum resolution
- Very flexible trigger with 40 MHz readout
- Trigger on low momentum particles



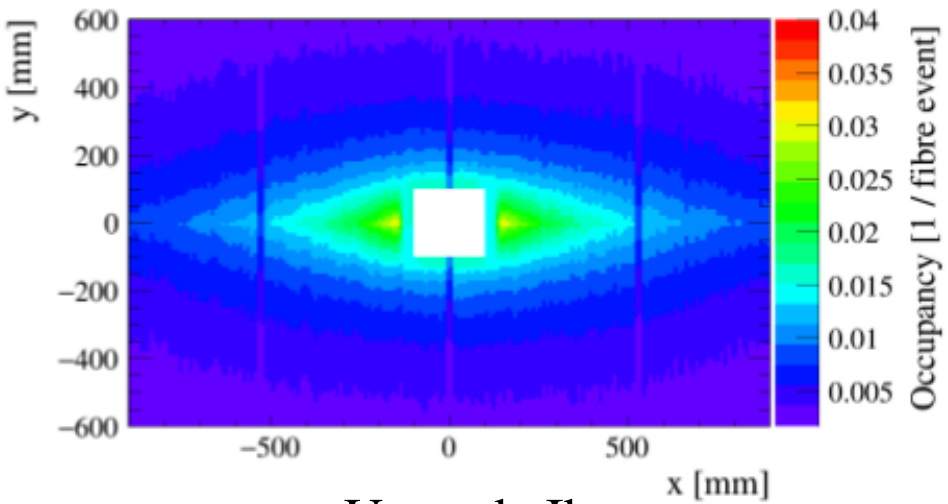
LHCb detector, Upgrade I

SciFi Tracker challenges for Upgrade II

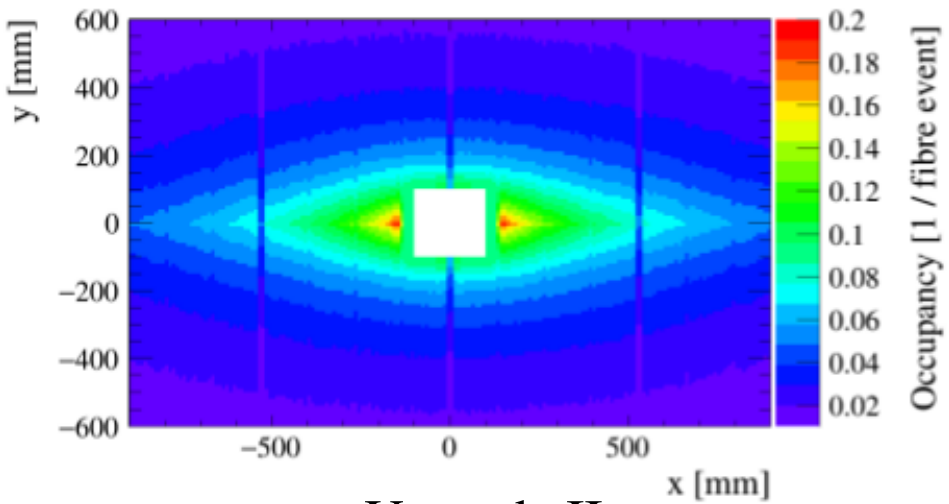


Planned LHCb Upgrade schedule

- $\int \mathscr{L} = 300\ \text{fb}^{-1}$
  → significant fibre radiation damage in inner region
- $\mathscr{L}_{inst} = 2 \times 10^{34}\ \text{cm}^{-2}\text{s}^{-1}$
  → very high occupancy (up to 20 % per fibre per event)



Upgrade Ib

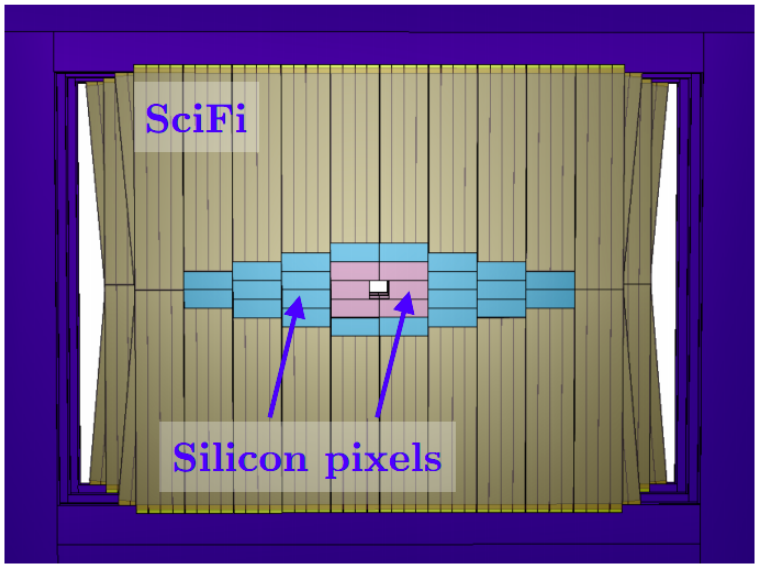


Upgrade II

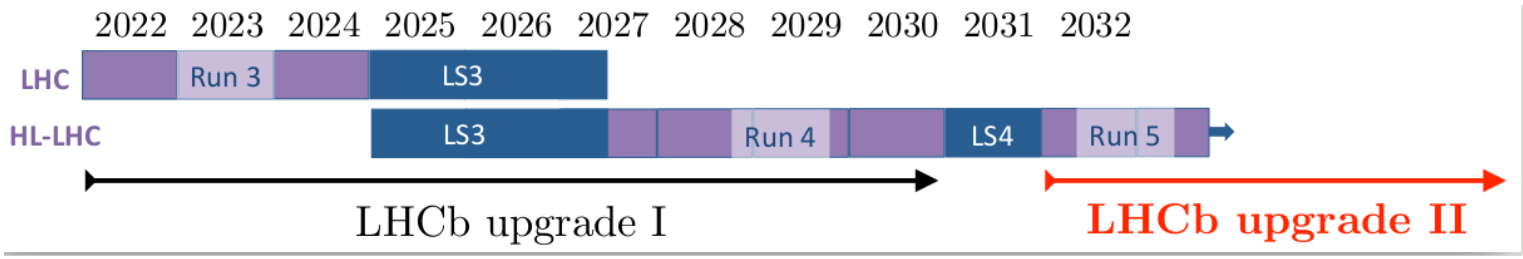
SciFi must be replaced near beam pipe to maintain the same (or better) performance

The Mighty Tracker

- The downstream tracking stations of LHCb Upgrade Ib and II are proposed to be constructed with hybrid technology modules (Mighty Tracker)
- Scintillating fibres in the outer region (good resolution at an affordable cost)
- MightyPix: Silicon in the most central region (granularity and radiation hardness required for the central region)

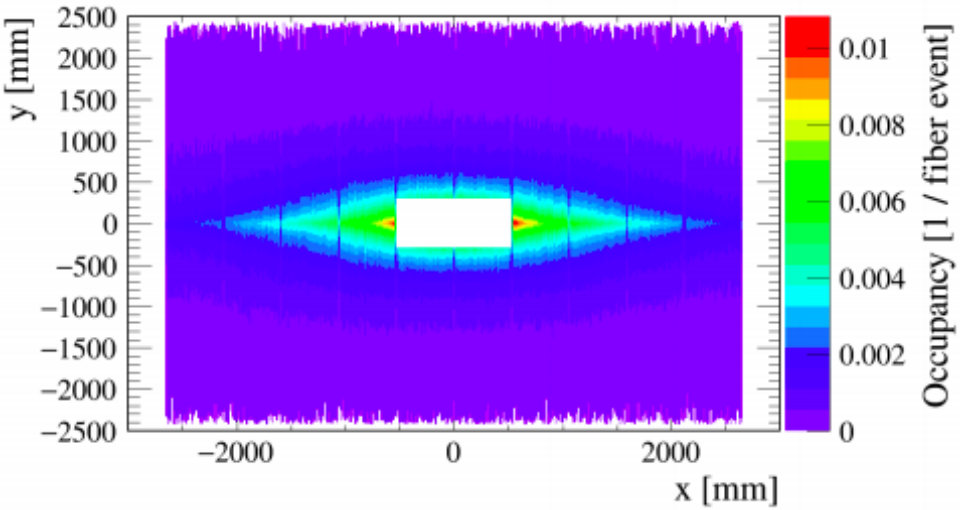


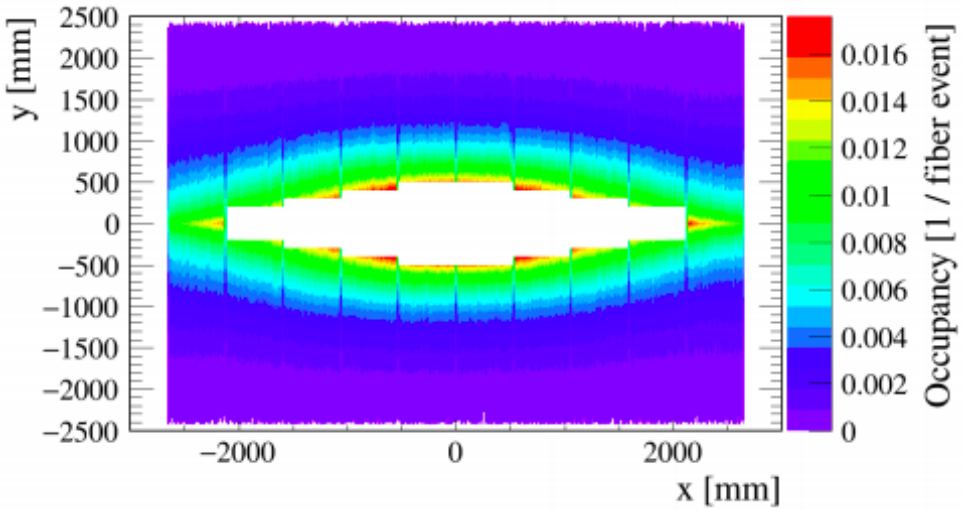
- Inner tracker (IT), consider installation in LS3, planned for operation in Upgrade Ib, with minimal changes to the Sci-Fi
- Middle tracker (MT), consider installation in LS4, planned for operation in Upgrade II

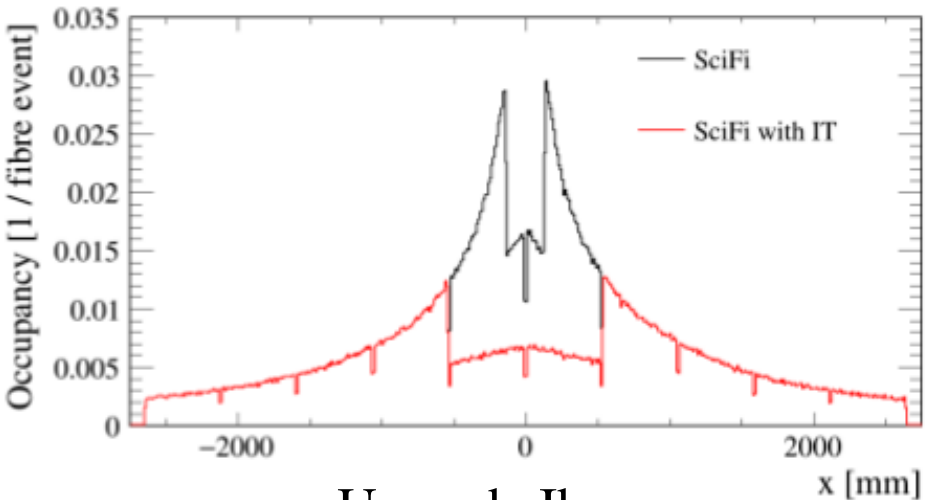


SciFi Tracker Upgrade Ib and II

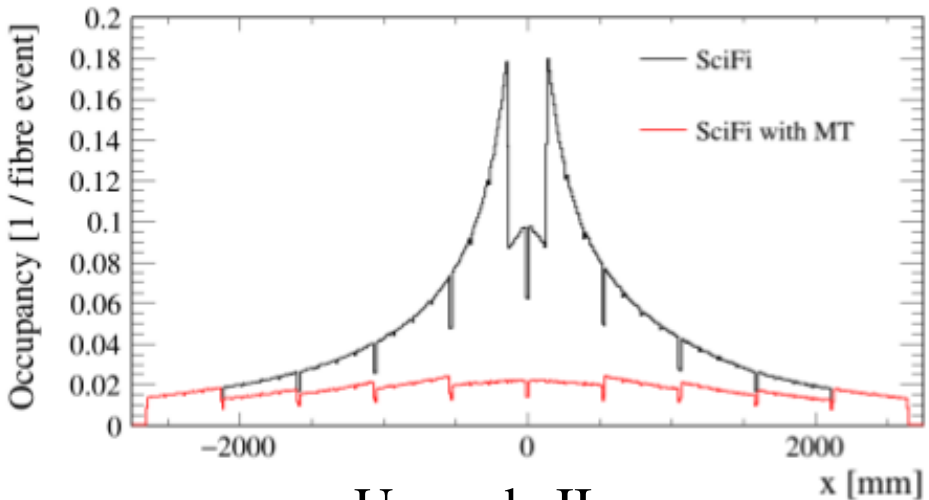
- Integrated occupancy for Upgrade Ib with the addition of the IT region (left) and Upgrade II with the addition of the MT region (right)







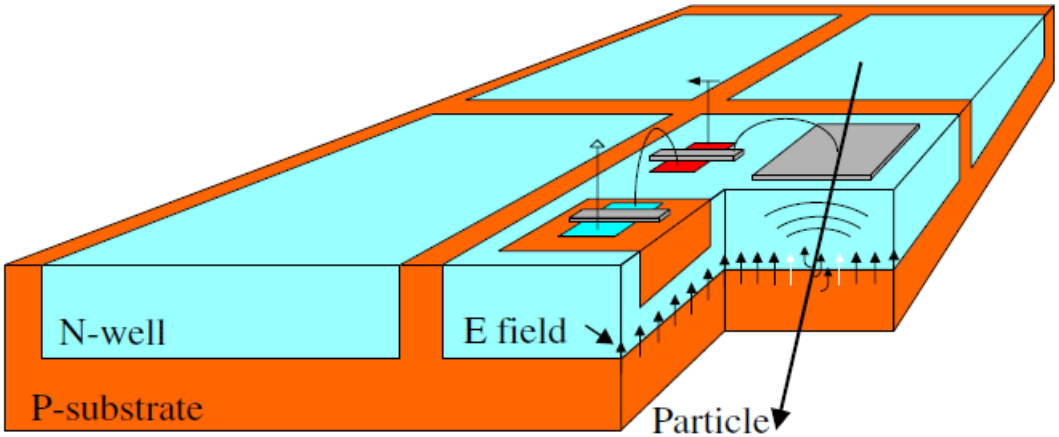
Upgrade Ib



Upgrade II

High Voltage Monolithic Active Pixel Sensor

- Integrated readout electronic and sensor (low material budget)
- Implemented in a commercial CMOS process (cheaper than hybrid detectors)
- Depletion area ~ 15 μm at -60V for 20 Ωcm
- Fast charge collection via drift (~ ns)

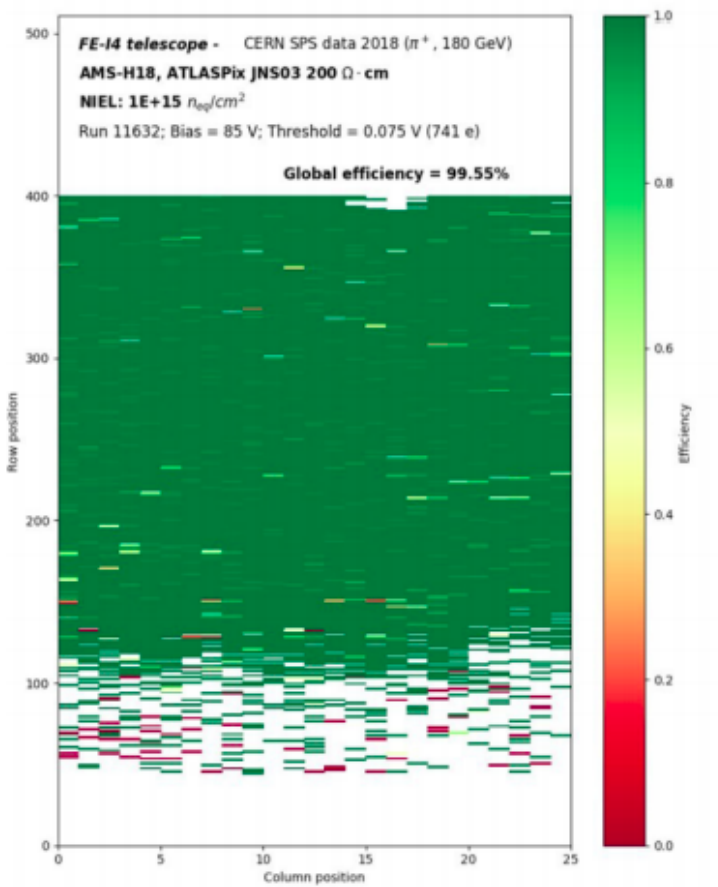


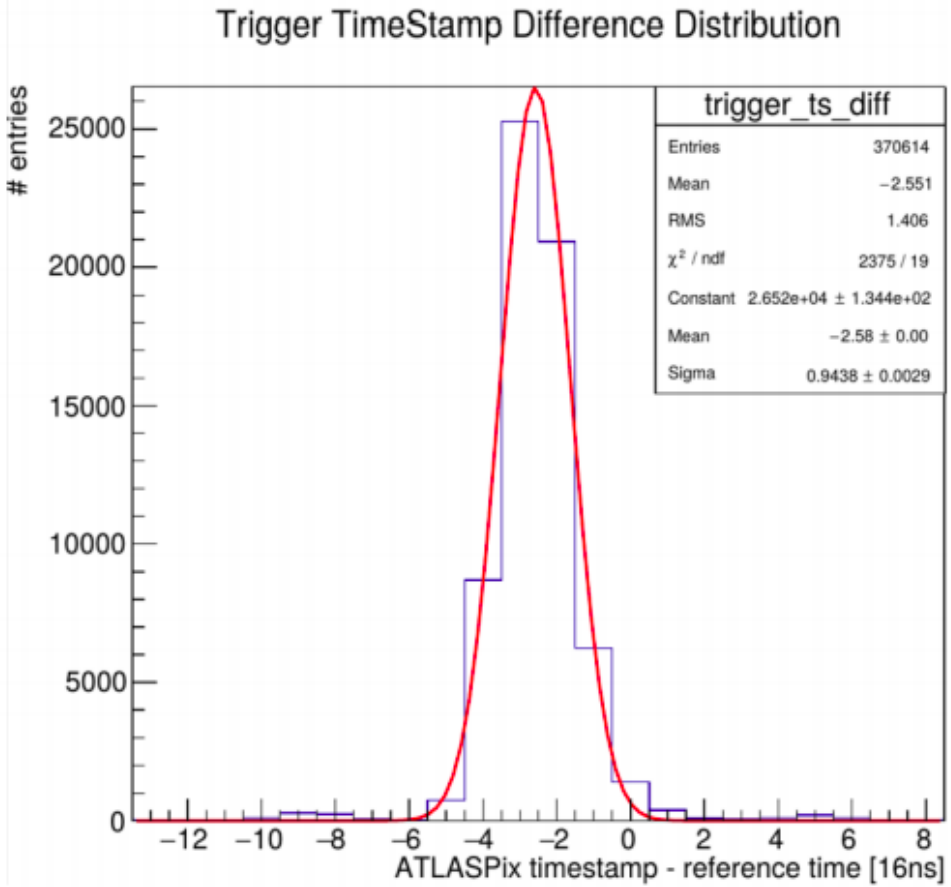
I. Peric A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, NIM A 2007

- Several technologies of HV-MAPS were originally studied:
  - Lfoundries 150nm, suitable but R&D not so advanced
  - TowerJazz improves power consumption but unknown radiation tolerance
  - MuPix and ATLASPix with AMS/TSI 180nm most advanced developments in CMOS sensors that meet the radiation tolerance specifications

MuPix-like sensors

- ATLASPix1 has shown a 99.55% efficiency and time resolution of 15 ns (on-chip correction methods can be used to improve this value) after neutron irradiation to 10^{15} 1 MeV n_{eq}/cm^2





A. Herkert Characterization of a Monolithic Pixel Sensor Prototype in HV-CMOS Technology for the High-Luminosity LHC, Dissertation

MightyPix requirements

Parameter	Specifications
Sensor Thickness (μm)	150
Pixel size (μm^2)	100x300
Time Resolution (ns)	3
Power Consumption (W/cm^2)	0.3
NIEL (1 MeV n_{eq}/cm^2)	2×10^{15}

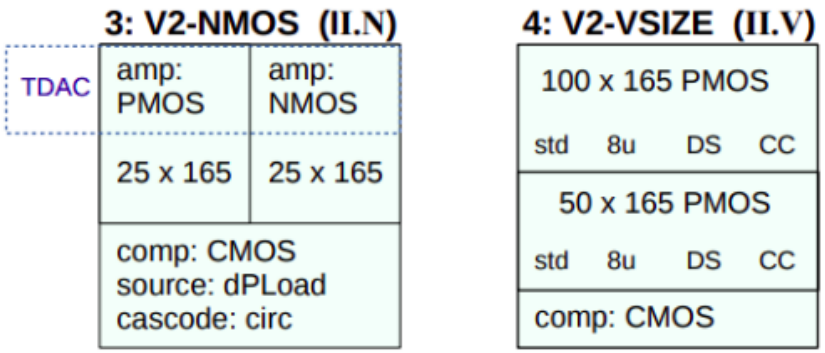
- Pixel size:
  → Size along the bending plane (x) constrained by momentum resolution
  → Size in orthogonal dimension (y) set by multiple scattering and pattern recognition
  → Saves power and readout bits

- Challenges for HV-MAPS:
  - Large pixel size are challenging
  - None of the current MuPix-like sensors meet the specific LHCb readout requirements
  - Time resolution

- Maximum occupancy during Upgrade II for IT < 1% per pixel per event

2020 HV-MAPS engineering run at TSI

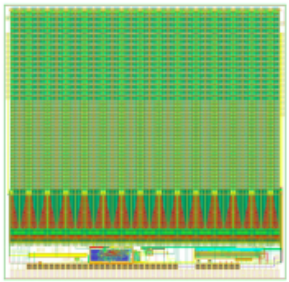
- Prototype sensors for TELEPIX, LHCb, PANDA
- 8 chips (5 chips attractive for LHCb MightyPix Tracker)
- 3 pixel sizes (25x165 μm^2, 50x165 μm^2, 100x165 μm^2)



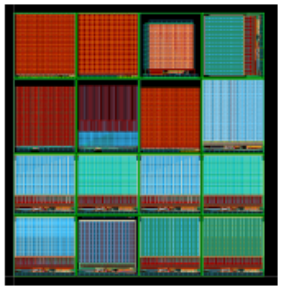
- 2 amplifier types according to input transisitor (NMOS and PMOS)
- 4 variants of the PMOS amplifier
  - 4 m input transistor, single source, linear cascode
  - 8 m input transistor, single source, linear cascode
  - 4 m input transistor, double source, linear cascode
  - 4 m input transistor, single source, circular cascode
- 3 pixel comparator types (NMOS, CMOS and distributed type)

Timeline

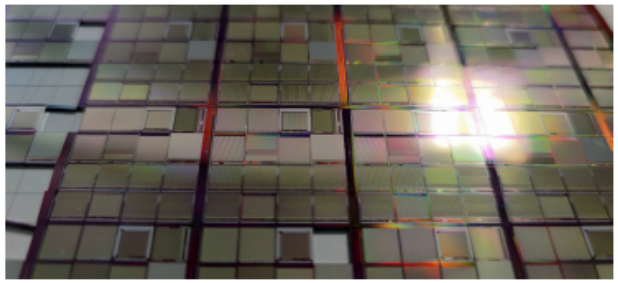
May/2020
submitted to TSI



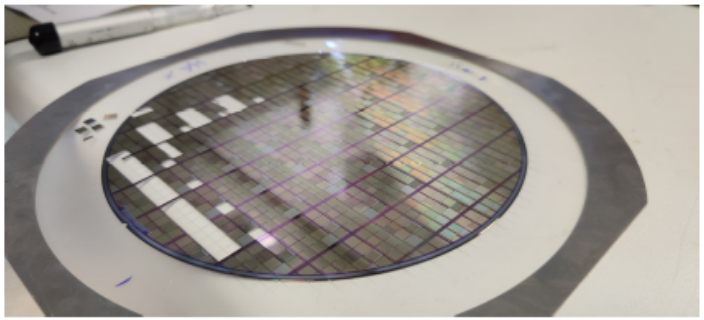
7 September/2020
arrived from TSI



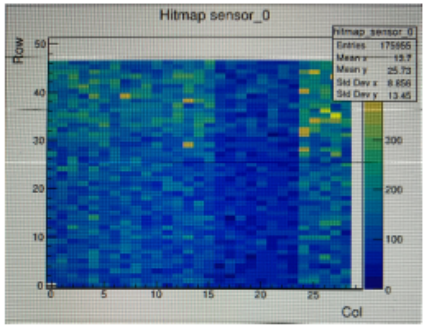
14 September
arrived after Dicing at KIT



15-18 September
picking and first lab test (insert, motherboard, firmware)



21 September-10 October
Order of new insert, population, picking new sensors, glue and bonded. Lab optimization and software implementation

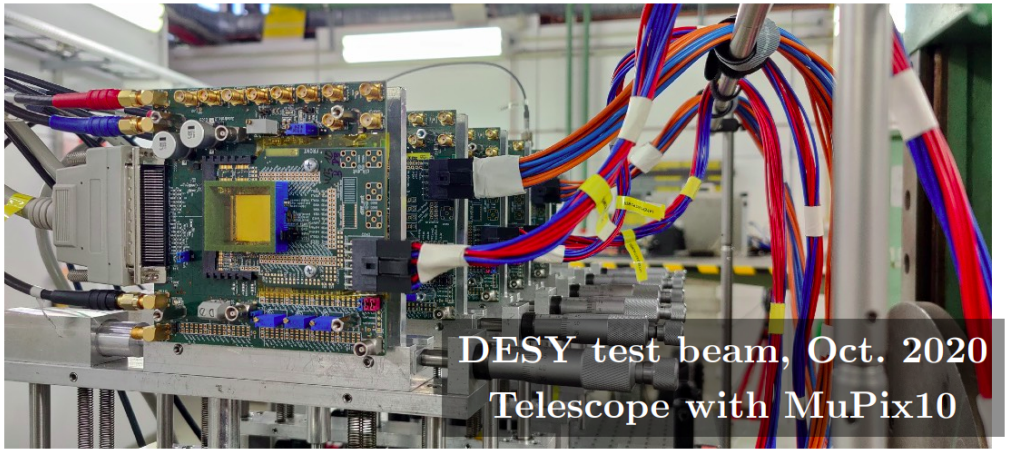


First tests in beam at DESY area 21 (19-25 October 2020)

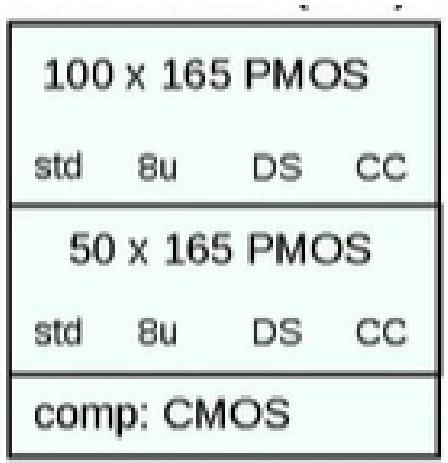
DESY Testbeam

- MuPix10 Telescope
  - 3 reference layers
  - pixel size: 80×80 μm^2
  - active area: 20.48×20.0 mm^2

*More in The Very Large HV-MAPS Tracking Telescope talk by David Immig

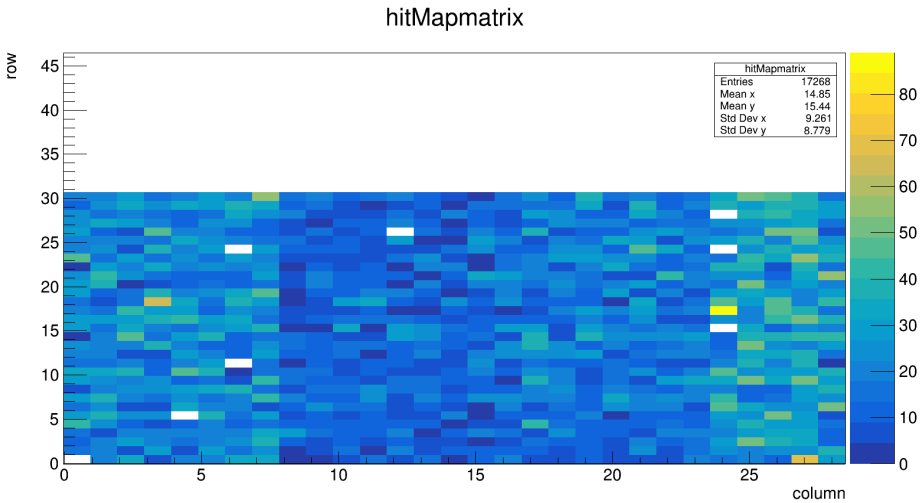


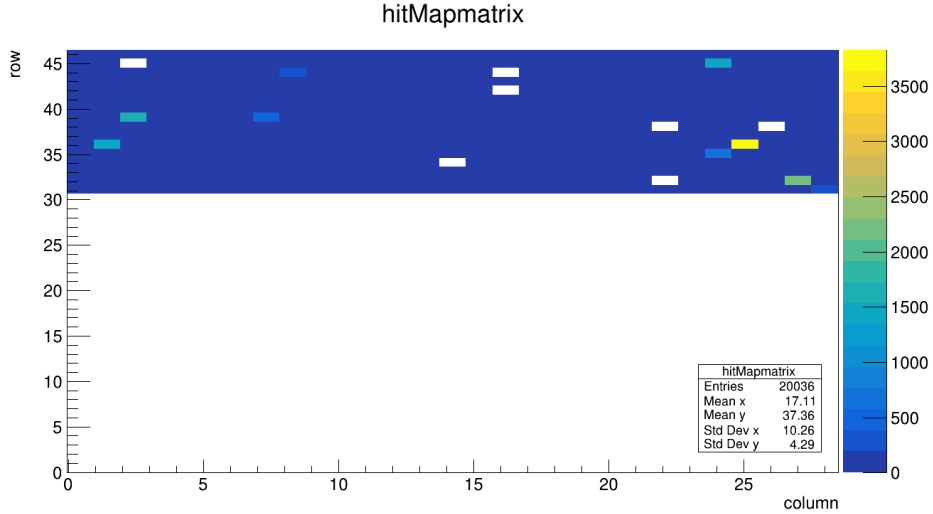
- DUT:
  - V2-VSIZE
  - 4 PMOS amplifier
  - CMOS comparator
  - 2 pixel sizes 100×165 μm^2 and 50×165 μm^2
  - Breakdown Voltage -118 V
  - Resistivity 200 Ωcm
  - Threshold scan (from 90 to 180 mV)



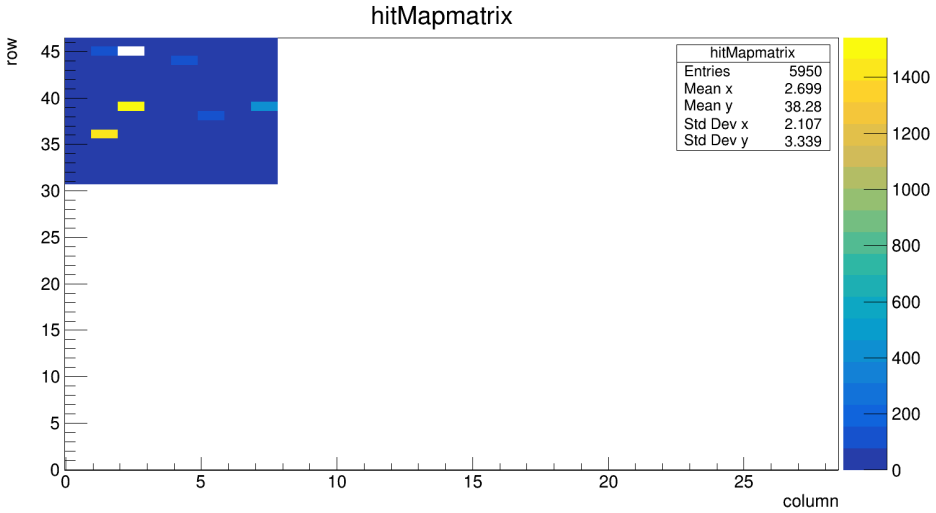
Data Analysis

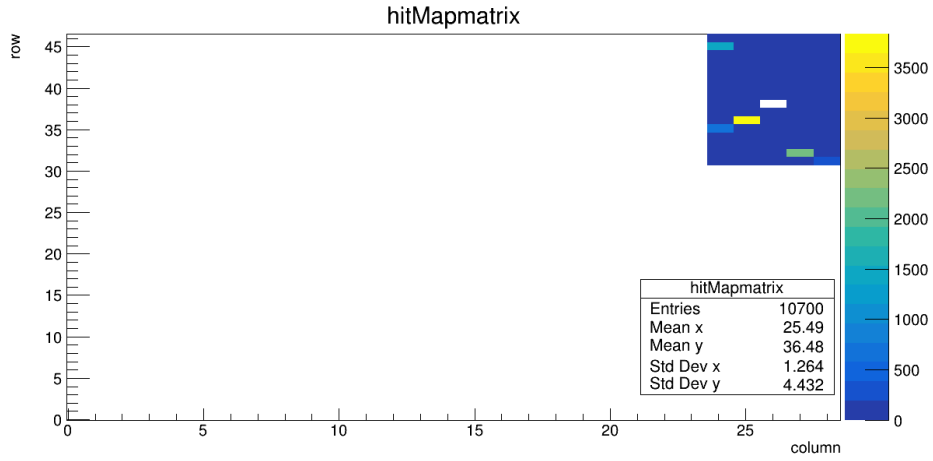
- The results presented in the following have been analysed with Corryvreckan:
  - A geometry file for each pixel size matrix





  - Analysis of the different matrices through definition of ROI

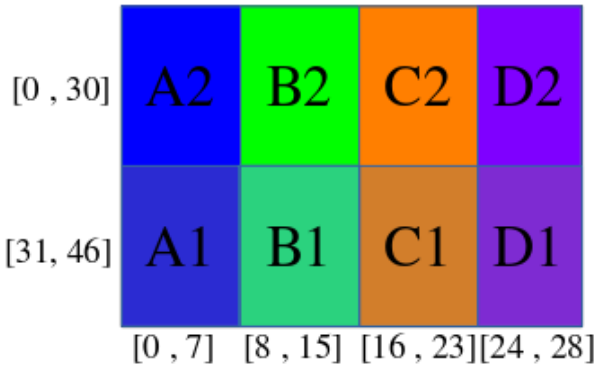




DUT Efficiency preliminary results

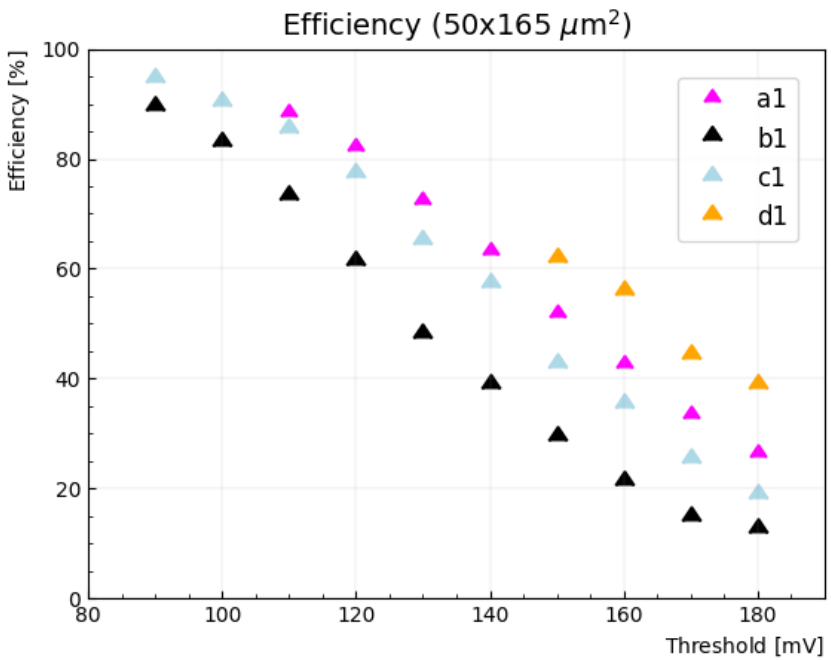
4: V2-VSIZE (II.V)

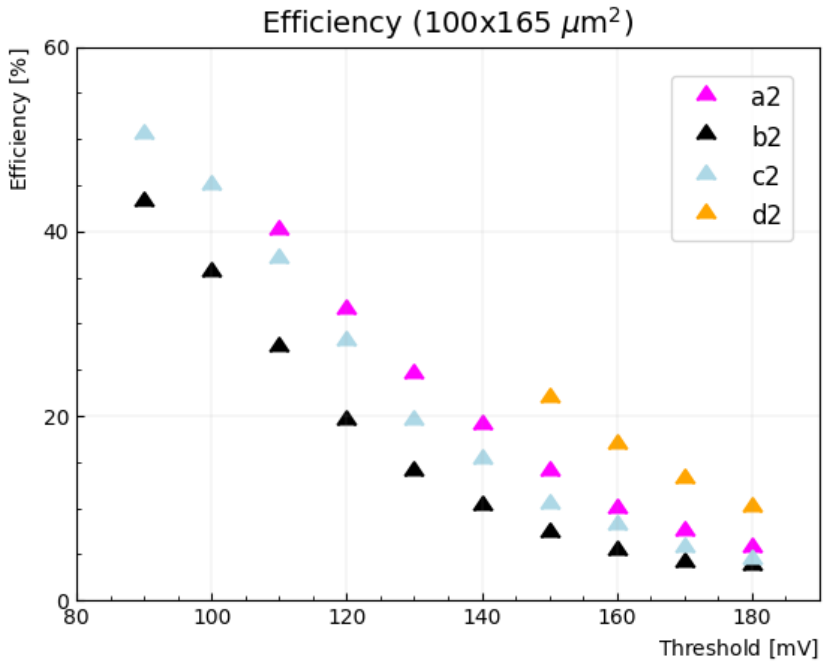
100 x 165 PMOS std 8u DS CC
50 x 165 PMOS std 8u DS CC
comp: CMOS



1. 50 x 165 µm - row: [0 ,30]
2. 100 x 165 µm - row: [31,46]

A) Single source - linear cascode - 4 µm input transistor
B) Single source - linear cascode - 8 µm input transistor
C) Double source - linear cascode - 4 µm input transistor
D) Single source - circular cascode - 4 µm input transistor





Noise and Uncorrelated hits

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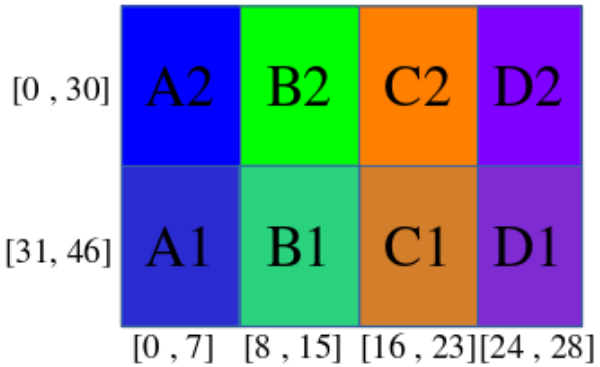

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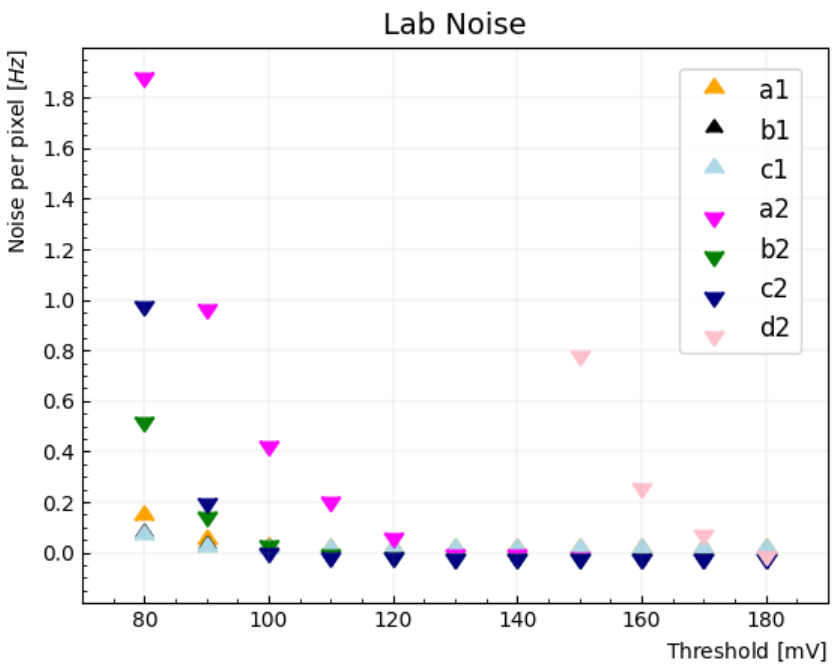
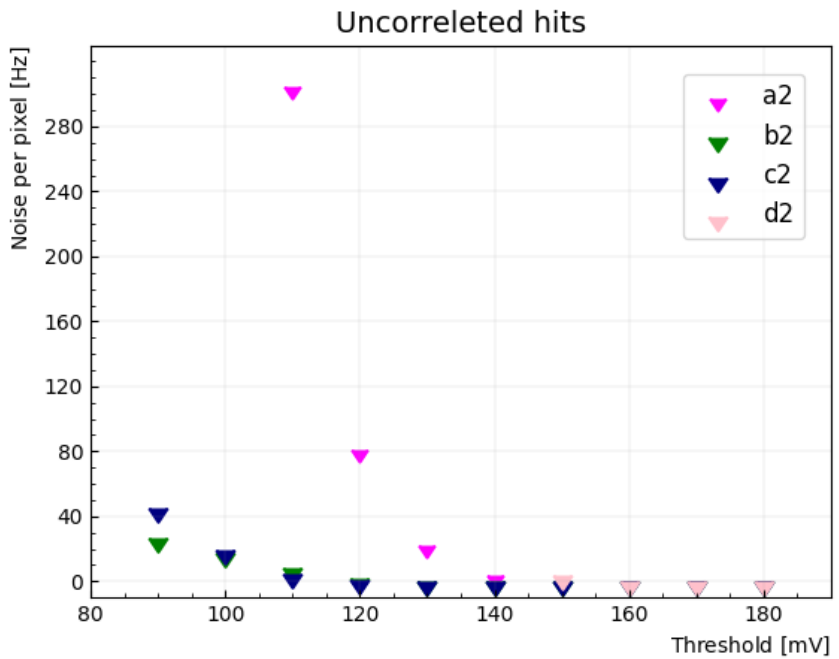
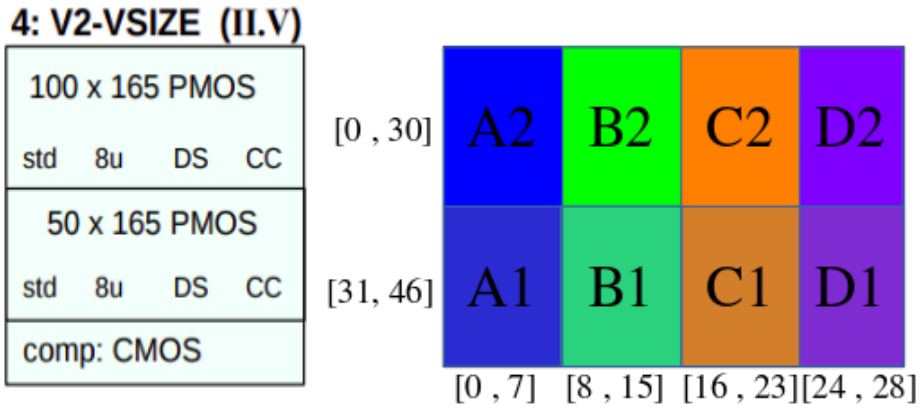




Further optimization of the sensor operation parameters

Uncorrelated hits



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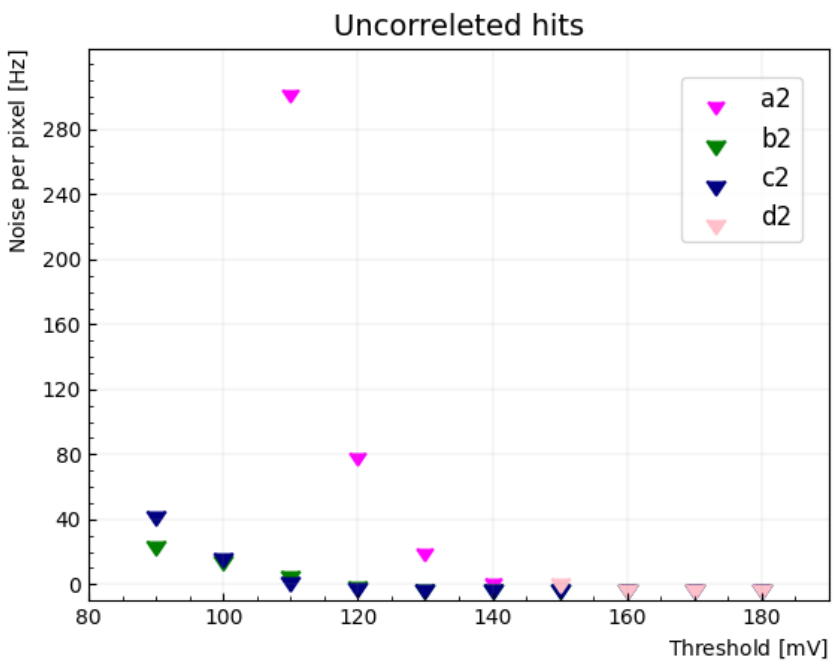

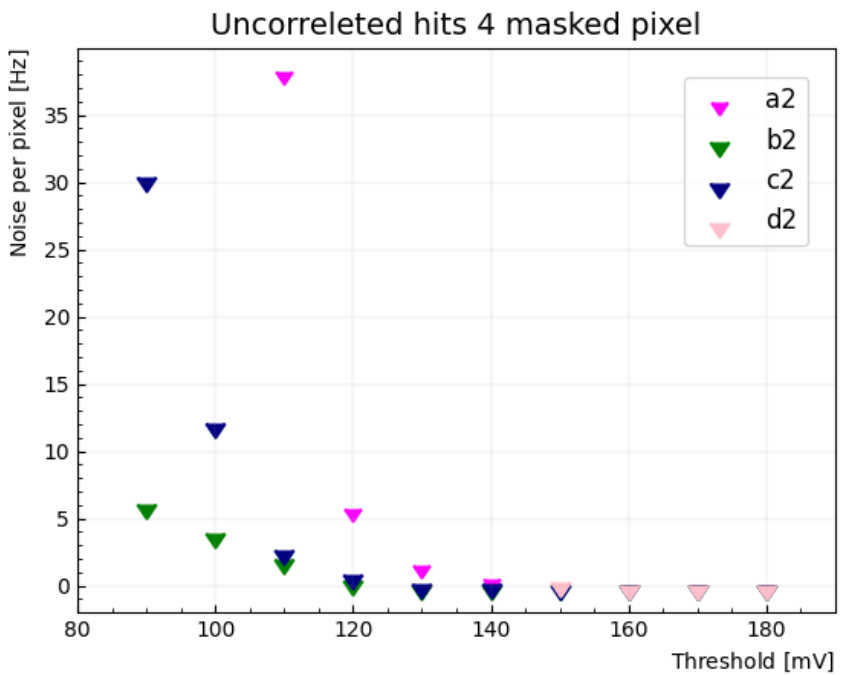

Individual pixel masking may allow to study lower thresholds

Summary and Outlook

- Tracking at LHCb in HL-LHC will be possible by using a combination of SciFi and HV-CMOS technologies
  → maintaining excellent performance in high-occupancy regions
- R&D at early stages
- Pixel size to be decided
  → baseline size 100 μm x 300 μm from physics requirements
  → considering smaller pixels (with logical sum included in readout) for lower noise and better time resolution
- October 2020 DESY testbeam data analysis in progress
- Testbeam at DESY in 2021
- Lab optimization in progress
- New submission in May/2021 compatible with LHCb readout and final pixel size
- Irradiated MuPix10 chips up to 9×10^{15} n_{eq}/cm^2 ; systematic studies soon