The AIDA Trigger/Timing Logic Unit:

Current status.
Future Plans.

David Cussans, BTTB9, 8/Feb/21

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.

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Outline

- Triggering and Timing at Beam Tests
  - Why?
  - How?
- The AIDA(2020) Trigger/Timing Logic Unit (TLU)
  - History
  - Features
  - Documentation
- Plans for AIDA-Innova TLU
  - New/Changed/Improved features

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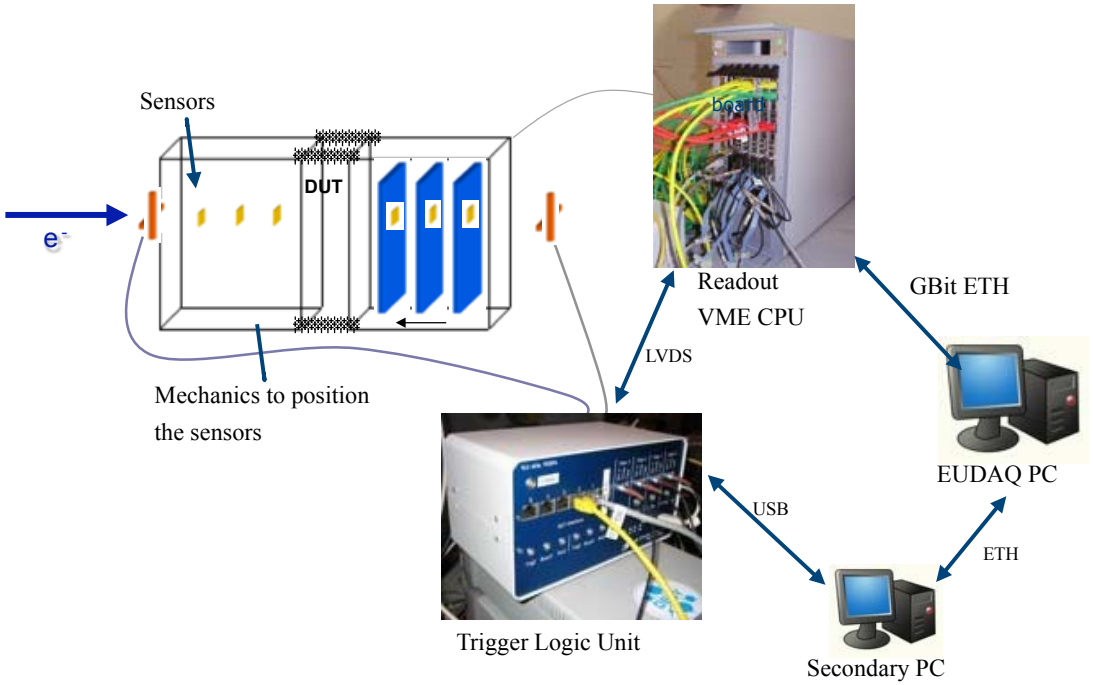
Why?

- Beam Telescope with “Detector Under Test”
  - Need to correlate data from a single particle in all detectors
  - Match tracks in telescope with hits in your DUT



From: Infrastructure for Detector Research and Development towards the International Linear Collider. https://arxiv.org/abs/1201.4657

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  - Distribute central clock/time-stamp to beam telescope and DUT
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  - … can mix time-stamping and triggering: TLU records both trigger-number and time-stamp
- Implementation: Box with signal conditioning and an FPGA
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History - EUDET

- EUDET TLU
  - Supporting beam tests for linear collider detector development at DESY
    - Low rate (< 10kHz)
    - Modest time precision
    - RJ45 for trigger/busy
      - LVDS
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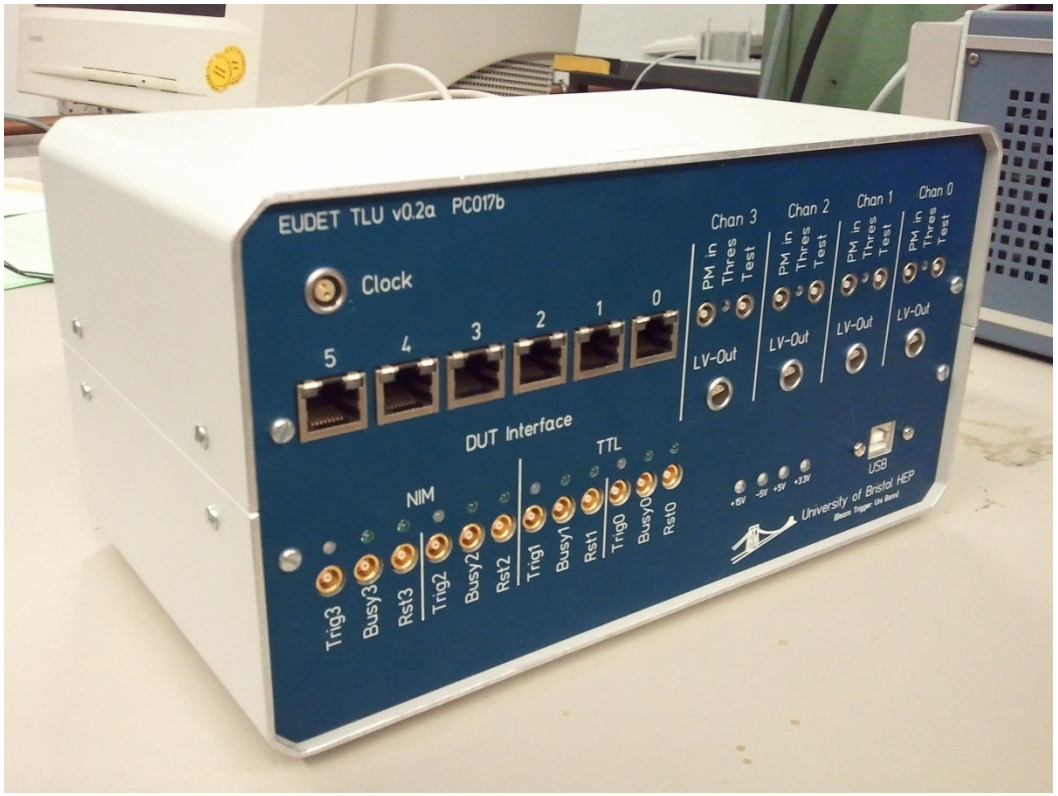
  - Many still in beam-lines and HEP institutes



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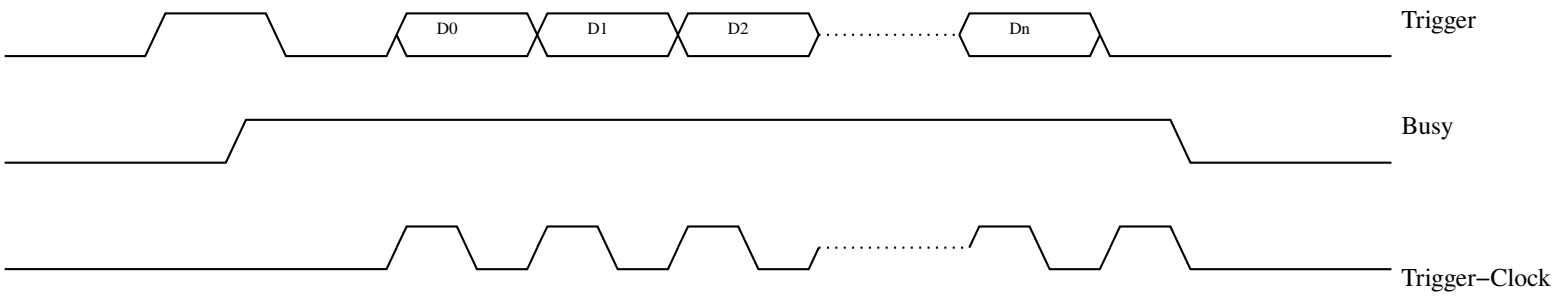

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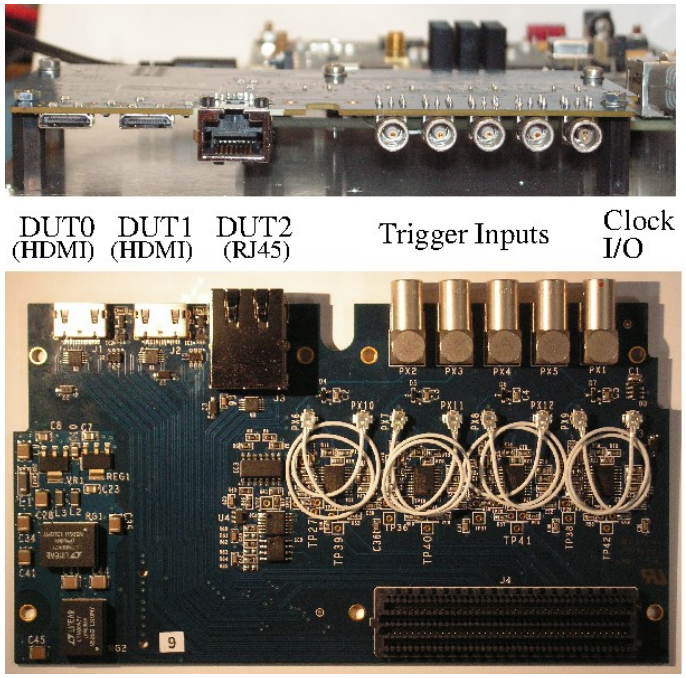

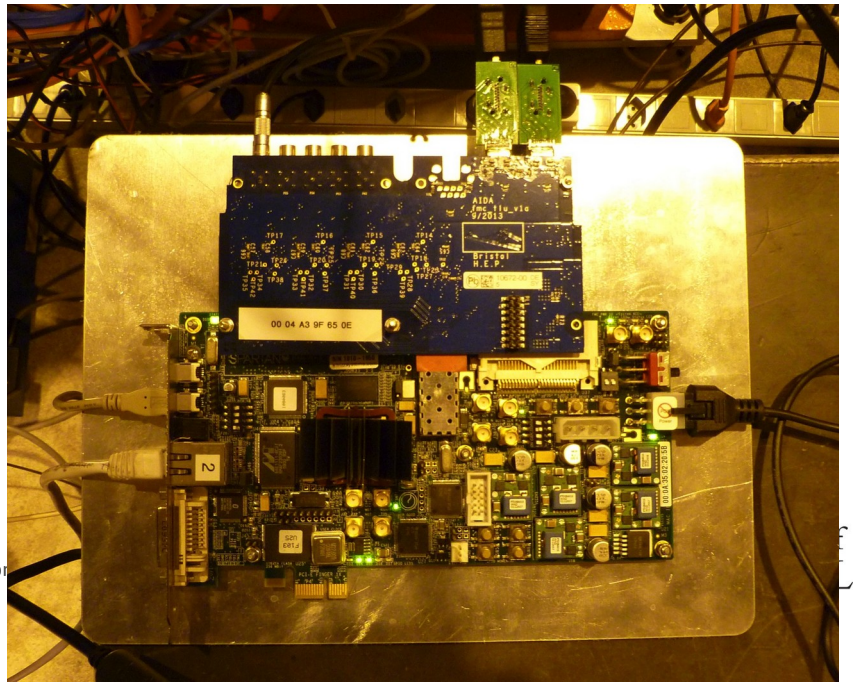

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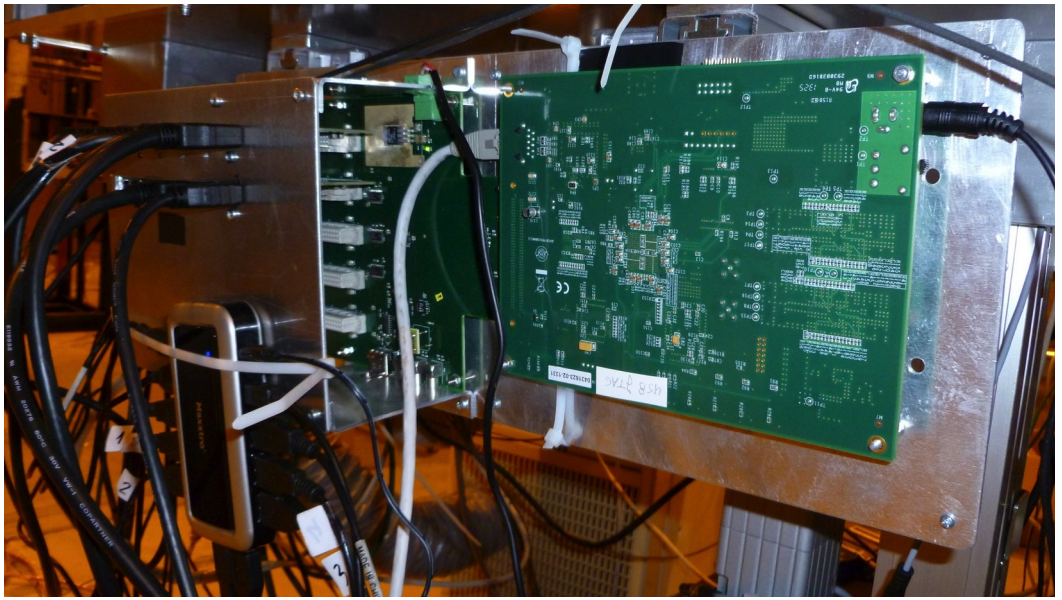

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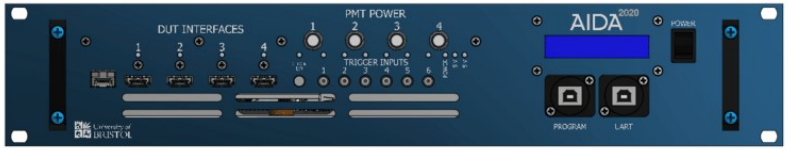
- Hardware permits optical distribution of clock/trigger
- In small desktop case or rack-mount case



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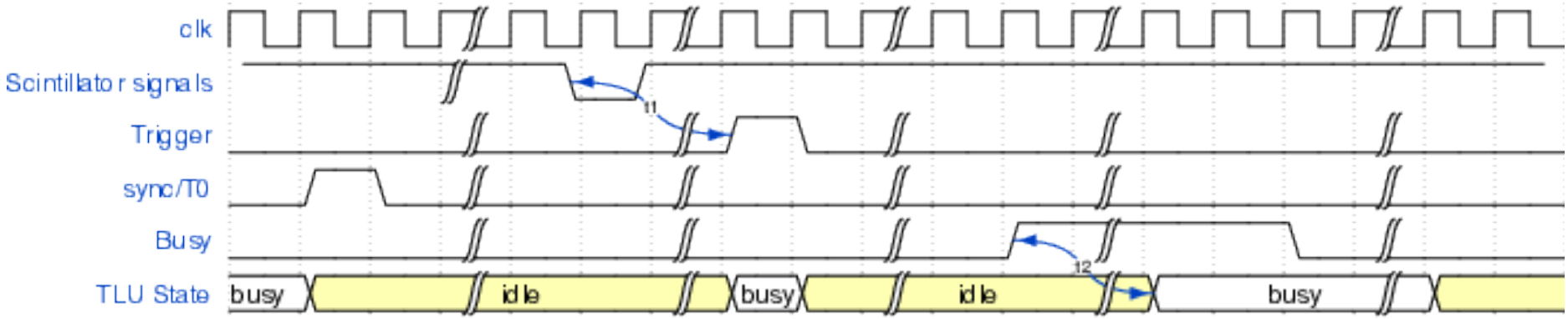
AIDA-2020 TLU – DUT Interfaces

- DUT interfaces can be used in “EUDET mode”
  - Trigger/Busy handshake
    - Need passive HDMI – RJ45 converter
- Can be used with a common clock
  - Permits higher trigger rate
    - No event-by-event handshake. Cross-check on trigger timestamps.



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- LUT programmed with which combinations produce a trigger
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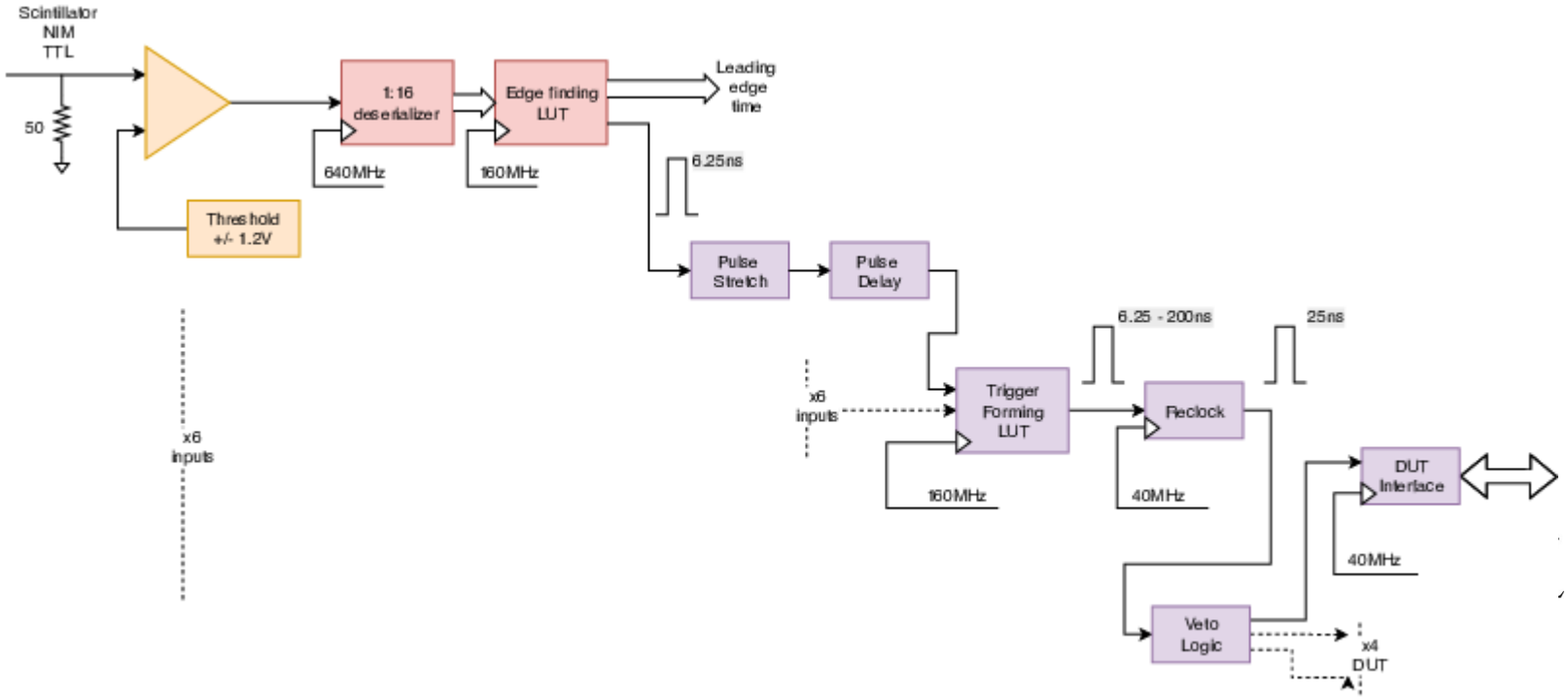

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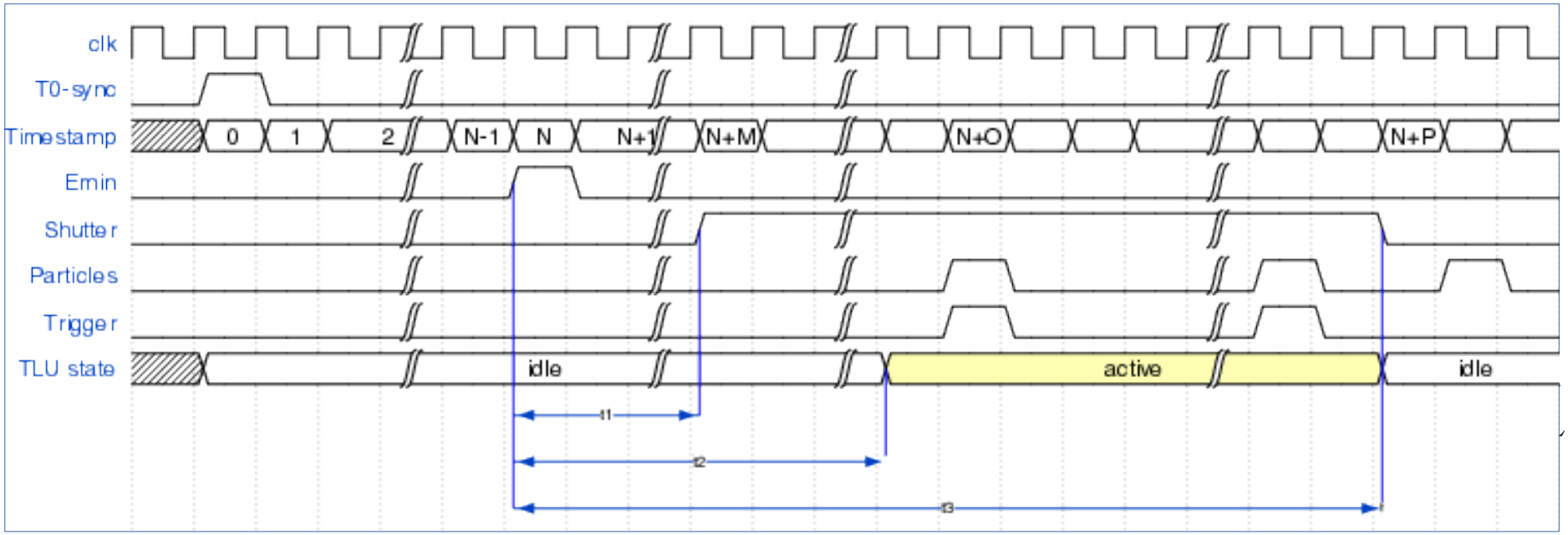
AIDA-2020 TLU DUT “Shutter”

- Some detectors can only capture data with a low duty cycle
- In many beam-lines particle are only present a certain times
  - DESY – 50Hz cycle
  - CERN – SPS cycle
- Detectors active period should occur when particles are present
- → Signal from accelerator can be used to generate a “shutter” signal sent to DUT



Documentation

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- Open Hardware project "AIDA-2020 TLU"
  - https://ohwr.org/project/fmc-mtlu
  - Hardware design files https://ohwr.org/project/fmc-mtlu-hw/
  - Firmware source code https://ohwr.org/project/fmc-mtlu-fw/
- User manual
  https://ohwr.org/project/fmc-mtlu/blob/master/Documentation/Main_TLU.pdf

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Firmware

- IPBus for control and readout of time-stamps
  - UDP/IP 1 Gbit/s Ethernet
- Ipbb build system
  - Scriptable build. Working on CI
- Open Source
  - https://ohwr.org/project/fmc-mtlu-fw/

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Software

- All versions of TLU integrated with EUDAQ DAQ software.
  - Run control
    - Configuration
    - Monitoring
  - Readout of trigger timestamps

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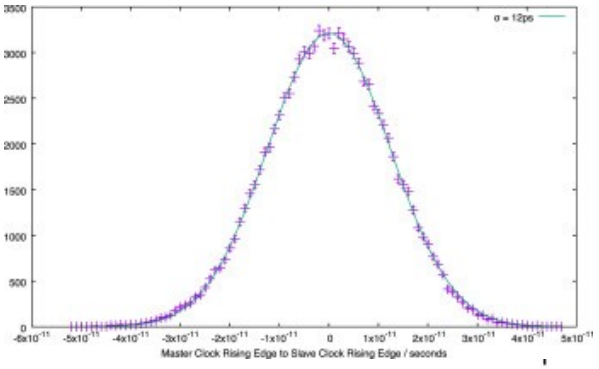
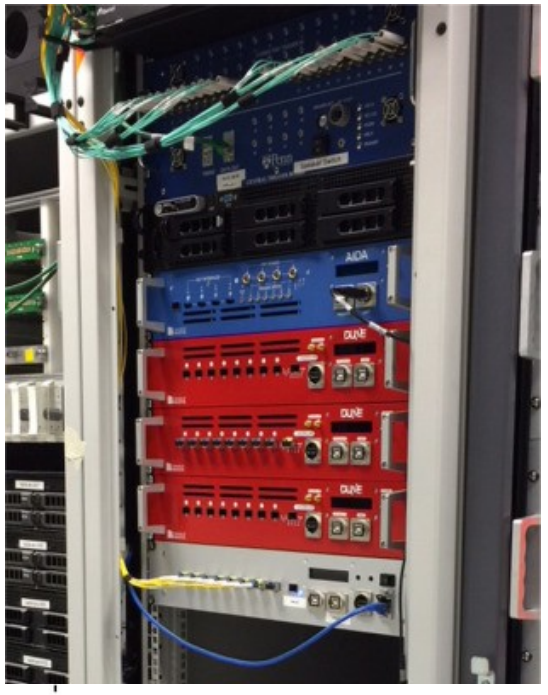
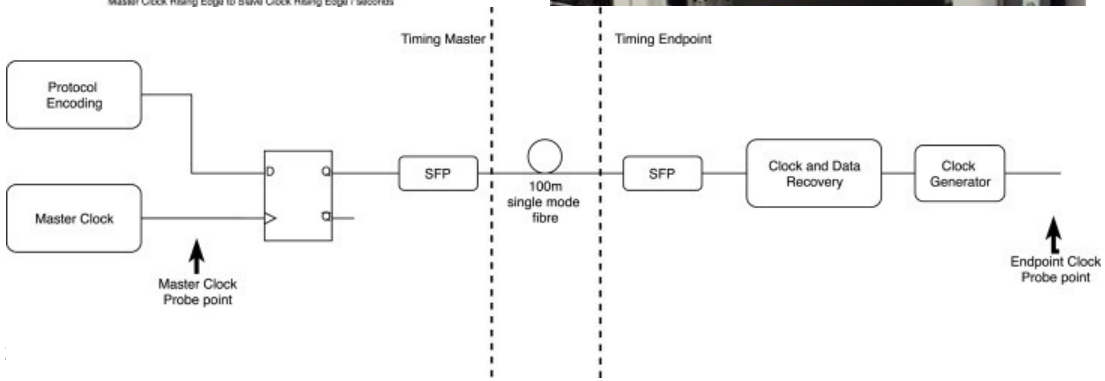
AIDA-2020 TLU Synchronization over fibre

- AIDA-2020 TLU used as synchronization and trigger distribution master in ProtoDUNE-SP tests at CERN
  - Using DUNE firmware
- Signals distributed over optical fibre
- Lab tests: Master → endpoint clock relative jitter σ ~ 12ps

Taken from Timing and synchronization of the DUNE neutrino detector, https://doi.org/10.1016/j.nima.2019.04.097







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AIDA-2020 TLU F/ware, S/ware updates?

- Use external RAM to buffer time-stamps
  - Not useful for continuous beam (e.g DESY)
  - Useful for high-rate CERN beam-tests
    - Take high rate during spill, readout triggers between spills
- Use of “carry chain TDC” implemented in FPGA
  - See e.g. https://ohwr.org/project/tdc-core/
  - Calibration of FPGA carry chain TDCs “fiddly”
  - Likely accuracy of TDC ~ 50ps
    - Current firmware – 781ps bins

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TLU Production

- New production of AIDA-2020 TLUs
  - Organized by DESY.
    - Contact Lennart Huth for details.

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AIDAInnova TLU

- Aim: (tens of) Picosecond Timing (clock distribution and time-stamping)
  - EUDET TLU – Precision ~ 100ns
  - AIDA/AIDA-2020 – Precision ~ 1ns
- Use TDC ASIC for time-stamping triggers?
  - PicoTDC ?
  - Carry-chain TDC inside FPGA probably not adequate (?)
- Constant Fraction Discriminator and/or ADC for time-walk correction?
- ~ 8 inputs
- >= 4 “DUT Interfaces
  - Move away from HDMI → Display Port
    - Passive adaptor HDMI ← → Display port
    - More robust. Better signal integrity on trigger line

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AIDAInnova TLU: Why timing?

- Increasing use of detectors with high timing precision to disentangle events in high-pileup beam-crossings.
  - Testing pico-second detectors requires pico-second time reference
  - Some beam-line users will bring their own time reference detectors. Some would benefit from precise time reference at beam-line
- Could use, e.g. Cherenkov light and high speed photo-detector
  - Used for “TORCH” LHCb upgrade beam-tests
  - MCP-PMT single photon jitter 66ps FWHM
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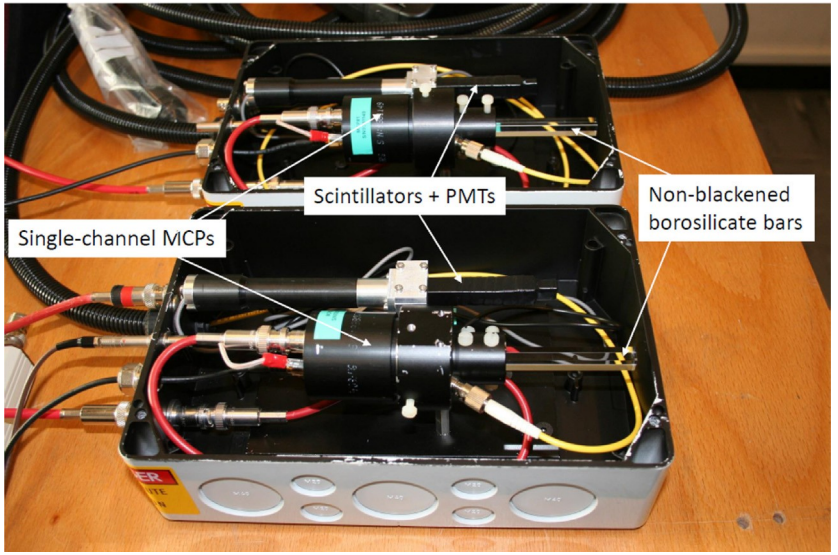

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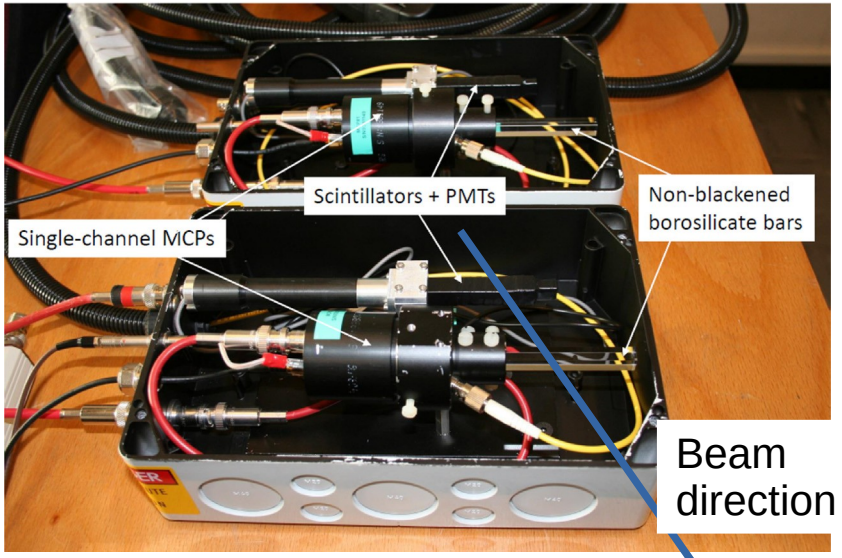

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Summary

- The AIDA family of TLUs provides a way of synchronizing detectors at beam-lines
- Integrated with EUDAQ
- Can be used in home-labs to simplify integration at AIDA supported beam-line
- Open Source hardware/firmware
  - Can be used for applications that require signal conditioning of pulses, clock distribution, FPGA logic.
    - e.g. was used for ProtoDUNE timing system

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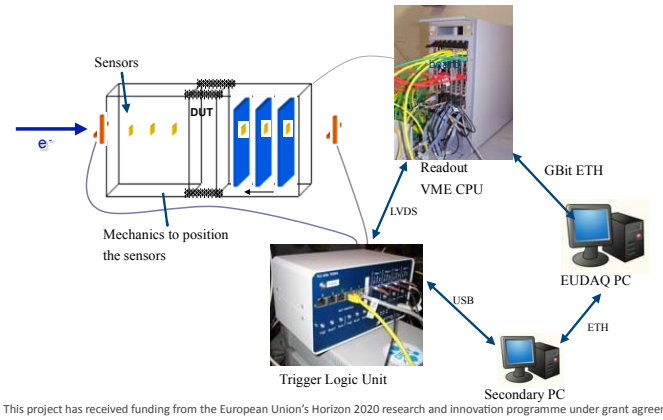

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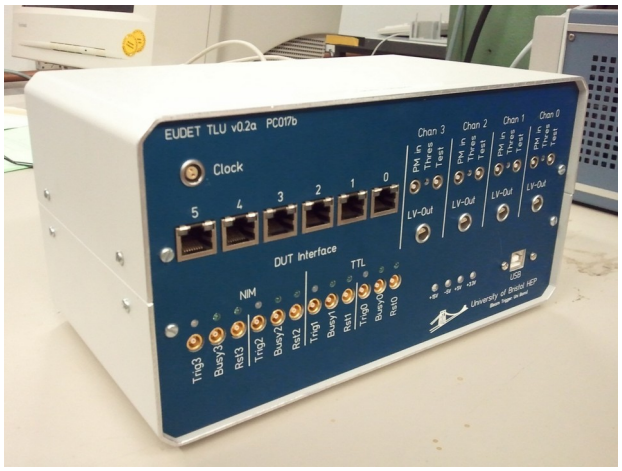

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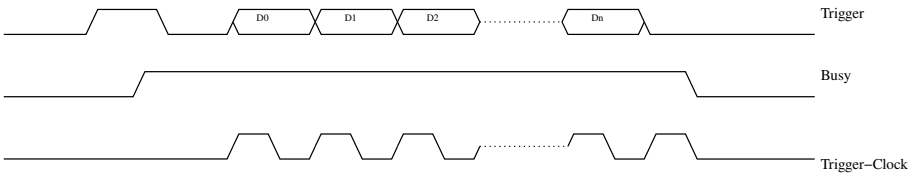

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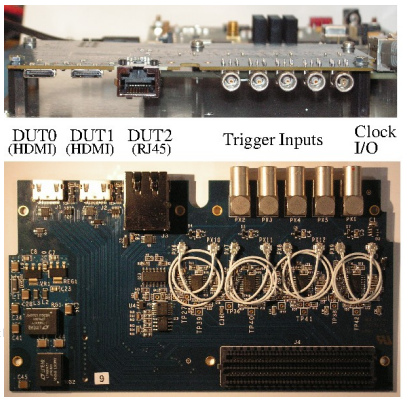

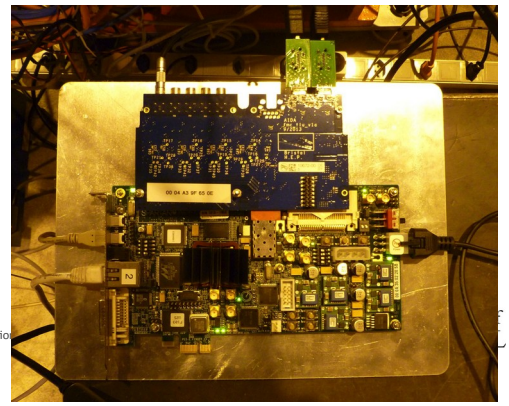

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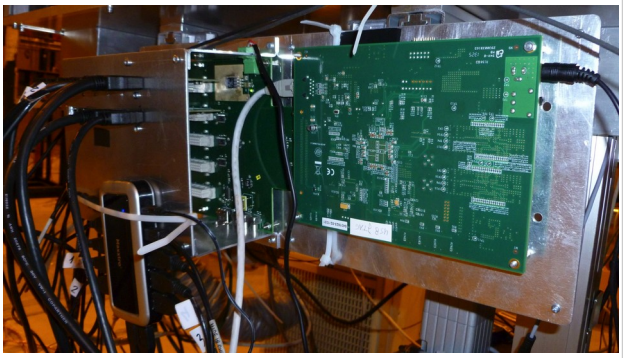

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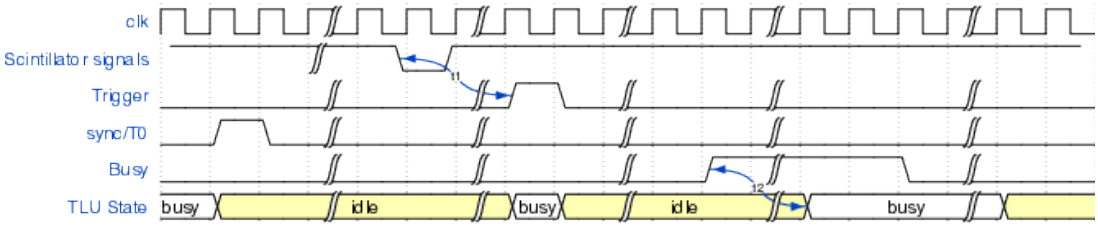

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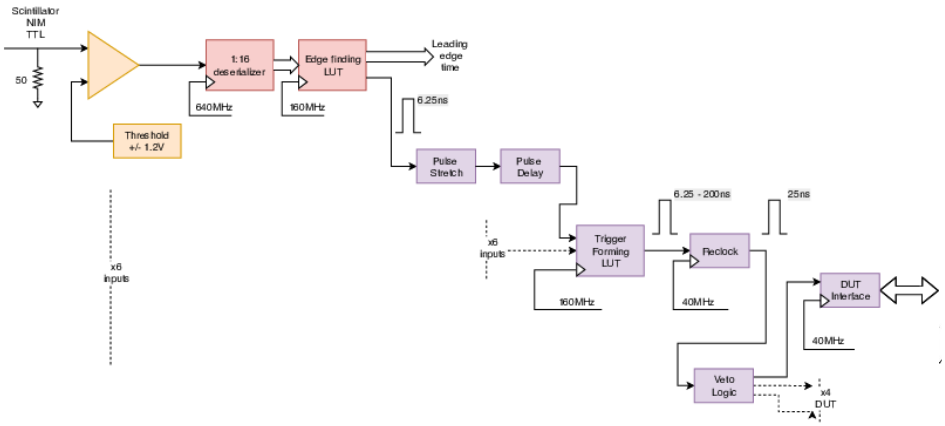

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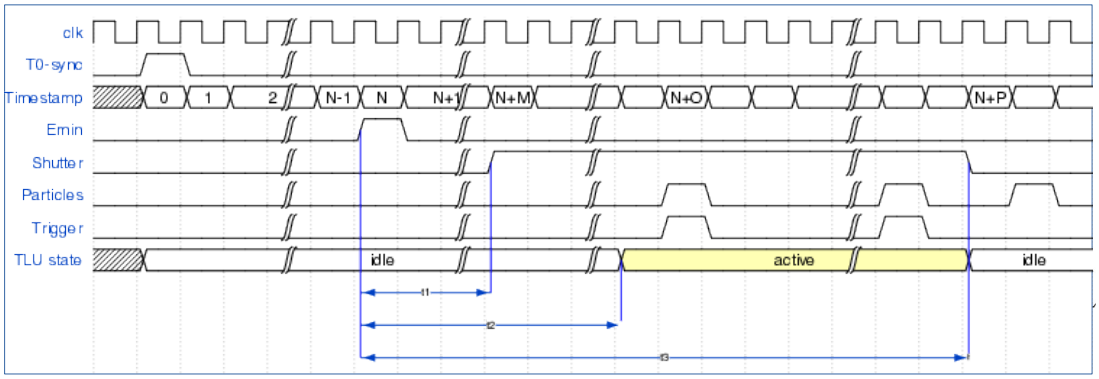

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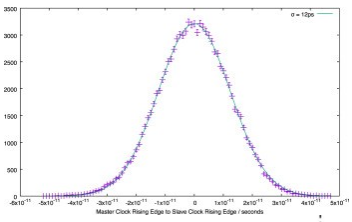
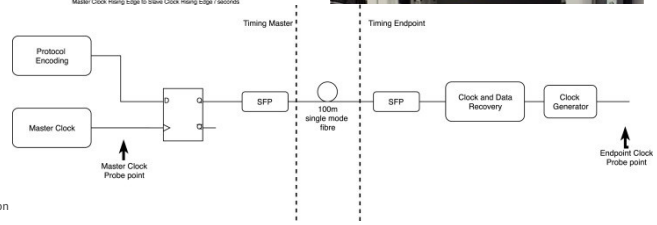
AIDA-2020 TLU Synchronization over fibre

- AIDA-2020 TLU used as synchronization and trigger distribution master in ProtoDUNE-SP tests at CERN
  - Using DUNE firmware
- Signals distributed over optical fibre
- Lab tests: Master → endpoint clock relative jitter σ ~ 12ps

Taken from Timing and synchronization of the DUNE neutrino detector, https://doi.org/10.1016/j.nima.2019.04.097





This project has received funding from the European Union's Horizon

AIDA-2020 TLU
F/ware, S/ware updates?

- Use external RAM to buffer time-stamps
  - Not useful for continuous beam (e.g DESY)
  - Useful for high-rate CERN beam-tests
    - Take high rate during spill, readout triggers between spills
- Use of “carry chain TDC” implemented in FPGA
  - See e.g. https://ohwr.org/project/tdc-core/
  - Calibration of FPGA carry chain TDCs “fiddly”
  - Likely accuracy of TDC ~ 50ps
    - Current firmware – 781ps bins

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TLU Production

- New production of AIDA-2020 TLUs
  - Organized by DESY.
    - Contact Lennart Huth for details.

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AIDAInnova TLU

- Aim: (tens of) Picosecond Timing (clock distribution and time-stamping)
  - EUDET TLU – Precision ~ 100ns
  - AIDA/AIDA-2020 – Precision ~ 1ns
- Use TDC ASIC for time-stamping triggers?
  - PicoTDC ?
  - Carry-chain TDC inside FPGA probably not adequate (?)
- Constant Fraction Discriminator and/or ADC for time-walk correction?
- ~ 8 inputs
- >= 4 “DUT Interfaces
  - Move away from HDMI → Display Port
    - Passive adaptor HDMI ← → Display port
    - More robust. Better signal integrity on trigger line

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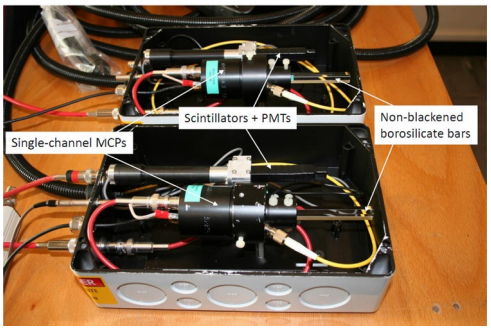
AIDAInnova TLU: Why timing?

- Increasing use of detectors with high timing precision to disentangle events in high-pileup beam-crossings.
  - Testing pico-second detectors requires pico-second time reference
  - Some beam-line users will bring their own time reference detectors. Some would benefit from precise time reference at beam-line
- Could use, e.g. Cherenkov light and high speed photo-detector
  - Used for “TORCH” LHCb upgrade beam-tests
  - MCP-PMT single photon jitter 66ps FWHM
    http://www.photek.co.uk/pdf/datasheets/detectors/DS006%20Photomultiplier%20Tube%20Datasheet%20issue%202.pdf

Taken from http://dx.doi.org/10.1016/j.nima.2016.06.087



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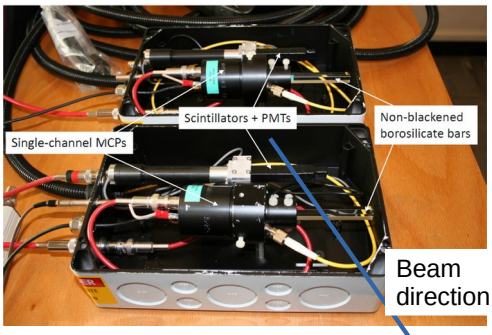
    http://www.photek.co.uk/pdf/datasheets/detectors/DS006%20Photomultiplier%20Tube%20Datasheet%20issue%202.pdf
    - For many photons timing precision ~ 10ps

Taken from http://dx.doi.org/10.1016/j.nima.2016.06.087



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Summary

- The AIDA family of TLUs provides a way of synchronizing detectors at beam-lines
- Integrated with EUDAQ
- Can be used in home-labs to simplify integration at AIDA supported beam-line
- Open Source hardware/firmware
  - Can be used for applications that require signal conditioning of pulses, clock distribution, FPGA logic.
    - e.g. was used for ProtoDUNE timing system

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