Recent Improvements of the Caribou DAQ System

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BTTB9 Workshop
2021/02/08

Outline:

Motivation and overview
Recent improvements
Ongoing developments and future plans
Conclusions

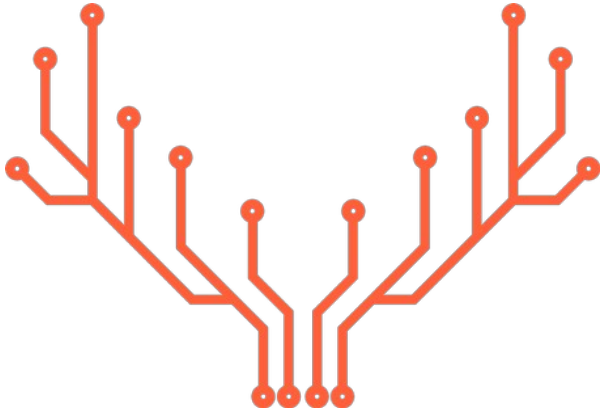
Motivation

- Many different silicon detector technologies under investigation
  - Typically single-chip prototypes with a lifetime of a few years
  - Similar DAQ requirements: readout, control, powering for most silicon pixel detectors
  - Differences in voltage levels, number of channels (data/voltage) or protocols
- A versatile DAQ system can significantly reduce time and cost for DAQ development
  - Re-usable hardware, firmware and software core components
  - Few changes/FW modules to write, large parts of system well tested

The Caribou Data Acquisition System

- Open source hardware, firmware and software for laboratory and high-rate beam tests

- Goal: Provide a versatile DAQ system which
  - minimizes device integration effort
  - reduces time to get first data from a new detector
- Developed & maintained by collective effort



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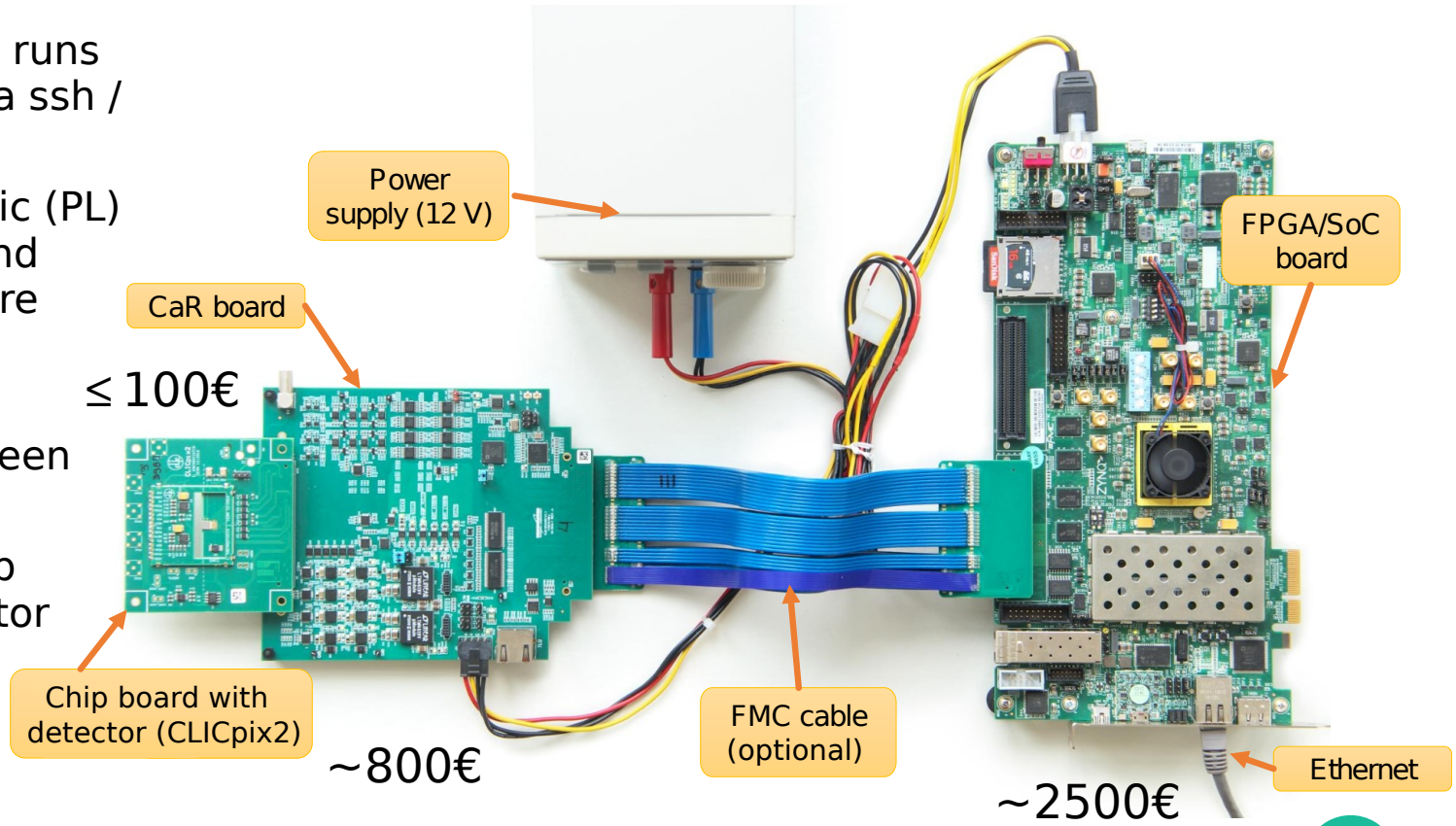
System Overview

- System on Chip (SoC) Processing System (PS) runs Linux, user connects via ssh / Ethernet
- SoC Programmable Logic (PL) runs detector control and data processing firmware
- Periphery CaR board provides resources and physical interface between SoC and detector
- Application-specific chip board containing detector
- No additional DAQ PC required!

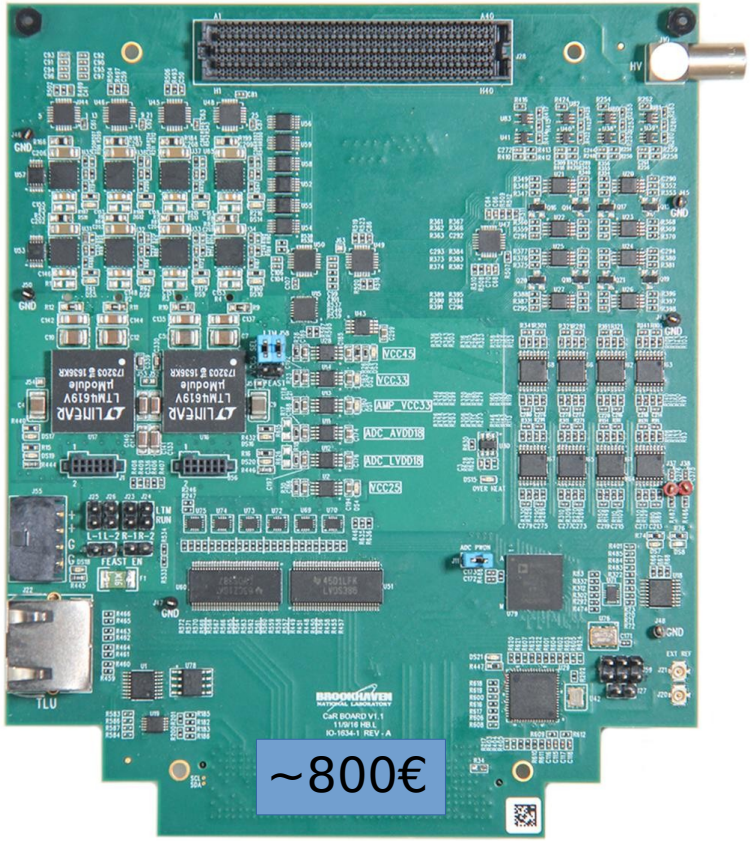


The Hardware: SoC Evaluation Board

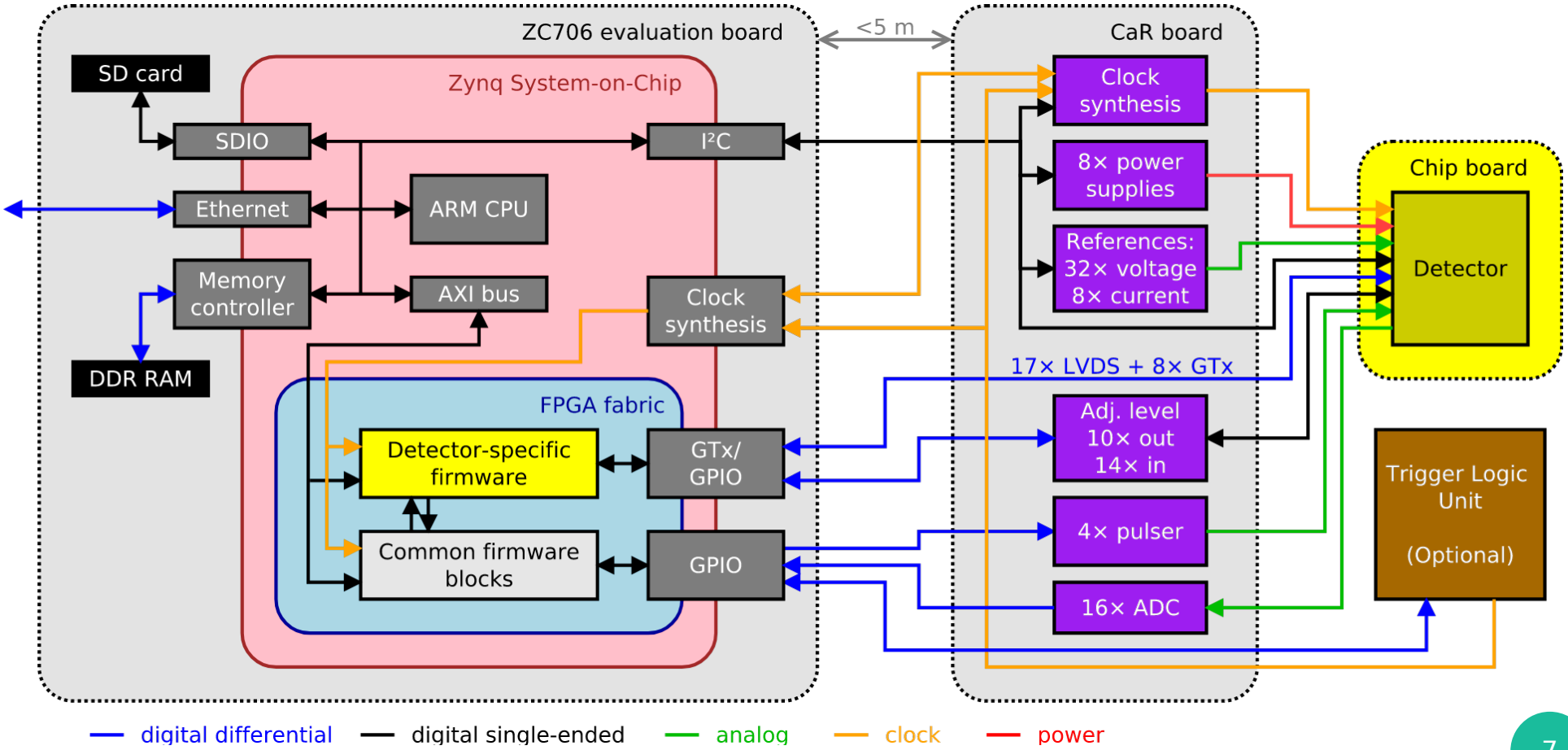
- Based on Xilinx Zynq series, currently supported: ZC706
  - PS (embedded ARM CPU) runs full Linux operating system
  - Standalone machine, connect to via Ethernet (ssh)
  - Runs DAQ software (Peary)
  - Allows to run data analysis (quality monitoring) locally
  - Data stored locally (on SD card) or on network-mounted storage (NFS, …)
- PL runs custom firmware blocks for data processing, detector control
  - Interface between FPGA fabric and CPU available
  - Firmware for signalling & lower layers of communication protocols
  - Possibility to (pre)process data in hardware
  - DMA (direct memory access) available in architecture, currently not implemented → higher DAQ bandwidth

The Hardware: Control and Readout Board (CaR)

- Provides physical interface from the FPGA/SoC to the detector chip and hardware resources
  - 8 adjustable power supplies with monitoring (0.8 – 3.6 V, 3A)
  - 32 adjustable voltage references (0 – 4 V)
  - 8 adjustable current references (0 – 1 mA)
  - 8 voltage inputs to slow (50 kSPS) 12-bit ADC (0 – 4 V)
  - 16 analog inputs to fast (65 MSPS) 14-bit ADC (0 – 1 V)
  - 4 programmable injection pulsers
  - 8 full-duplex high-speed GTx links (<12 Gb/s)
  - 17 LVDS links (bidirectional)
  - 10/14 output and input links, adjustable level (0.8 – 3.6 V)
  - Programmable clock generator, External inputs for high voltage, clock reference, trigger
  - Interfaces: FMC to FPGA, 320-pin SEARAY to detector



The Hardware: Schematic



The Firmware and Software

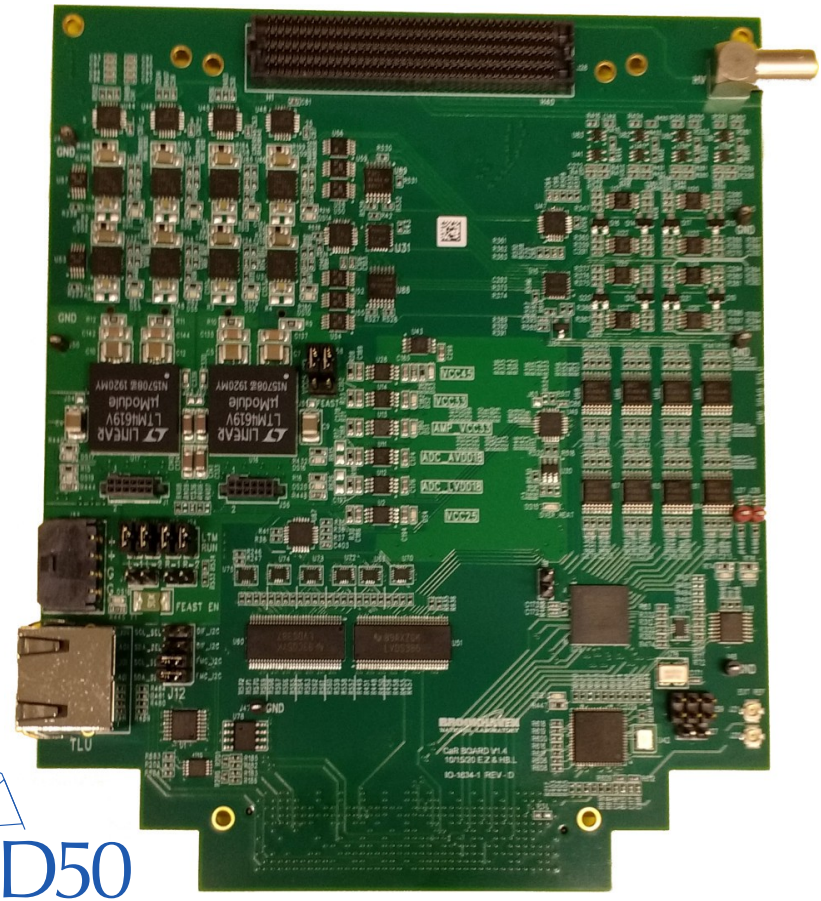
- **Firmware**: Based on combination of custom Caribou modules and commercial Xilinx IP cores
  - Provides an interface between CPU (SW) and a detector (HW)
  - Modules are connected to CPU through AXI bus
  - Registers are mapped to CPU memory space (/dev/mem)

- **Software Stack**: Custom Yocto-based Linux distribution (meta-caribou)
  - Common Linux tools and packages are pre-installed (ssh, python etc.)
  - Includes Caribou software (EUDAQ, Peary)

- **DAQ Software Framework**: Peary
  - Hardware Abstraction Layer (HAL) to handle peripherals as objects in C++
  - Functions to control CaR board, set/measure voltages, capture ADC, ...
  - Various user interfaces: command line, scripting, EUDAQ2 producer for test beam integration

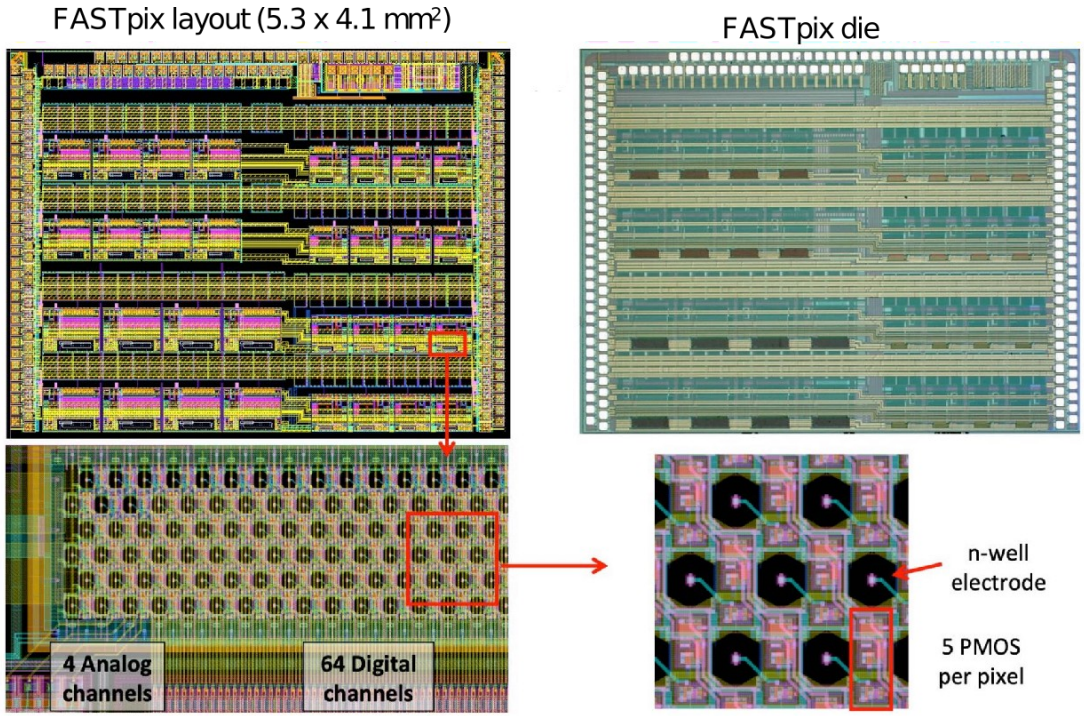
New CaR Board Revision

- New revision 1.4 of CaR board
  - Overcurrent protection
  - Chip board selection in software
- Prototype board (v1.3) tested and integrated into Peary
- Batch of 20 new boards arrived
  - Testing of the boards is ongoing
  - Will be distributed to RD50 institutes:
    - CERN, DESY, Univ. of Liverpool, IFIC Valencia, HEPHY Vienna, JSI Ljubljana, Univ. Sevilla, NIKHEF, Lancaster U.
  - Testing of RD50-MPW1/2, 65nm MLR1, ...



Implementation Example: ATTRACT FASTpix

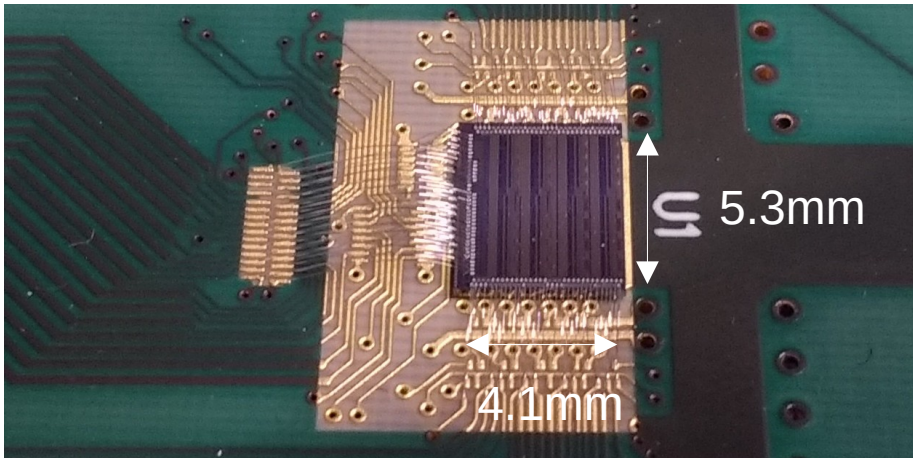
- Technology demonstrator for monolithic pixel detector with sub nanosecond timing
- Implemented in modified 180nm CMOS imaging process
- 32 matrices of hexagonal pixels:
  - 4 pixel pitches: 8.66, 10, 15, 20 µm
  - 8 pixel designs: combination of process and layout variations
- In each matrix: 4 analog channels, 64 digital channels
- Digital matrix: 1 LVDS fast OR of pixel signals, 2 LVDS ToT / pixel encoding via delay lines
- 1 LVDS for test-pulse injection
- Precursor of test chips in recent 65nm CMOS Multi-Layer-Reticle submission MLR1

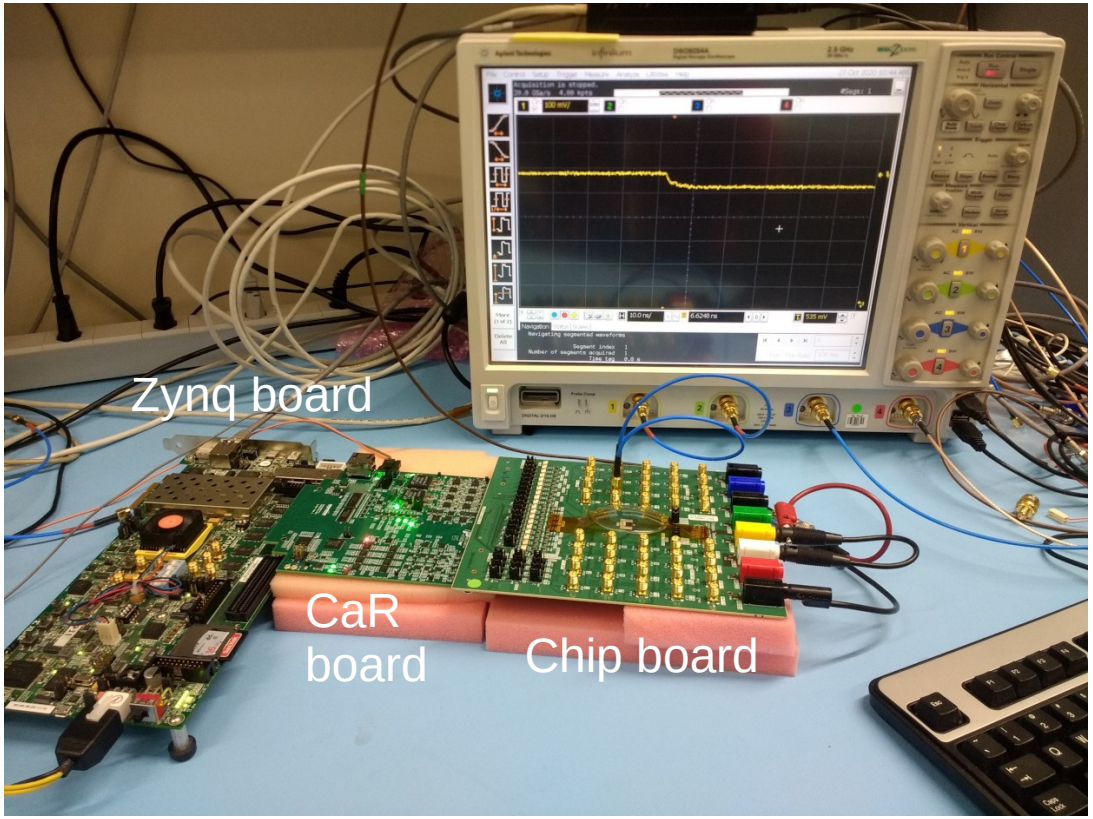


T. Kugathasan et al.: https://doi.org/10.1016/j.nima.2020.164461

FASTpix Integration

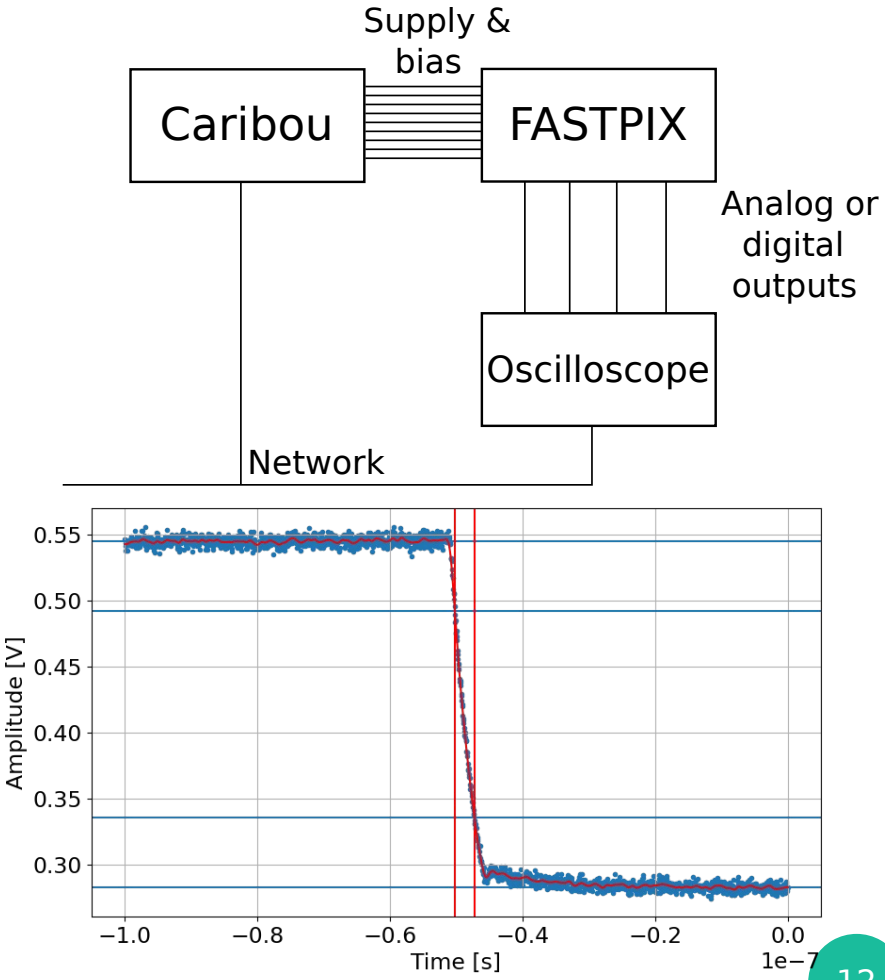
- Test setup controlled by Caribou
  - Connected to chip board with FASTpix
  - Readout of analog and digital outputs over network with oscilloscope
    - Requires high bandwidth and good time resolution





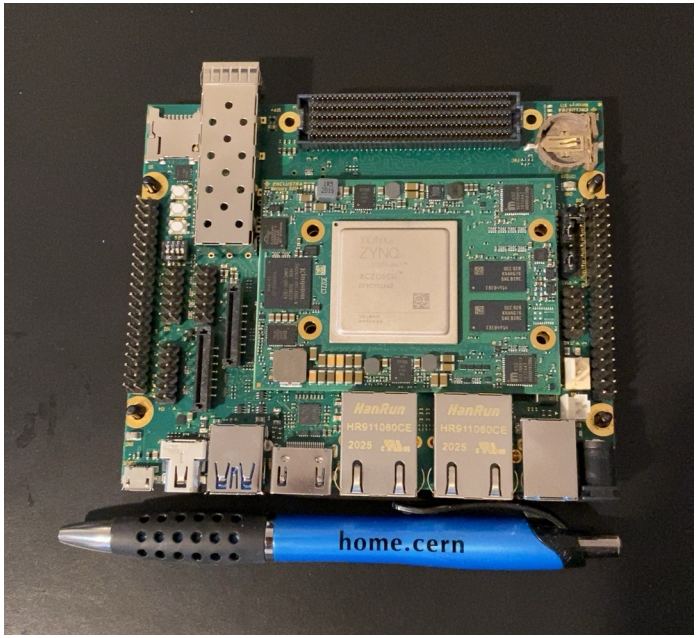
FASTpix Integration

- FASTpix and oscilloscope controlled by Peary
- Supply voltages, bias voltages and currents provided by CaR board
  - Can be controlled and monitored in software
  - Tuning of all chip parameters in software
- Oscilloscope (DSO9254A) is read out by Peary over network
  - Raw waveforms are recorded and stored by Peary for offline analysis
  - Scans can be automated in Peary
- Implementation of other oscilloscopes in progress



Future Plans

- Reduce size and cost of Caribou system by integrating CaR board and SoC board:
  - Custom carrier board with regulators, current sources…
  - Equipped with commercial SoC mezzanine board
- Upgrade from Zynq-7000 to UltraScale+ Zynq
  - Increased CPU performance
  - Requires porting of FW, OS stack and Peary



Conclusions and Outlook

- Caribou system supported and used by various collaborations:
  - Part of the CERN EP R&D program, WP1.4: Si Simulation and Characterization
  - Part of the AIDAinnova project, WP3: Testbeam and DAQ Infrastructure
  - RD50 project
- Strong & continued collaboration on future Caribou system development and support

Getting Started

- Caribou paper: https://cds.cern.ch/record/2703500
- Gitlab: https://gitlab.cern.ch/Caribou

- Caribou meetings
  - Indico: https://indico.cern.ch/category/13530/
  - E-group: caribou-users