The silicon strip telescope at FTBF

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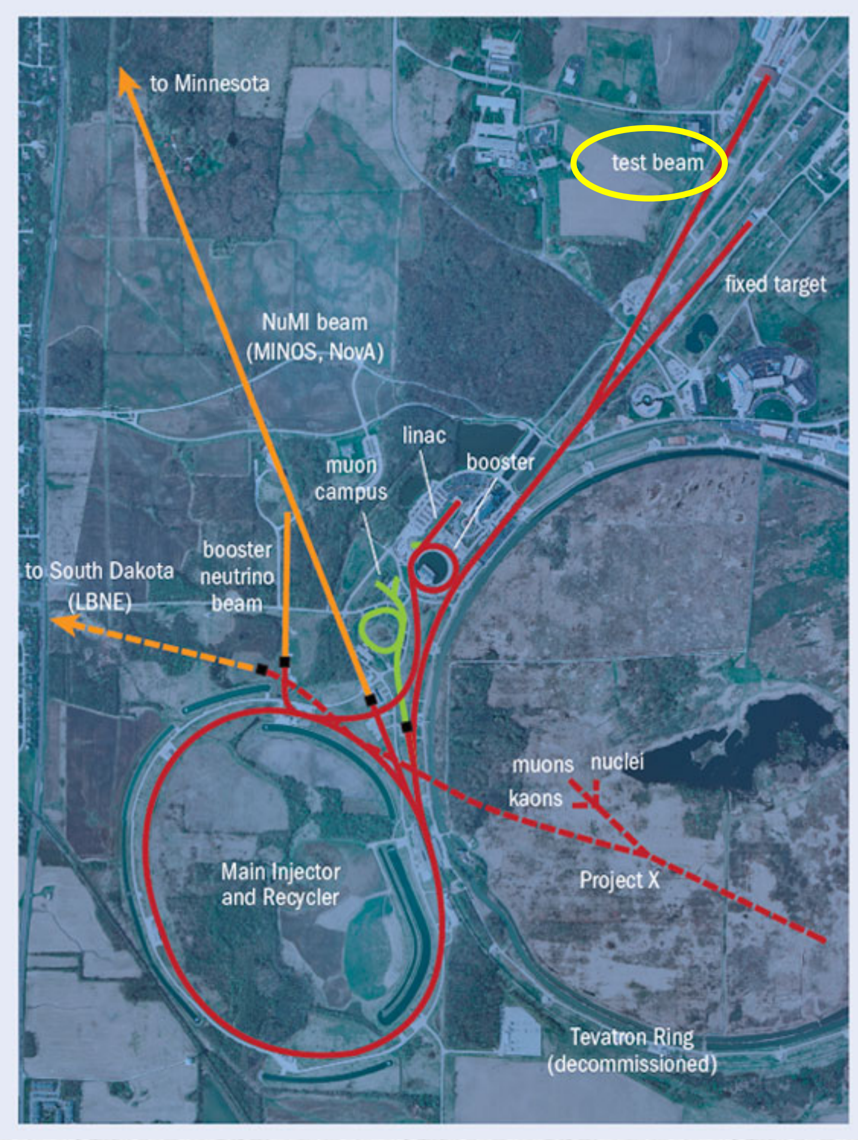
On behalf of the CMS tracker group

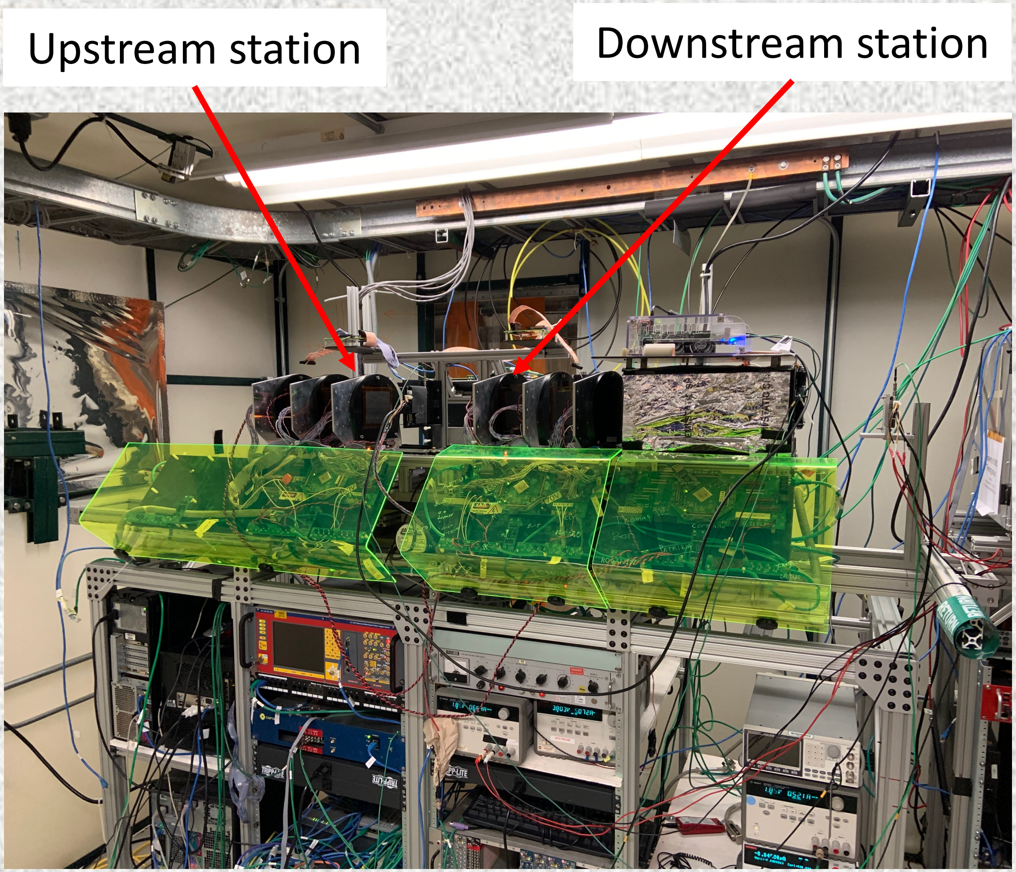
Fermilab Test Beam Facility (FTBF)



- Main Injector accelerates protons to 120 GeV
  - Accelerating RF frequency: 53 MHz
  - Ring circumference: 11.13 µs
- Up to 800k protons per spill to test area over 4.2 seconds, repeated every 60 seconds
- Secondary beams including kaons, pions, electrons and muons

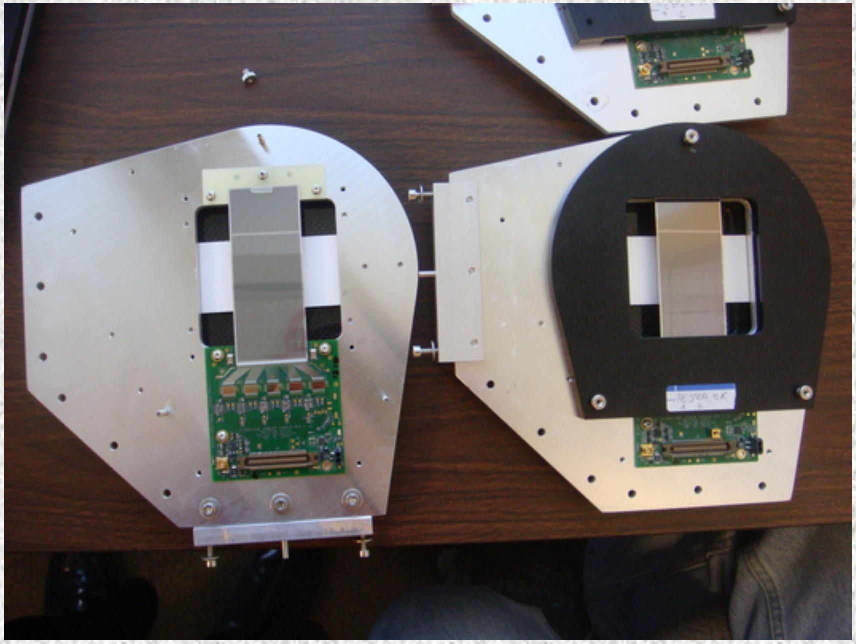
Introduction

- The Fermilab Test Beam Facility provides user a silicon strip based telescope to reconstruct the trajectories of the particles
- The telescope is composed by 12 planes, 6 upstream and 6 downstream the Detector Under Test (DUTs) station
- The two arms can be moved to leave enough space for any device to be mounted on a remotely controlled moving table
- A dry air system and a chiller + Peltier cells system can be used to keep the DUTs at controlled humidity and temperature



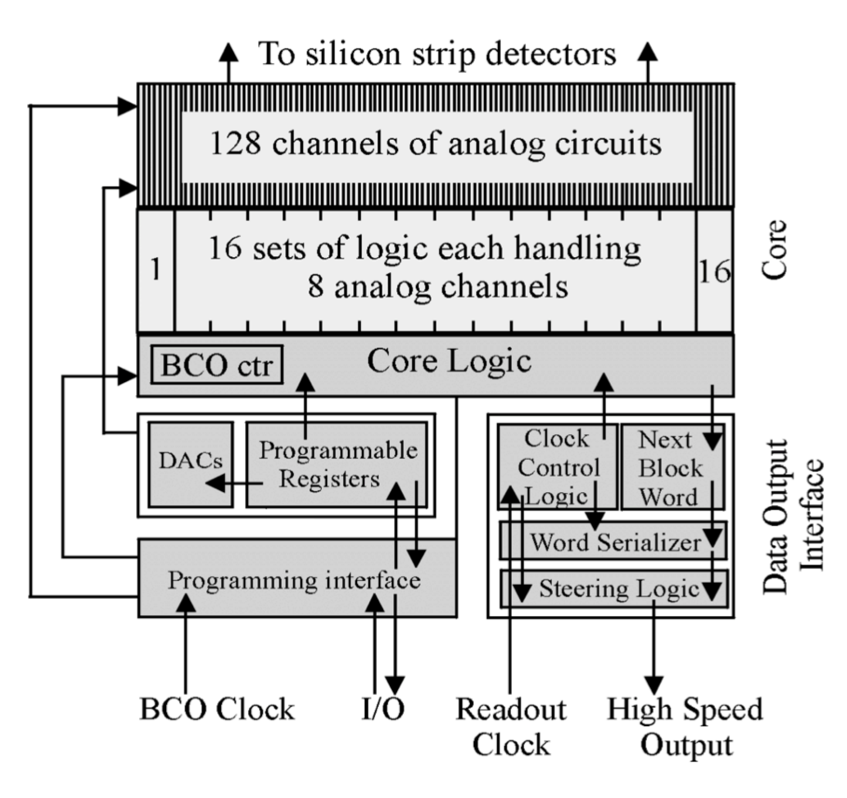
Sensors

- Each sensor has 640 strips and a thickness of 320 µm
- Strip pitch is 30 µm
- The readout pitch is 60 µm, exploiting the capacitive charge-division
- Each station is composed by two sensors mounted on a support, rotated by 90 deg relative to each other
  - a 2D hit position can be reconstructed from each pair of sensors
- The supports are tilted by 15 deg around the vertical axis
- The overlap area of the two sensors is 3.8 x 3.8 cm^2



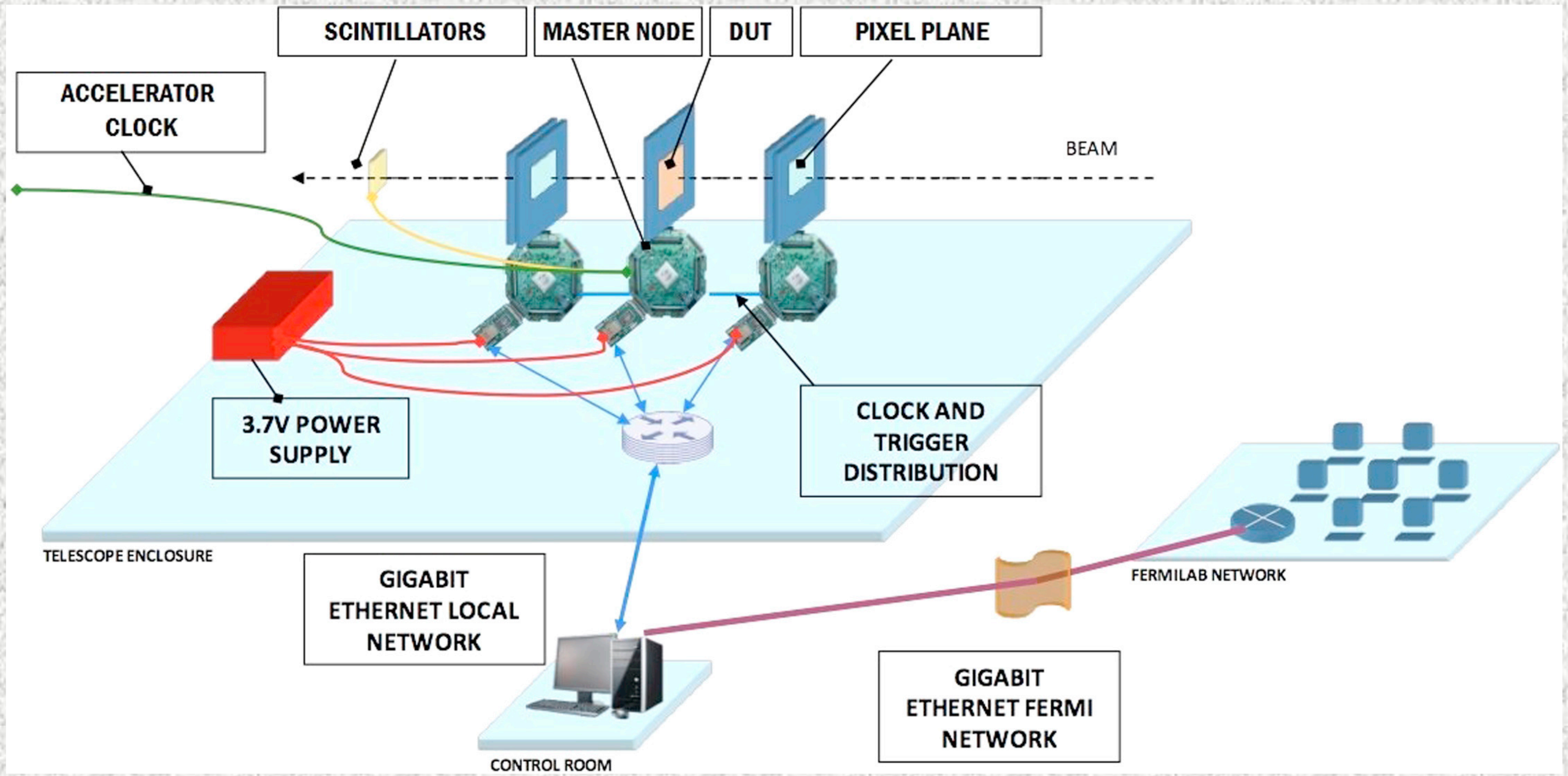
Readout chip (FSSR2)

- 0.25 µm CMOS process
- 128 analog inputs
- Independent Beam Crossing Oscillator (BCO) and readout clocks
  - The BCO has 8 bits and is used to tag the incoming data
  - Readout clock runs at up to 70 MHz
- Data driven readout: all data that are above threshold are transmitted
- Both sensors and ROCs are leftover production for the cancelled D0 Run IIb



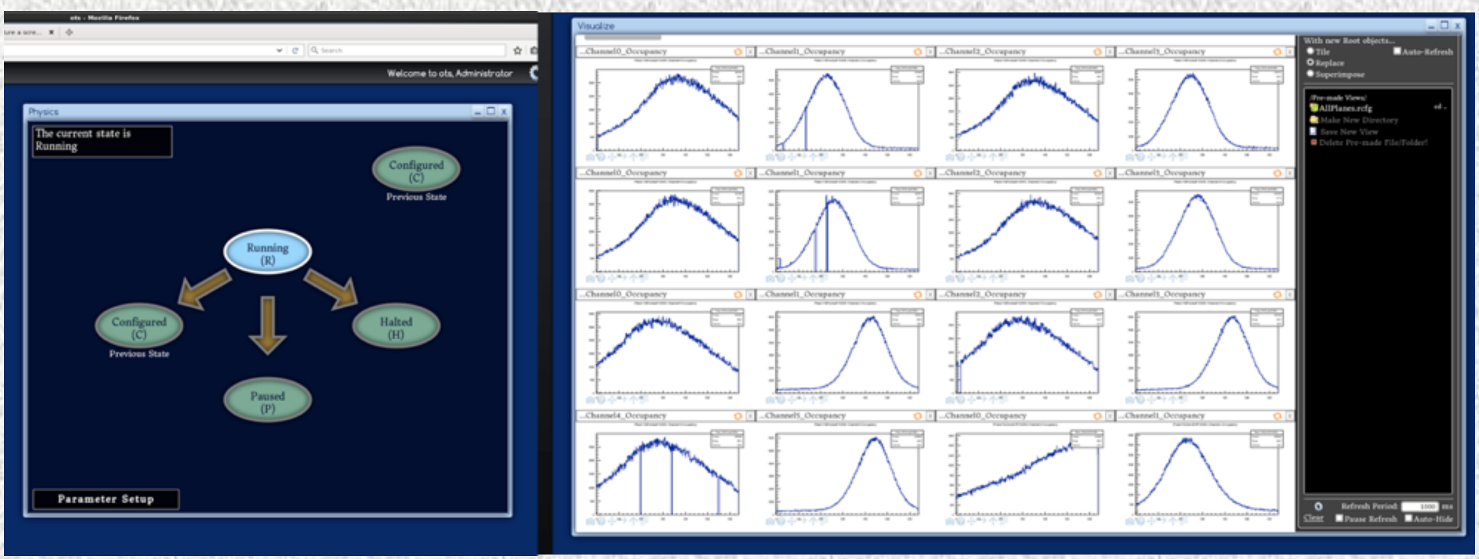
Telescope readout - 1

- DAQ is based on the CAPTAN hardware (Compact and Programmable daTa Acquisition Node) designed few years ago at Fermilab
- Simple FPGA board with an Ethernet link
- The DAQ can operate safely up 50 kHz trigger rate



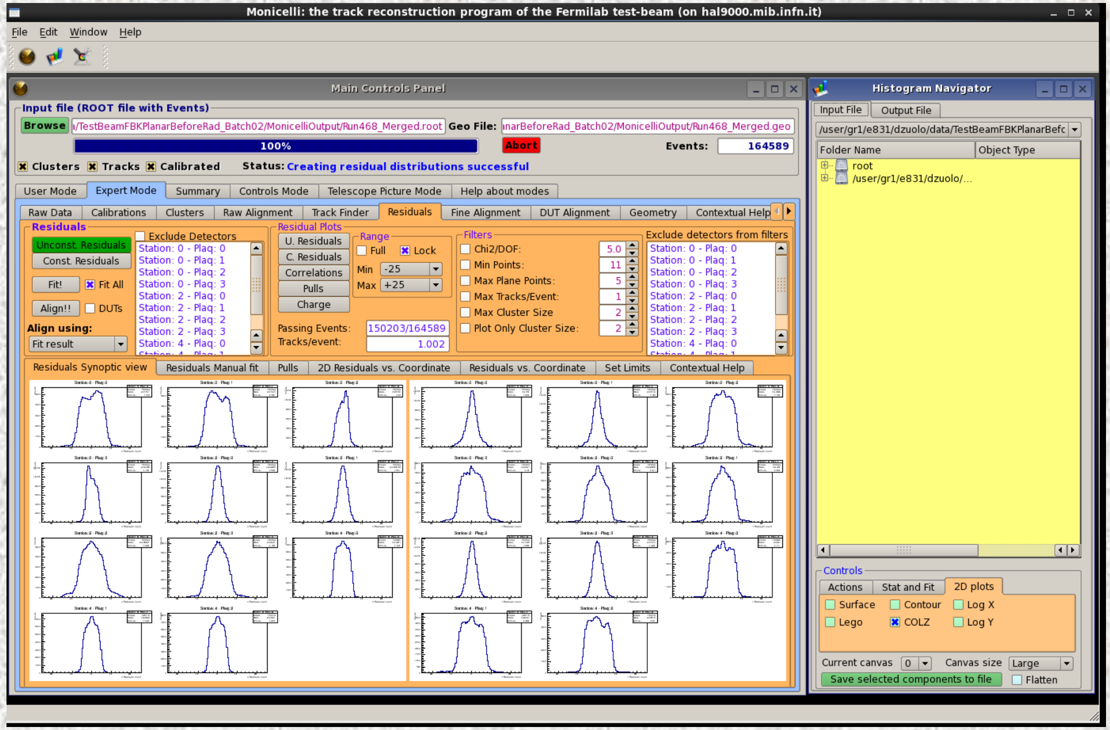
Telescope readout - 2

- The Fermilab computing division is developing an Off The Shelf Data Acquisition (OTSDAQ), based on the XDAQ CMS framework
- OTSDAQ is used to take data with the silicon strip telescope and allows easy integration of any DUT by means of
  - a DAQ interface providing standard Finite State Machine functions (“Configure”,”Start”,”Stop”)
  - a low level C++ interface to its readout chip
- Most of the CMS Fermilab based experimenters, CMS Inner and Outer Tracker, CMS Timing, CMS HGCAL have been fully integrated in OTSDAQ and are taking data synchronized with this telescope



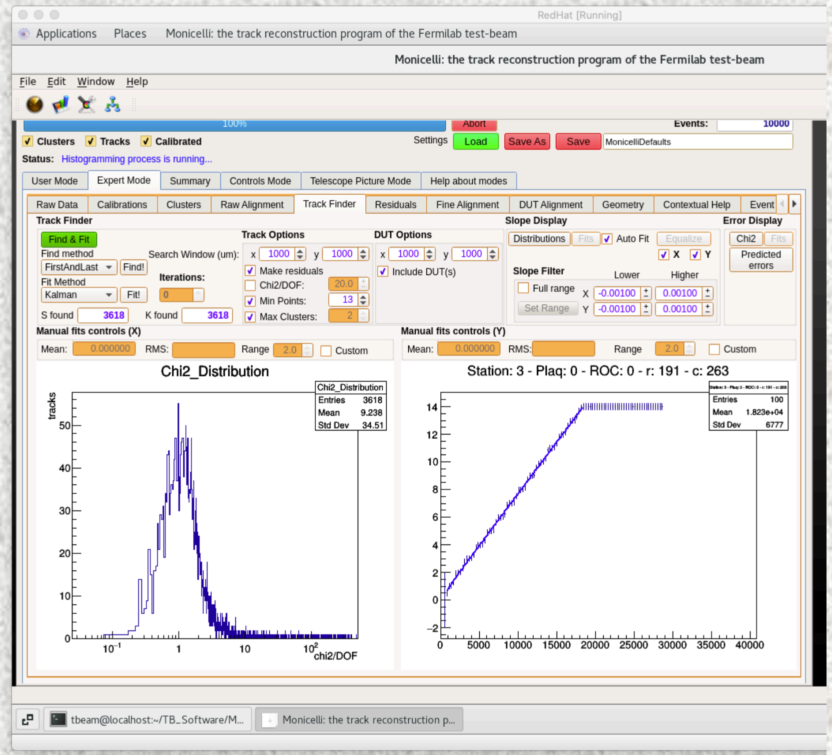
Track reconstruction and alignment - 1

- Track reconstruction and telescope alignment are performed by means of a C++ based package called [Monicelli](), developed and maintained by a FNAL - INFN Milano - Bicocca team
- A graphical interface guides the user through the steps of the procedure
- The program processes two files: the raw data file and an XML file containing the geometry of the telescope (positions and rotations of each plane and its readout chips)



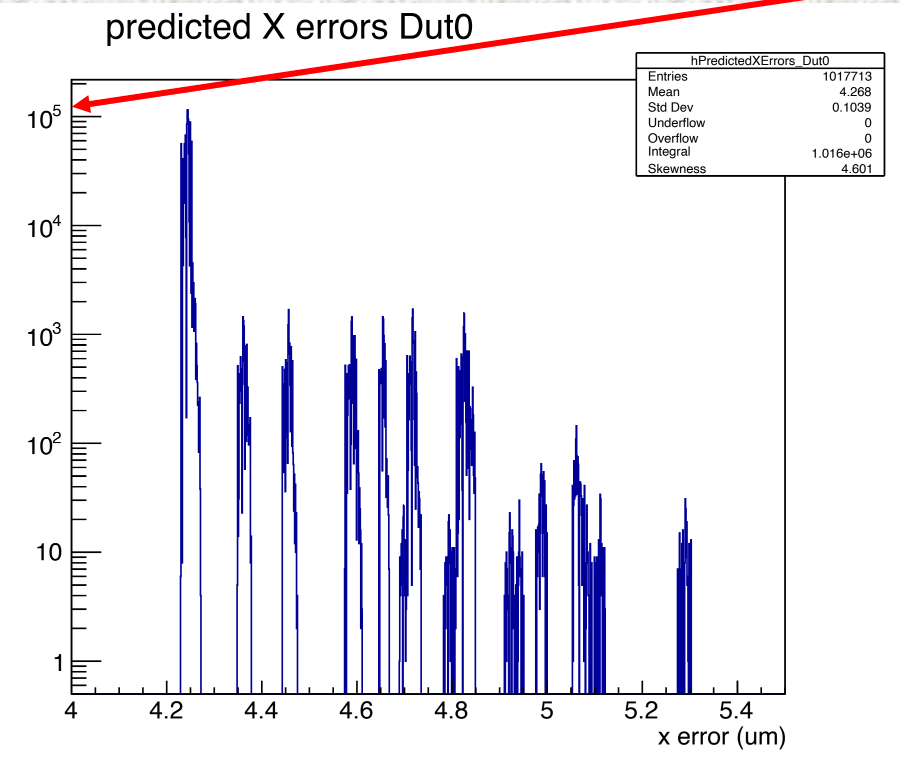
Track reconstruction and alignment - 2

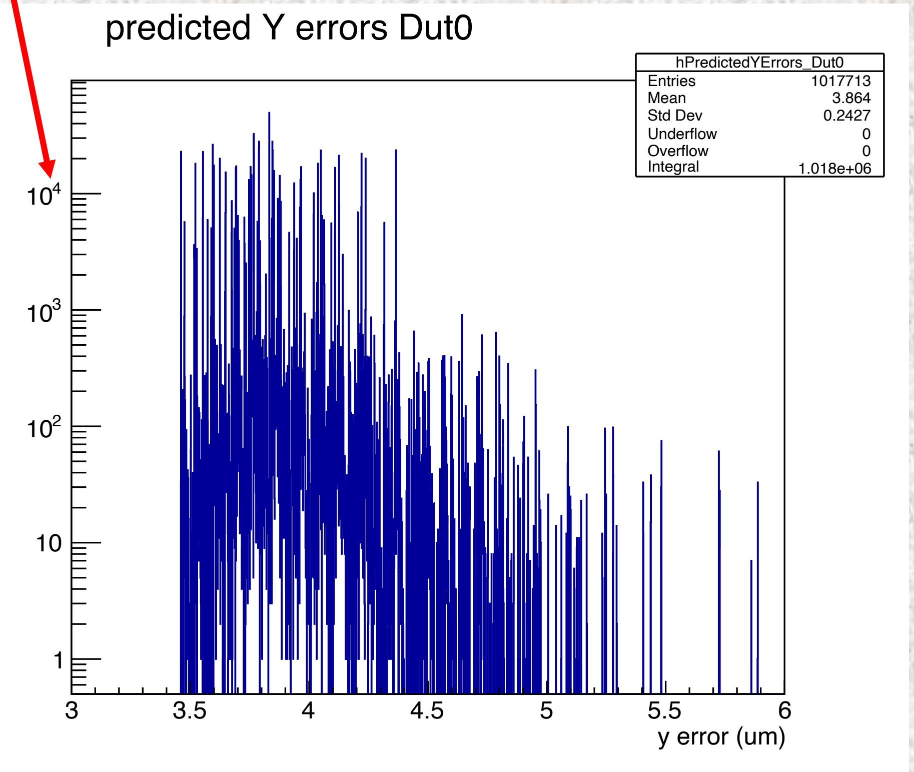
- The algorithm exploits the [Kalman filter] to get the best track parameters and impact point coordinates + errors at each plane of the telescope
- Control histograms can be produced and visualized at each step in order to verify the status of the alignment
- Final ROOT n-tuples contain the reconstructed tracks and the associated hits on each plane and DUT
- A new geometry file can be produced containing the updated geometry
- Another C++ package called [Chewie] is available to analyse the final n-tuples



Predicted errors on DUT

!!!Please note the log-scale!!!





Tilted telescope planes

Probability (size 2 clusters) >> Probability (size 1 clusters)

Peaked structure arises

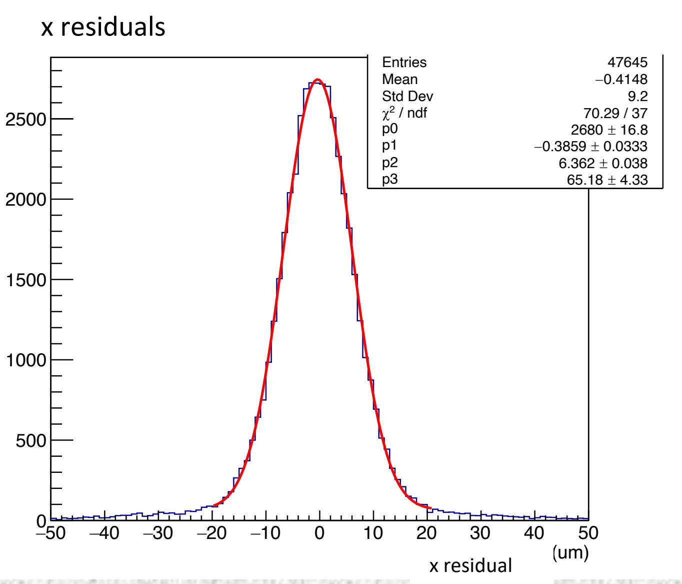
Not tilted telescope planes

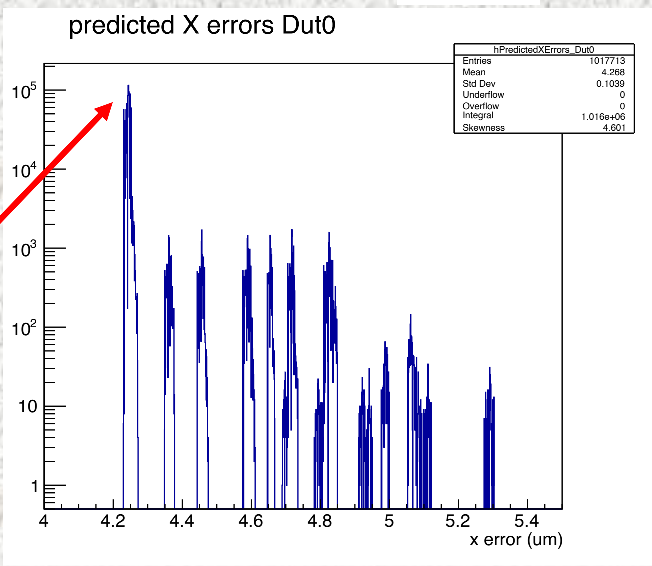
Equal probability of size 2 vs size 1 clusters

No peaks

Checking the predicted errors - 1

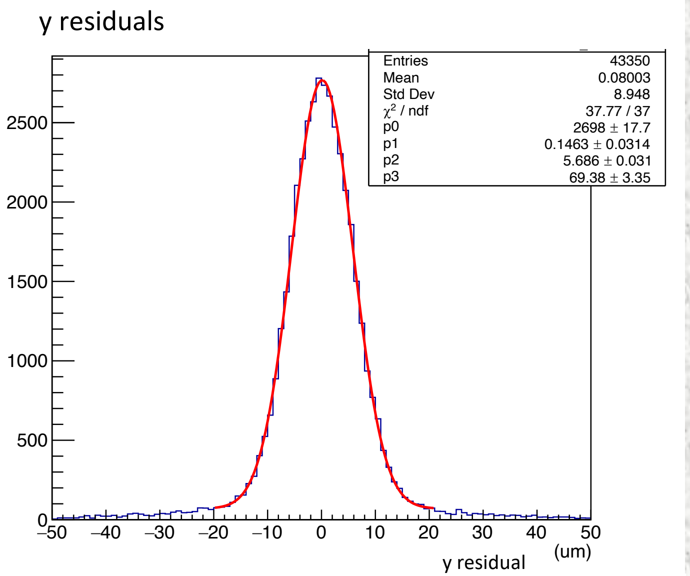
- FBK 3D silicon pixel detector for the CMS tracker phase 2 upgrade
- Active thickness 150 µm
- Pixel cell 50 x 50 µm^2
- bias voltage 20 V
- threshold 1200 e$^-$
- DUT tracks residuals distributions
- Hits on DUT with cluster size 2
- Track impact point computed using charge weighting
- RMS is 6.4 µm
- Subtracting in quadrature the mean values of the telescope errors (4.25 µm) the detector resolution results 4.7 µm

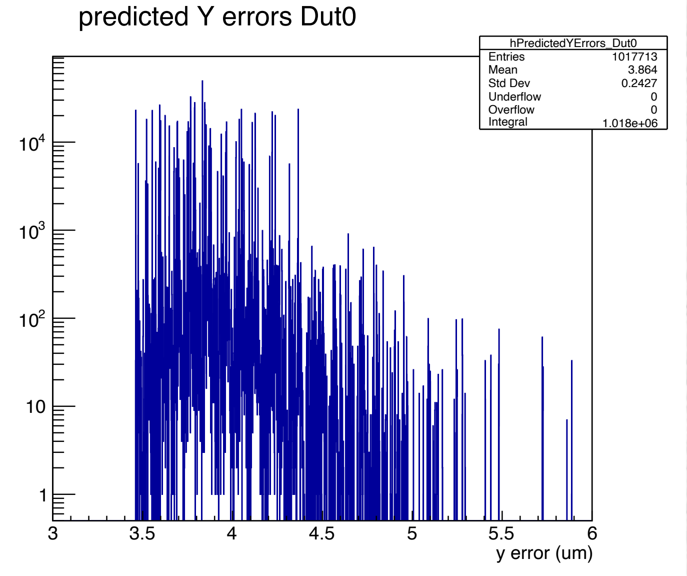




Checking the predicted errors - 2

- DUT tracks residuals distributions
- Hits on DUT with cluster size 2
- Track impact point computed using charge weighting
- RMS is 5.7 µm
- Subtracting in quadrature the mean values of the telescope errors (3.9 µm) the detector resolution results 4.2 µm
- The measured detector resolution is compatible with measurements carried out at other facilities





Conclusions

- The strip telescope of the FTBF have been successfully installed and commissioned in the second half of 2018
- A dedicated track reconstruction and alignment procedure, based on the Kalman filter approach, has been implemented
- The error on the track impact position at the DUT position has been measured to be ~ 4 μm

Acknowledgements

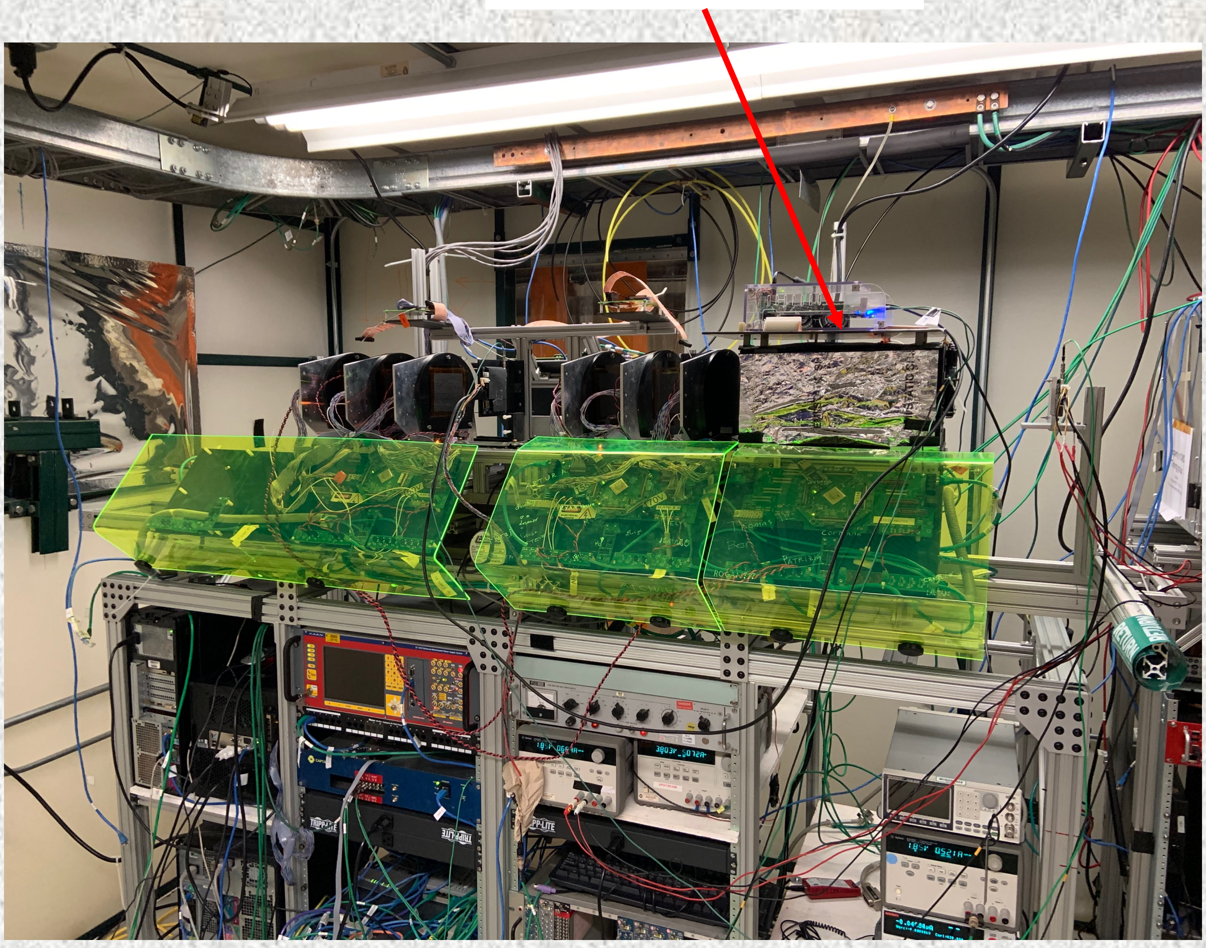
- Alan Prosser, Ryan Rivera and Lorenzo Uplegger (FNAL)
- Mauro Dinardo, Dario Menasce and Luigi Moroni (INFN Milano Bicocca)
- US-CMS TFPX team

Backup

Introduction - 2

- One of the stations of the pixel telescope previously installed is still present
- It is not used for track reconstruction but each reconstructed track is required to have an associated hit on one of these planes
- This is done to reduce the fake rate determined by the trigger-less readout of the strip planes

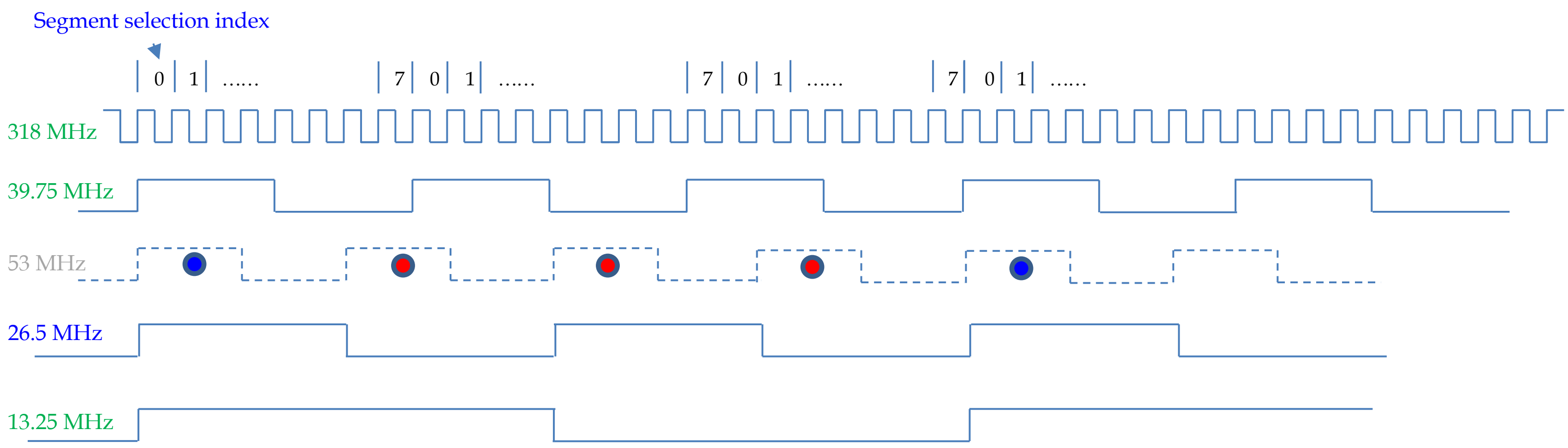
Pixel station



Telescope readout - 1

- The FSSR2 transmits all data that are above threshold
- Data are internally time-stamped in the chip with a running 8 bit counter (BCO)
- In order to correlate these data with a trigger, another counter, synchronous with the BCO counter of the FSSR, has been implemented in the CAPTAN FPGA. This counter is used to extend to 48 bits the native FSSR 8 bits counter but also to time-stamp the trigger coming from the scintillators.
- Since the trigger is always registered in the FPGA with a fixed delay, then we can correlate the particle arrival and FSSR BCO with the constant delayed trigger counter latched in the FPGA.

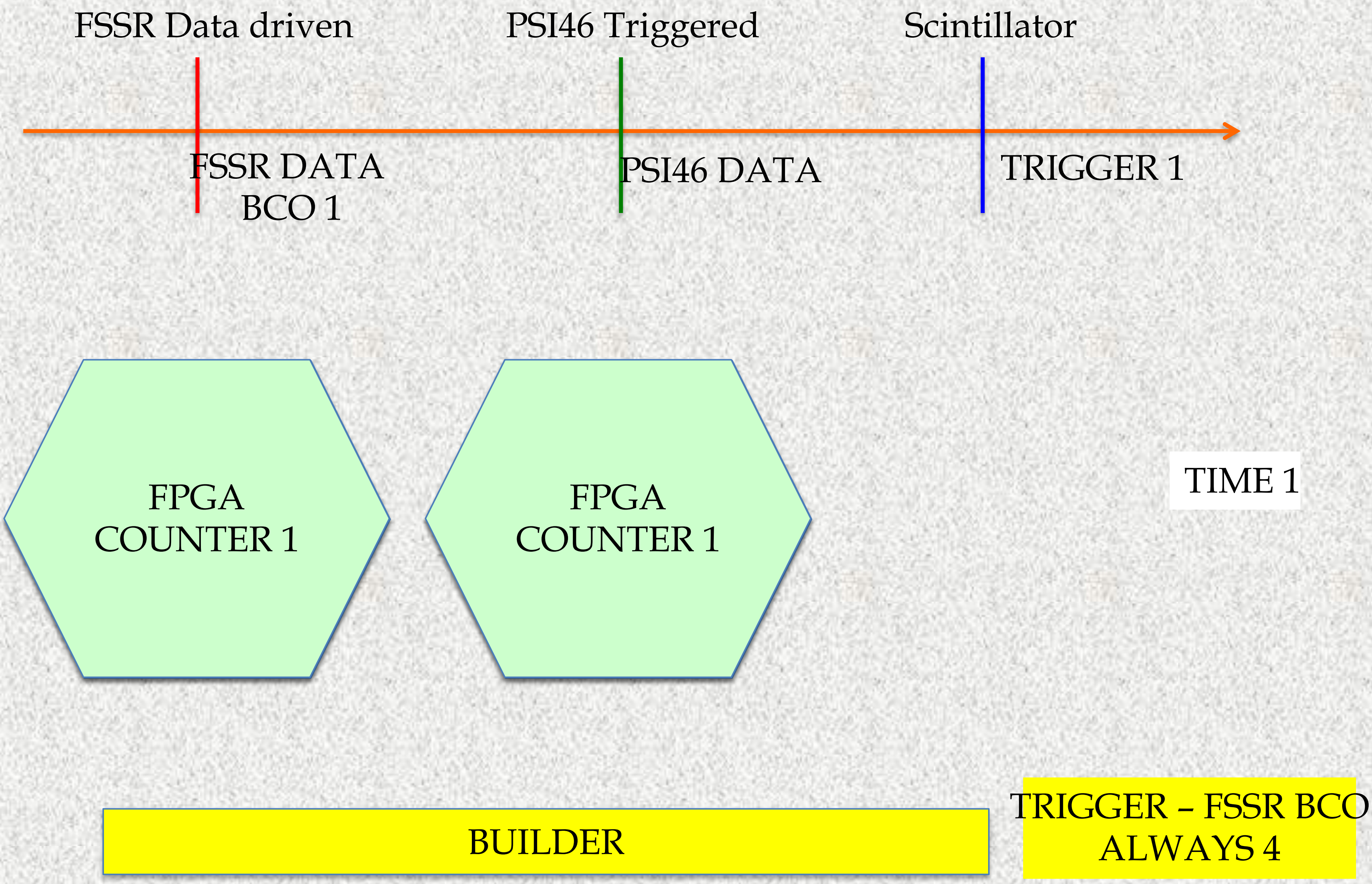
Clock distribution scheme



26.5 MHz: external clock

318 MHz, 39.75 MHz, and 13.25 MHz clocks are derived via MMCM from 26.5 MHz clock

Synchronizing a data driven ROC with a trigger



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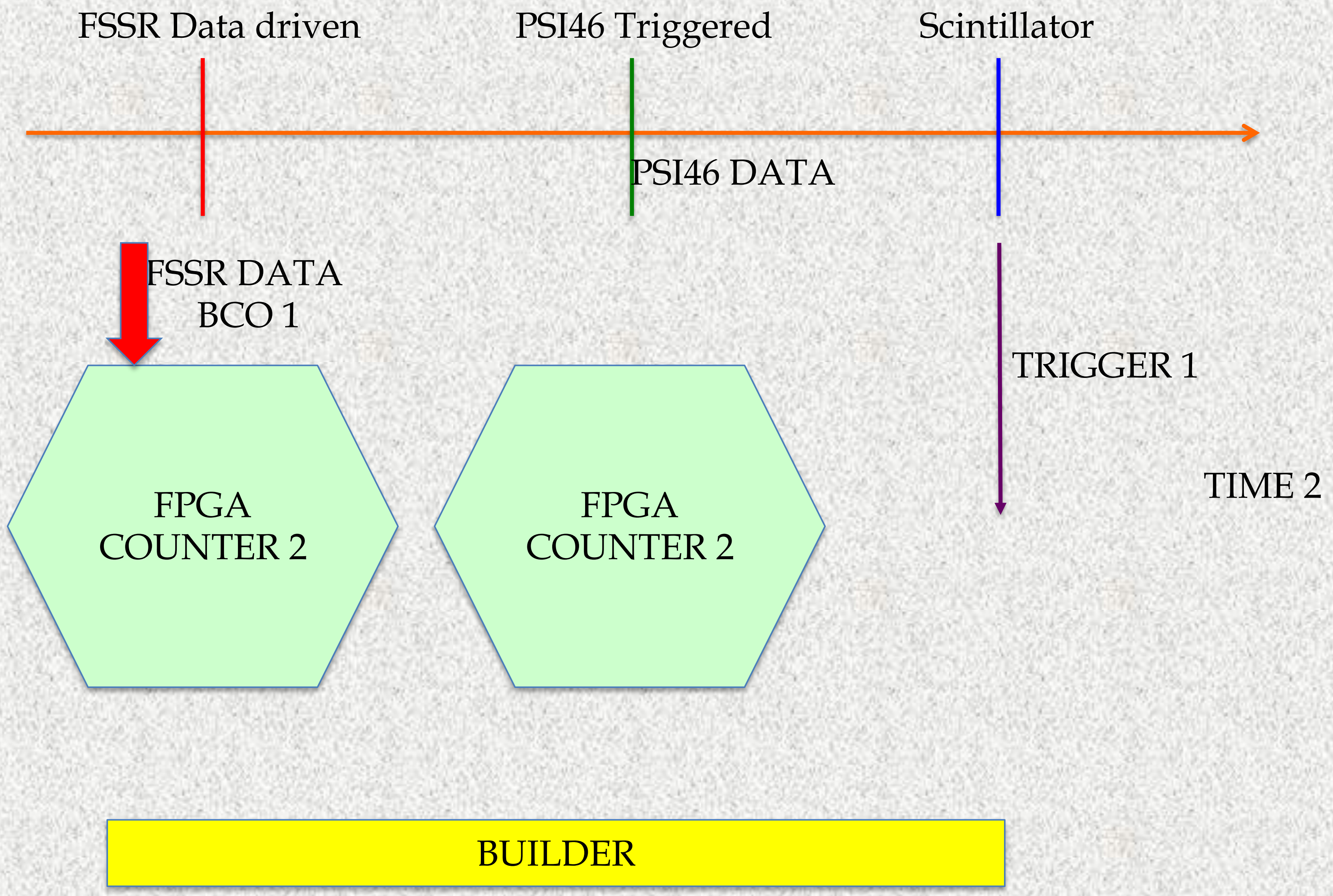

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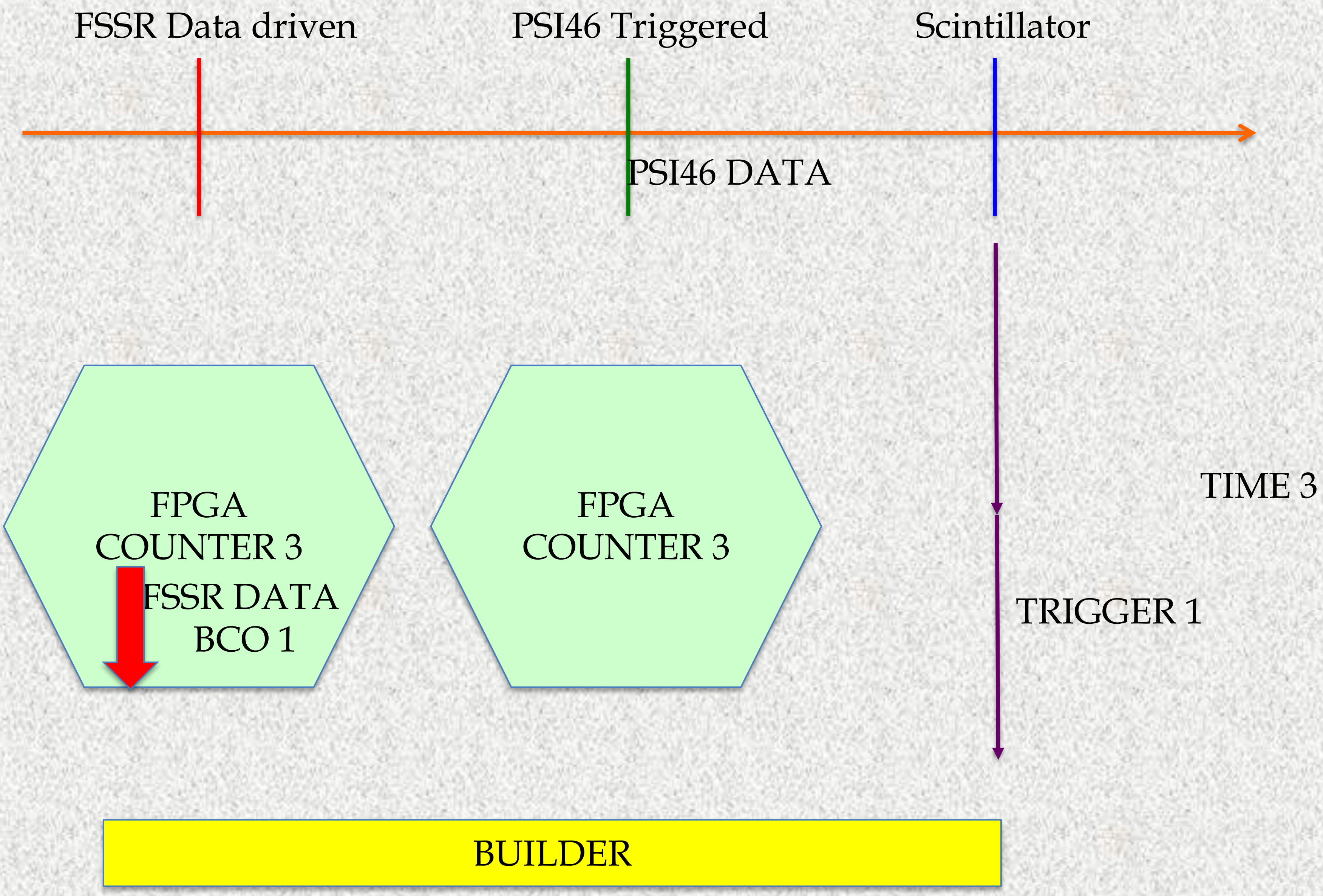

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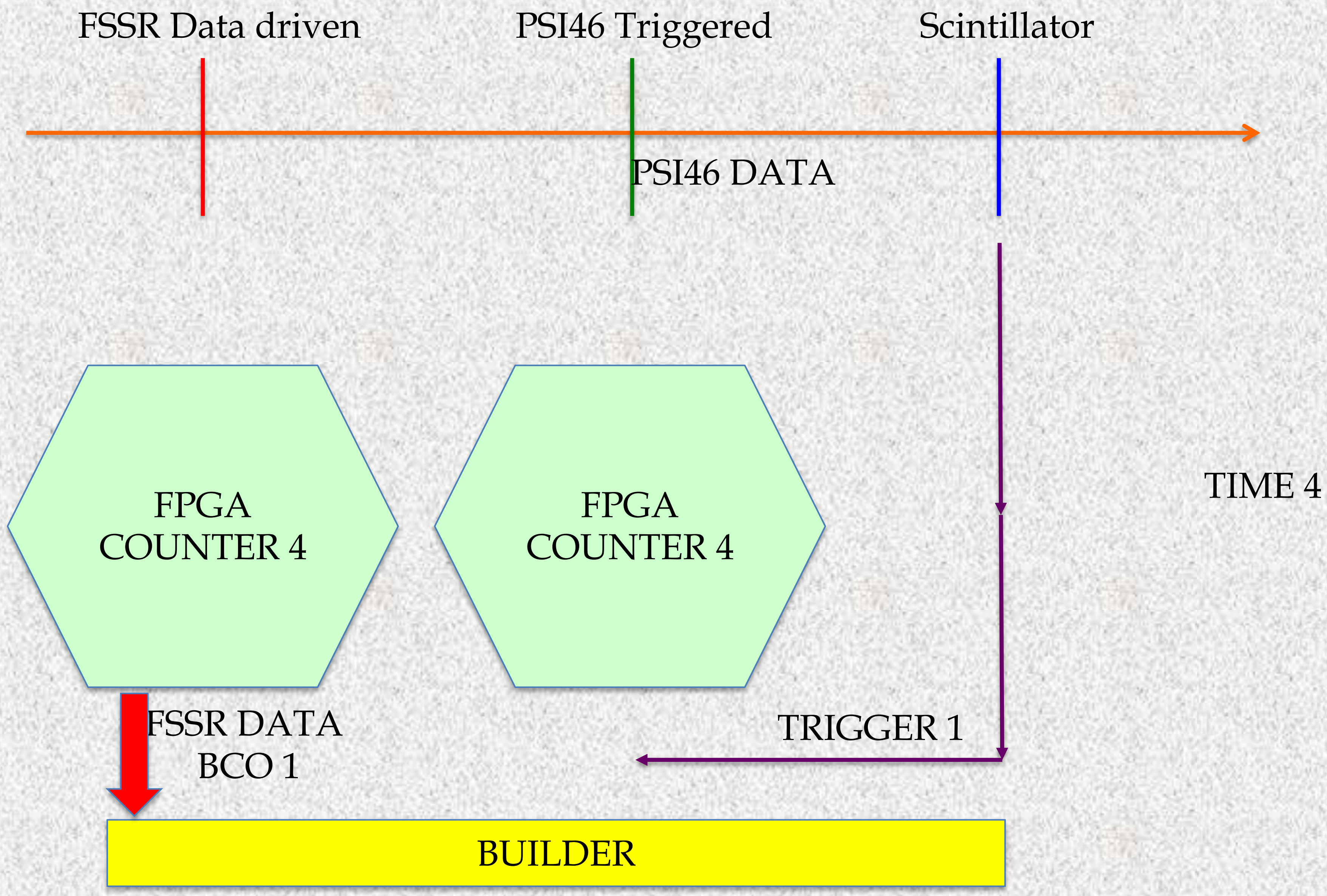
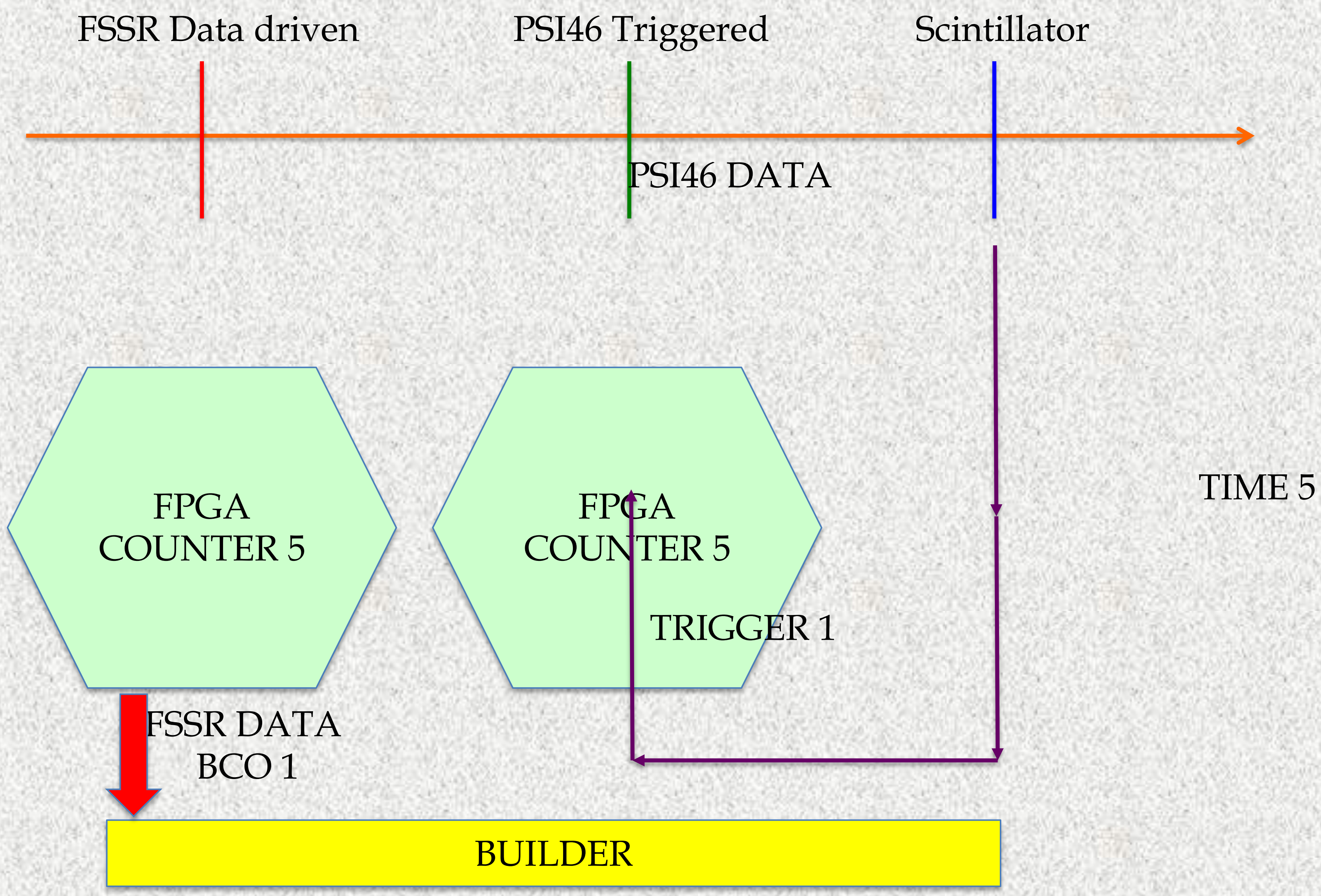
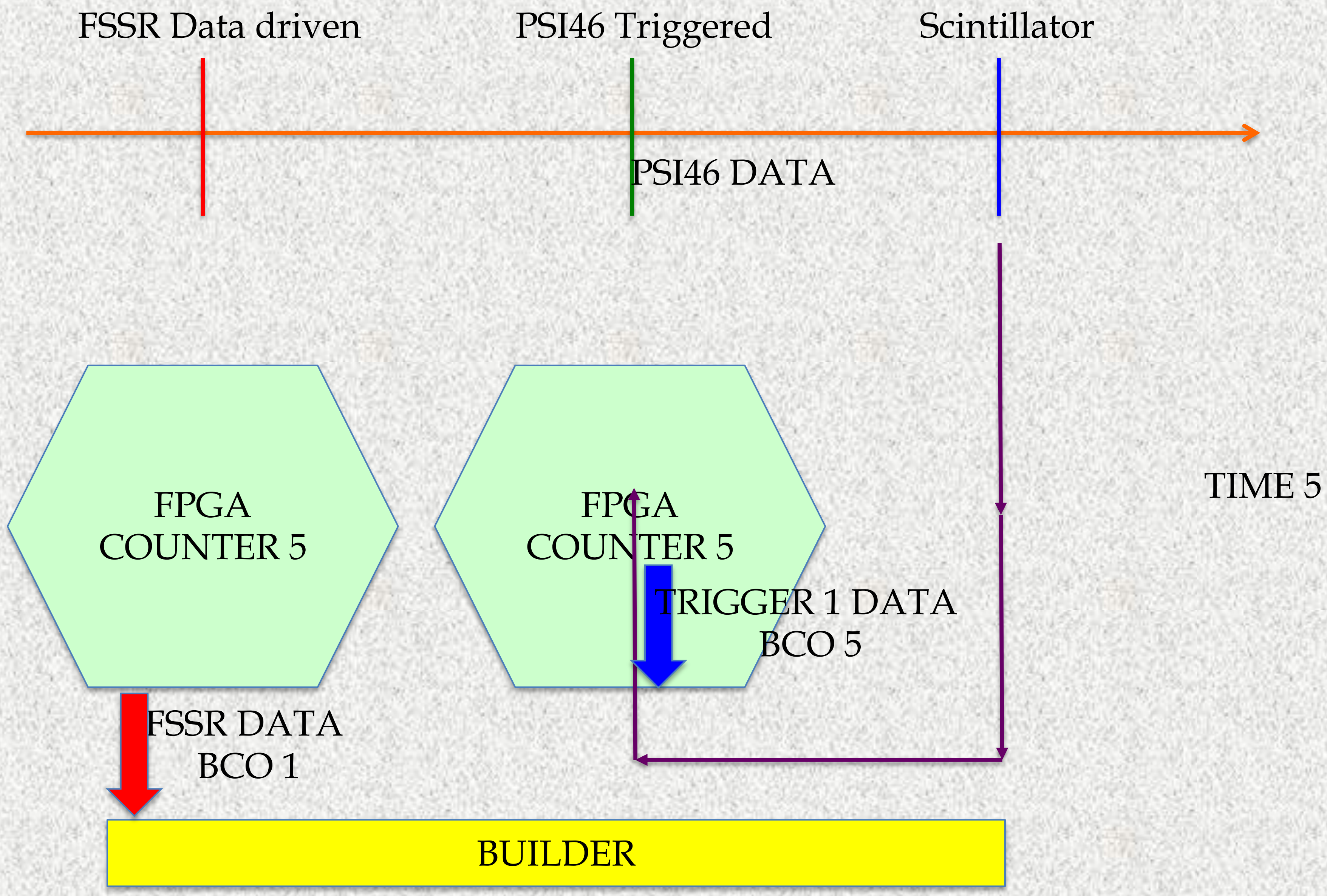


Synchronizing a data driven ROC with a trigger



Synchronizing a data driven ROC with a trigger



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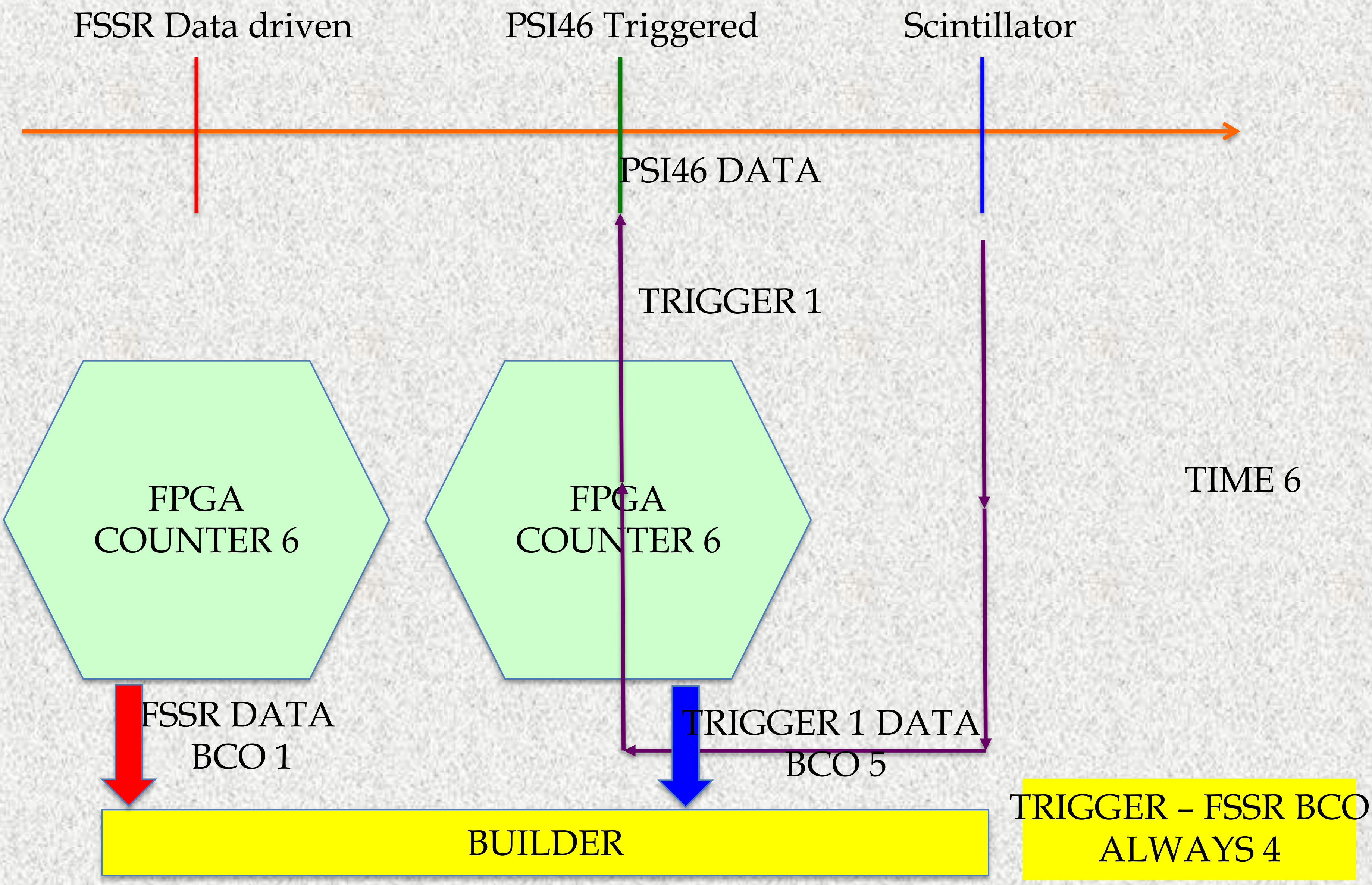

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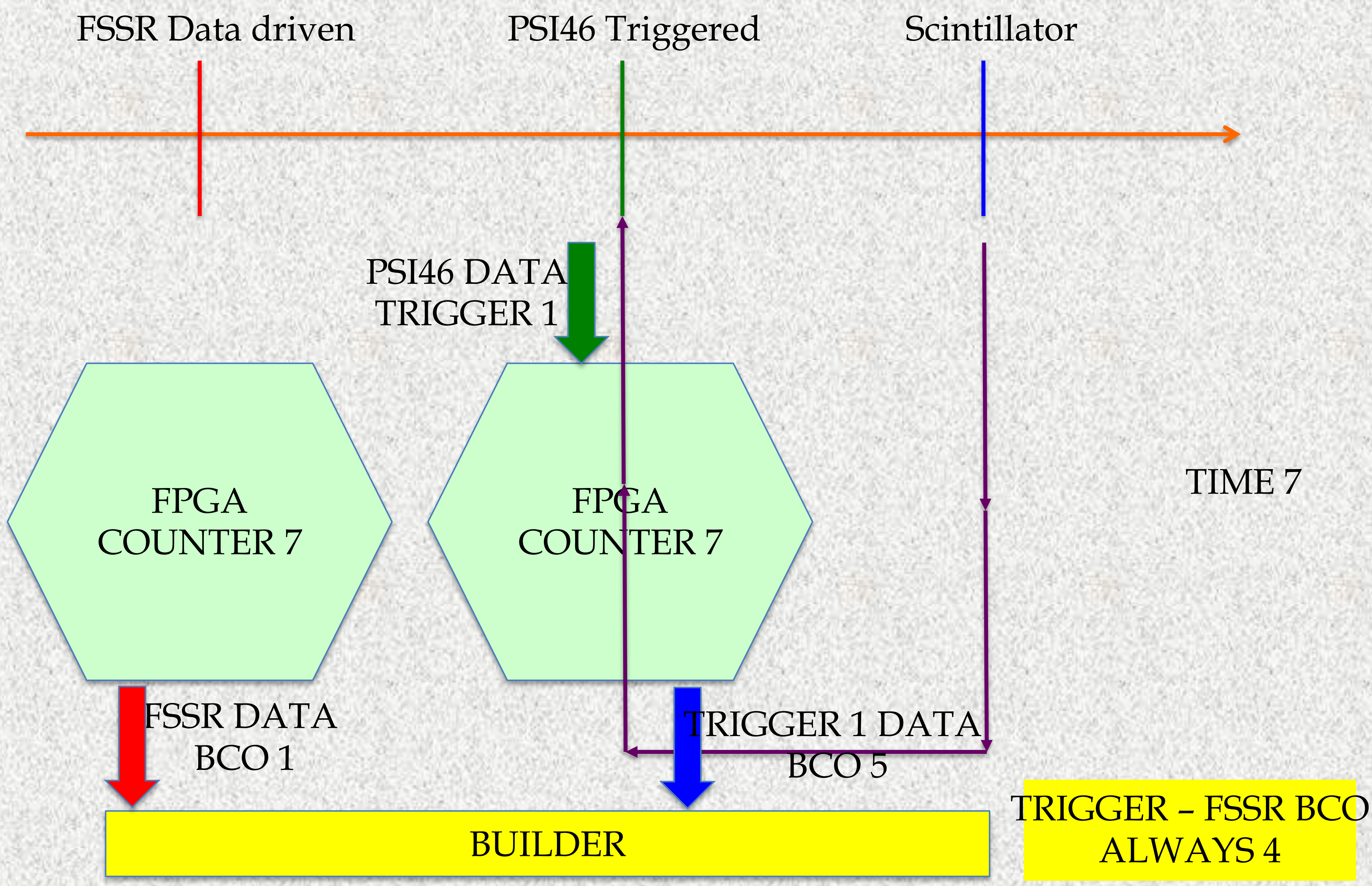

Synchronizing a data driven ROC with a trigger