Beam Tests of the CALICE AHCAL

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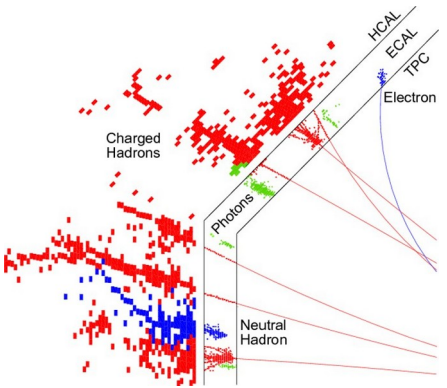
Content

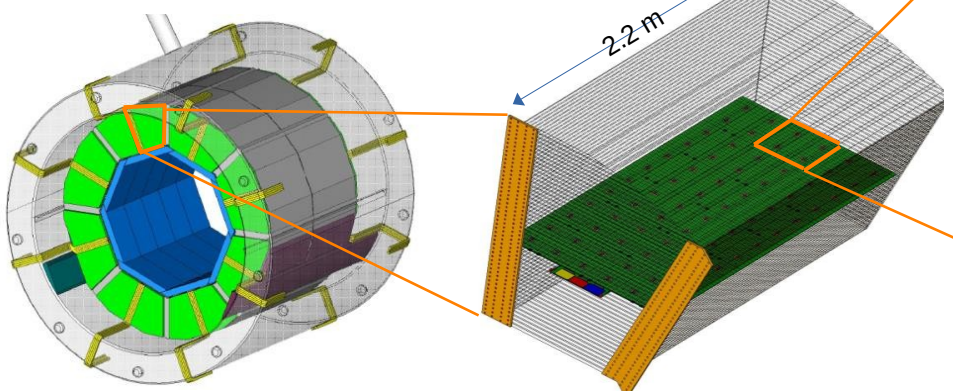
- AHCAL – imaging calorimetry introduction
- Testbeams 2020:
  - AHCAL with Alpide Telescope
  - “Megatile” scintillator project
  - KlauS readout ASIC
- AHCAL timing performance
- Testbeam 2020: Scintilator timing setup

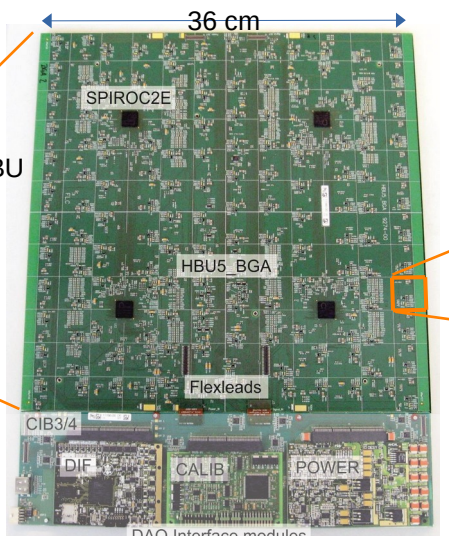
Covered by Lorenz

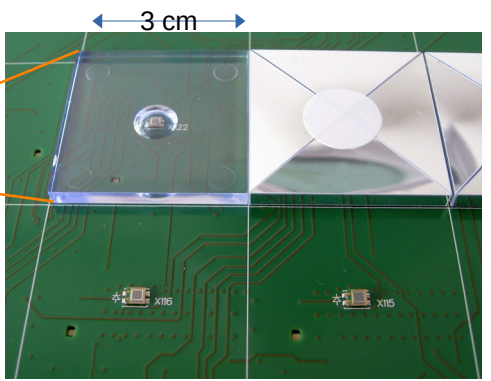
Introduction to AHCAL

- Analogue Hadron Calorimeter is one of the technology options for a calorimeter at a future **linear e+e- collider**
- Excellent jet energy resolution (3 – 4%) achieved via a **particle flow** algorithms
  - Very **high granularity** required for separation of overlapping showers
- Small 30x30x3 mm³ **scintillator tiles** with **individual SiPMs**
  → **8M channels** (barrel+endcap)
- Challenges:
  - No active cooling inside of the absorber → need <25 uW / channel
  - Electronics inside 4T magnetic field
  - Mass-production feasibility



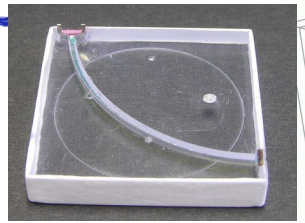


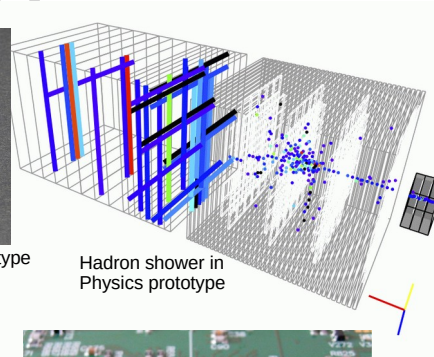


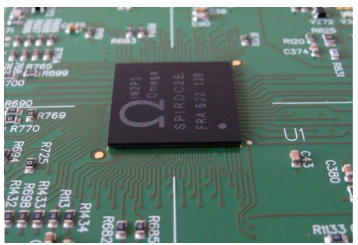


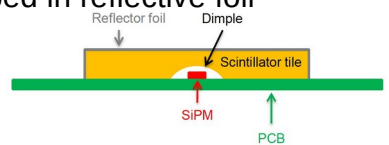
AHCAL detector evolution

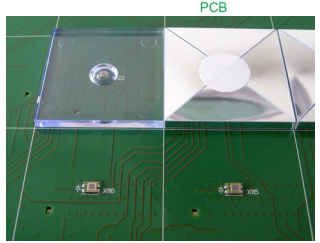
- "Physics prototype", tested @CERN and @FNAL (2006-2012)
  - First **large-scale use of SiPMs**: 7608 channels, various scintillator sizes (3x3, 6x6x 12x12)
  - SiMP coupled to a WLS fibre inside the scintillator tile
  - **physics demonstration** of the high granular calorimeter
- Technological prototype with **embedded front-end electronics** ("SPIROC" ASIC) under tests since 2010
  - Also demonstrated the scalability of the base modules (HBU) to form large modules (up to 2m in length)
- 2018: construction of a **large scale technological prototype** with **22000 channels**
  - **Mass production**: automated assembly, QA of ASICs & SiPMs, module commissioning & calibration
    → Demonstration of feasibility to construct a multi-million-channel detector
  - SMD SiPMs from HPK used (S13360-1325PE), **Scintillator tile with a dome**, wrapped in reflective foil (automated manufacturing).
  - New DAQ HW, DQM, online monitoring, EUDAQ integration
  - Broad physics program @CERN SPS testbeam 2018, ongoing analyses
- **AHCAL Tests in 2020** @DESY testbeam:
  - "**Megatile**" scintillator (Combined running: AIDA-TLU + **Alpide telescope**)
  - "**KlauS**" very front-end readout chip as an alternative to SPIROC ASIC
  - **CMS HGCAL** Tile-board (previous talk)
  - **Tile Timing** studies (second part of this talk by Lorenz)

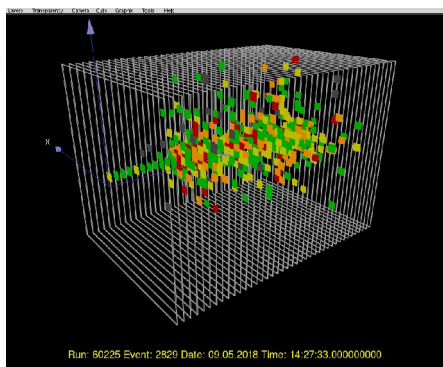

SiPM+WLS Scint. Tile, Physics prototype


Hadron shower in Physics prototype


Integrated front-end ASIC: SPIROC2E



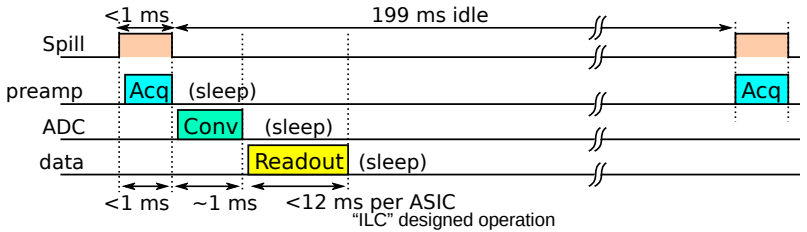

SMD SiPM, Scint. Tile 3x3cm³
"naked" and wrapped in reflective foil



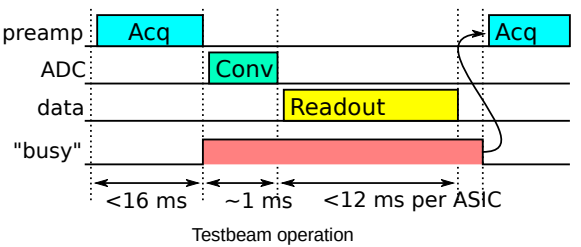
Hadron shower in the Engineering prototype, 2018

AHCAL prototype operation (intro)

- Designed for **very low duty cycle** of ILC machine
  - <1 ms spill followed by 199 ms idle
  - Bunch Crossing (collisions) within acquisition every few hundreds of ns
  - Separate power for Acquisition, Conversion and Readout stages
    → significant reduction of power & **heat dissipation**
- The SPIROC ASIC has 16-events deep **analogue memory cells**,
  - store the signal amplitude (High & Low gain) + TDC value for all channels
  - 1728 capacitors!
  - Converted after acquisition



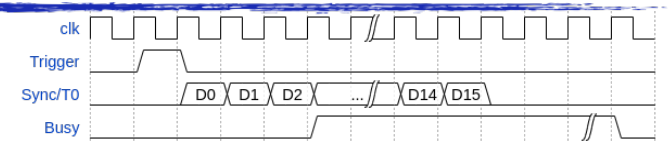
- Hits are **self-triggered** (discrimination typically at the level of several single-photo-electrons) → Hits are **not** triggered externally
  - Event *validation (*everything not validated is rejected*)* is possible order to reduce the noise occupancy
    → not needed and not used since 2018 due to **very low-noise SiPMs** (typical 0.1-0.2 Hz / Tile, incl. cosmics)
- ILC timing is **inefficient** with CERN/DESY Beams → need some tricks for TB
  - Acquisition phase is prolonged to 16 ms
  - Acquisition phase is stopped earlier if any asic fills its all memory cells (propagation via “busy” signal)
  - Wait until all modules are done with readout, then restart immediately

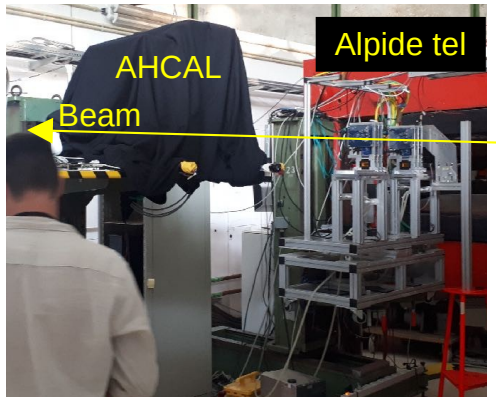


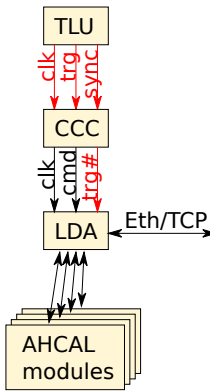
- Acquisition rate strongly depends on particle type, hit occupancy and beam rate
  - Typical achieved data taking rate in TB mode is **hundreds evt/s** (100-800 evt/s)
  - Maximum acquisition duty cycle in TB mode: **90%** (cosmics)
- Effort put into **combined data-taking** and hardware/software synchronisation with other detectors
  - Calice ECAL, Mimosa Telescope, eudet-TLU, AIDA-TLU, CMS-HGCAL, mini-TLU
  - Intrinsically, events are addressed by an Acquisition cycle & BXID
    → External timestamping and trigger counting implemented in the DAQ concentrator card (“LDA”)

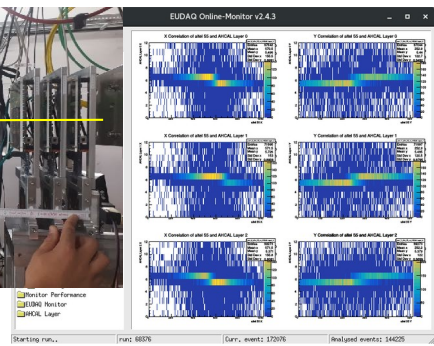
TB 2020: Alpide + AIDA-TLU

- Unusual setup: DUT is 1 m behind the Telescope
  - Track extrapolation accuracy not critical: aiming for 0.1 ~ 1 mm
  - Additional material in the path (black cloth cover, steel cassette)
- Past experience with Alpide telescope in **2019** – EUDET TLU synchronization & counting of triggers → **occasional de-synchronization problem**
- Alpide telescope implemented a “sync” mode of AIDA-TLU (trigger number sent along the clock from TLU)
- **New**: AHCAL DAQ implemented the same scheme, though still running on independent 40 MHz clock
- With great help from Yi Liu, all hardware and software problem solved
  → enjoyed remaining **2 days of stable combined running**
- New way of building Alpide software (including EUDAQ producer): built outside of the EUDAQ repository – very convenient
- (small) problems:
  - TLU clock signal stops during init/configuration
    → clock not internally usable by AHCAL CCC
  - TLU/telescope trigger efficiency and scalers not well understood (due to new PMTs?)
  - Bit shifts in trigger number seen in LDA (35 times) – AHCAL DAQ firmware bug?
    - Not an issue - Immediately recovers and re-synchronizes with new trigger number



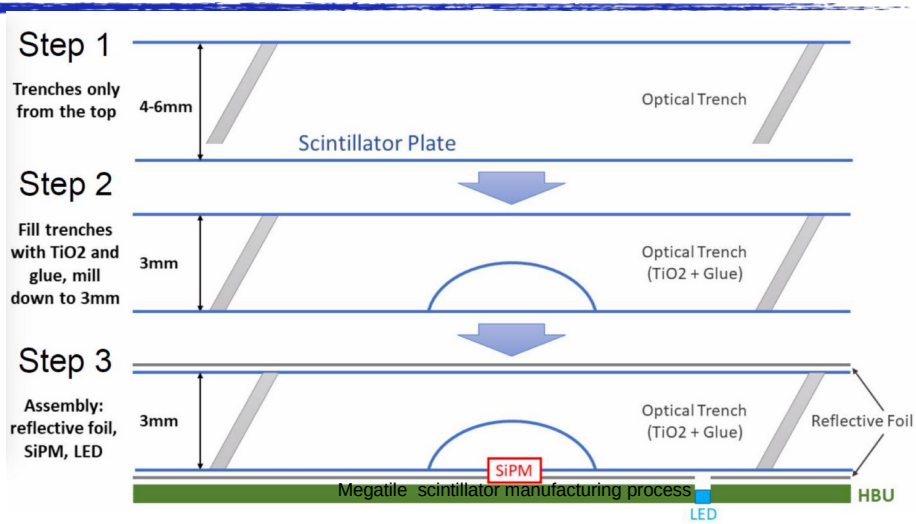


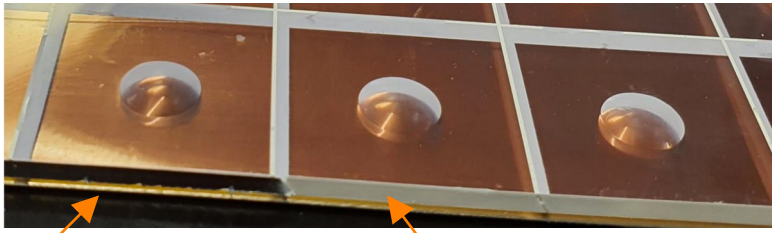




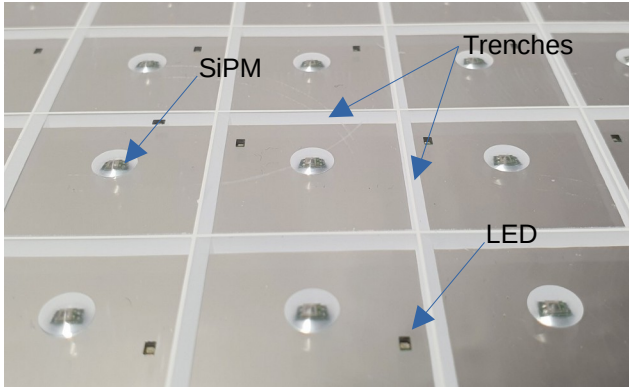
DESY TB 08/2020: Megatile

- Evolving design @Uni Mainz
- One piece of scintillator 36x36 cm^2 with **trenches**
  - Trenches filled with reflective glue with TiO_2 – separation of channels
  - Tilted trenches (30°) → Small dead area
  - Reflective foil on HBU (with laser-cut holes)
    - Air gap can create crosstalk (simulated 3.5% for 100 µm)
- **Simplification** of manufacturing and assembly
- **Compatible** with the current tile-on-SiPM design
- New type of **edge coating**: white varnish
- Tests performed with 1 Megatile HBU and 2 reference HBUs
- **Measurements** done:
  - Light yield (automated scan using DESY table)
  - Uniformity scan (Alpide telescope & DESY table)
  - Crosstalk (with W absorber)





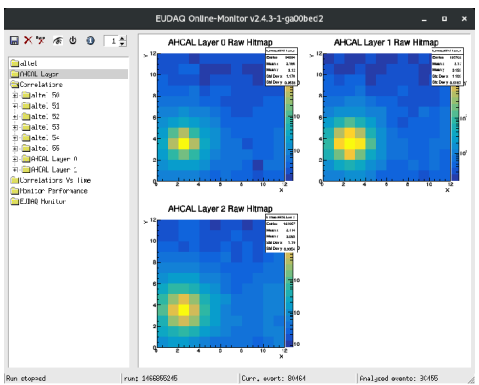

Megatile on HBU (36x36 cm^2)



Megatile very preliminary results

- **Light yield** rather uniform in the center (~32 p.e. in the center), confirmed in the beam
  - Edges with reflective foil: 30% lower (Lab measurement 2019)
  - Edges with **white varnish**: only **~10% lower** (preliminary, not fully analyzed yet)
  - Ongoing analysis!
  - Edge Light yield remains a challenge
- **Cross-talk**:
  - Expected: 3.5% with air gap of 100 µm. ~5% measured in cosmic test stand @Mainz
  - 2019: up to 15% observed & non-uniform – possibly due to **increase of the air gap** between megatile and reflective foil
    → Has been addressed in this TB by **gluing of the foil** above the trenches
  - Ongoing analysis
- **Tile uniformity** fine scan in 4x6 cm regions: 600 measurements in 2 mm steps, 5k events per position
  - Ongoing analysis

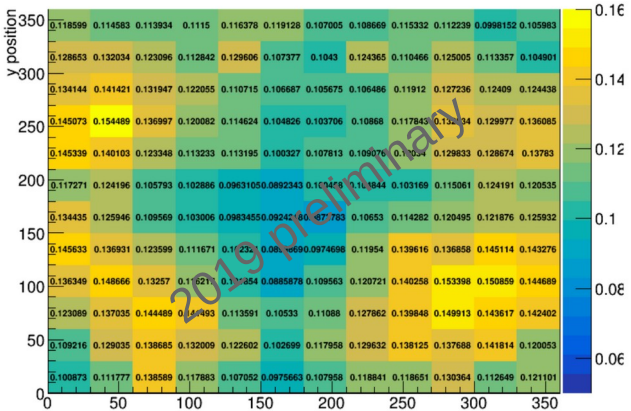
Light yield in the LAB (reflective adhesive edges)



AHCAL Hitmap, run W absorgers


HCAL layer in “air” stack

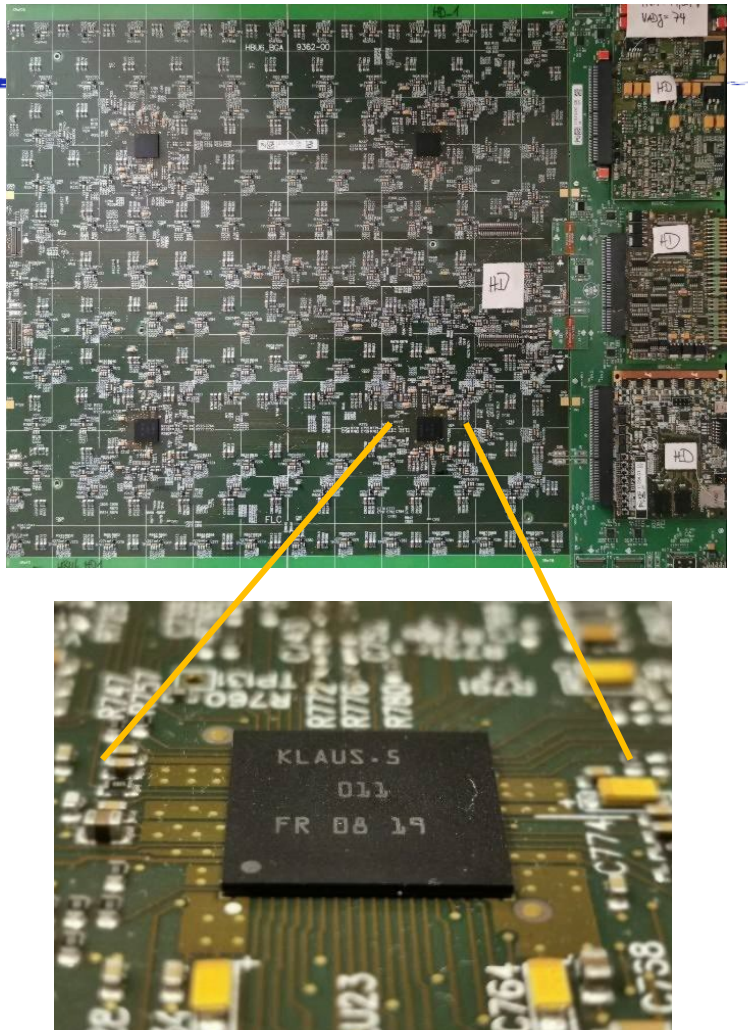

W absorbers



2019 measurements: Cross-talk - up to 15%

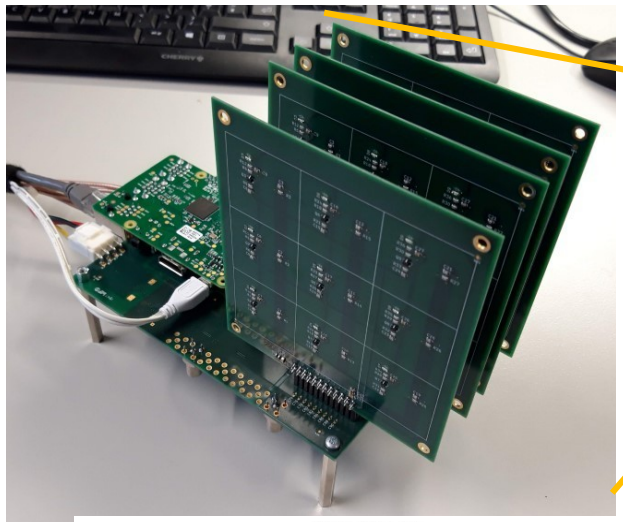
KLauS

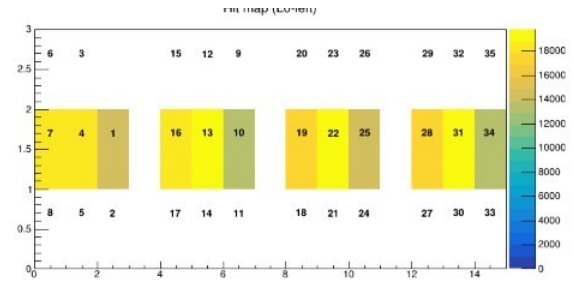
- Parallel development of Readout ASIC @KIP – Uni Heidelberg
  - Alternative design of the readout ASIC
  - evolved in **fully functional readout chip** with 36 channels, 12-bit ADC and PLL-based TDC with **200 ps bins**
  - Can operate in “ILC” spilled mode (similar to SPIROC)
  - **Can run continuously**
- New **HBU with KLauS-5** ASIC
  - same form factor, connectors and DAQ interfaces
  - Aim is to keep the compatibility with “SPIROC” HBU
  - Different configuration and readout (I2C)
  - different DIF FW modified (@KIP)
  - Status: USB readout established in the LAB
- Full DAQ integration (HDMI readout) pending(@KIP,Prague)
- Testbeam with **KlauS-6** on **Testboard**

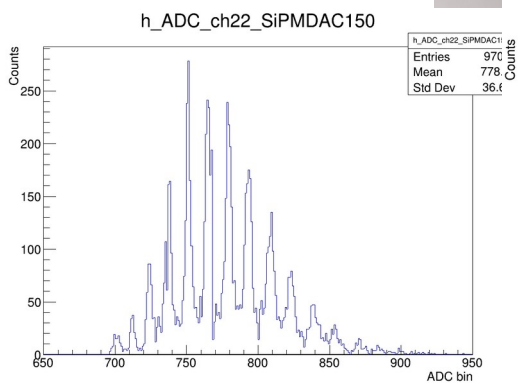


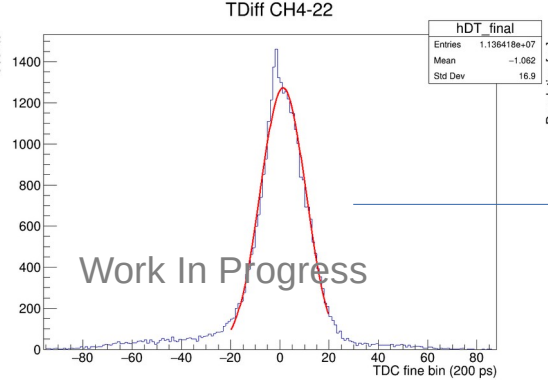
KlauS-6 in Testbeam

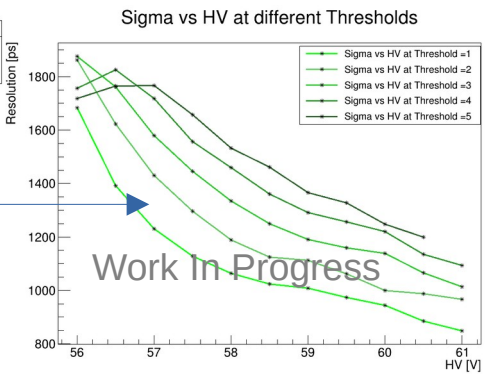
- 12 equipped channels (out of 36), 4 layers
- Two types of SiPMs (15, 25 µm)
- Goal: validation of chip in the beam
  - Found bad filter capacitor → Fixed
  - Single p.e. comparable to previous KlauS generations (after fix)
- Measure the timing performance between two layers
  - Full chain Scintillator+SiPM+Frontend/TDC: up to 1 ns resolution (VERY preliminary)
    - Varies will SiPM over-voltage and threshold
  - Lab reference measurement with LED (w/o scint.) < 100 ps
- Issue identified in the digital part → fixed for the next revision KlauS-6b









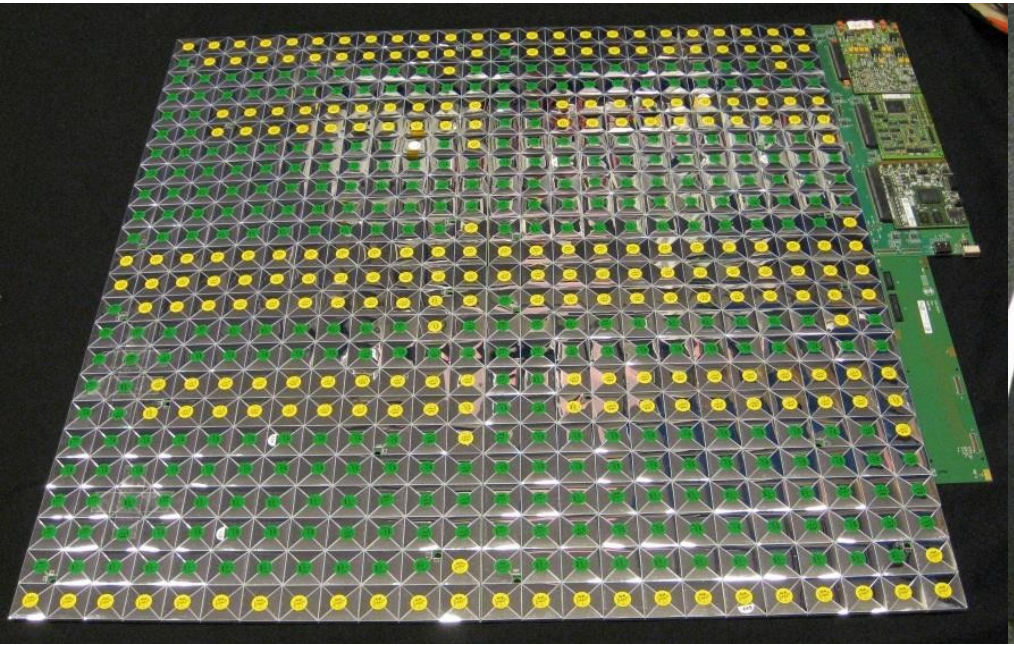


(Intermediate) Summary & plans

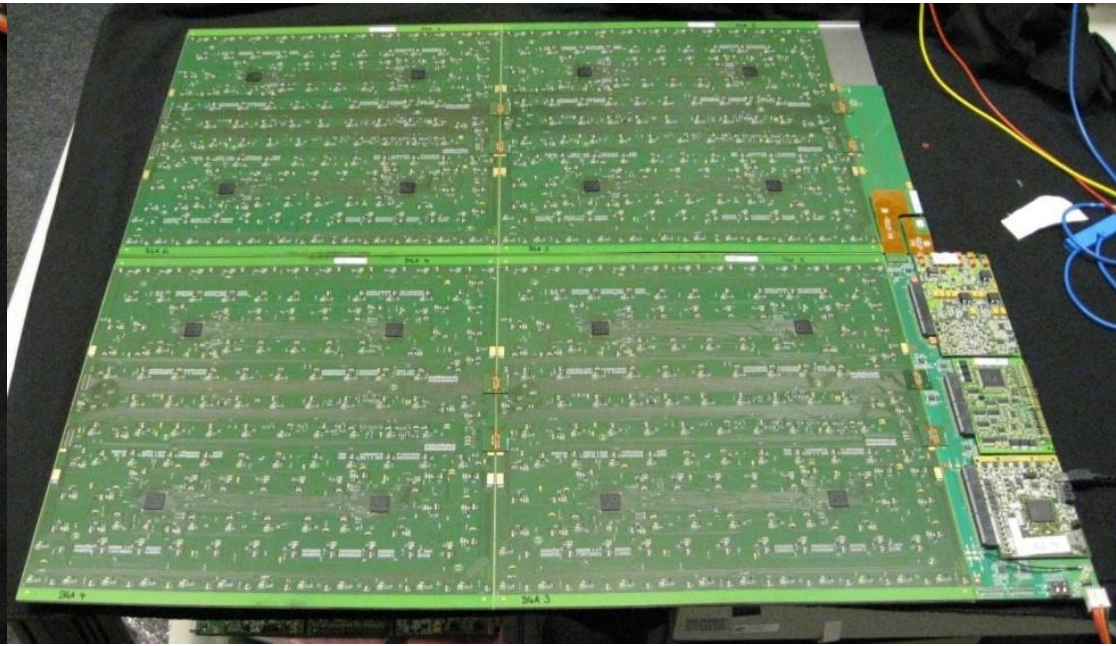
- Reduced, but fruitful testbeams @DESY 2020
- Good push in the Megatile performance study
  - Improvements already done, waiting for analysis results (and another test)
- New version of KLauS readout chip tested in the beam
  - Chip performs well (detailed analysis still ongoing)
  - Some minor bugs fixed/identified
- The large AHCAL prototype waiting for the opportunity to show its performance again
- Next plans:
  - Combined running with the SiECAL (@DESY first, ultimately @CERN)
  - Combined beam with the fully assembled KlauS-HBU (still needs DAQ integration)

Backup slides

AHCAL 2x2 (72x72 cm^2) module



Bottom (Scintillator tiles)



Electronics side

AHCAL cross-section