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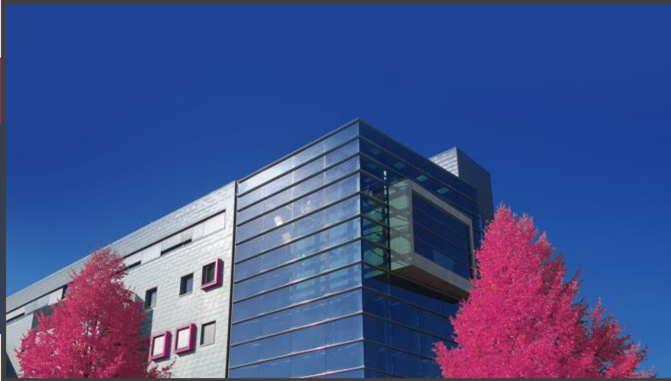


08.02.2021

9th Beam Telescopes and Test Beams Workshop

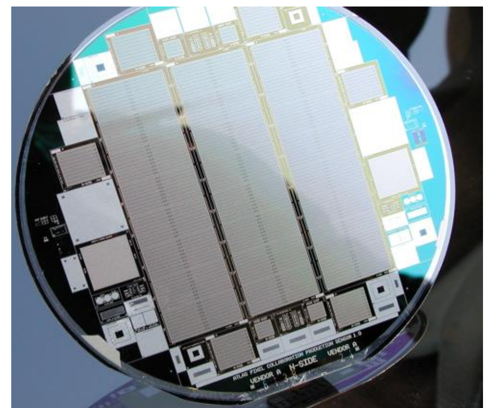
- ONLINE -

Silicon Processing Techniques

Thomas Ortlepp, Tobias Wittig

Outline

- 1. Overview of micro systems technologies
- 2. How to process a planar radiation detector - step by step
- 3. Special cases of radiation detectors



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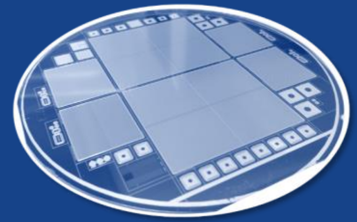
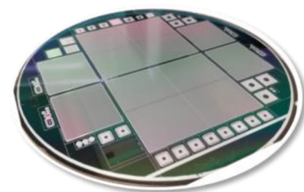


1. Introduction and basics of micro systems technologies

Silicon Processing Techniques | BTTB9 | online | 08.02.2021 | T.Ortlepp, T.Wittig

Micro systems technologies
Introduction

- technology for (Si) wafer fabrication
- applications:
  - CMOS electronic industry (ICs)
  - Micro-Electro-Mechanical Systems (MEMS)
  - Micro-Opto-Electro-Mechanical Systems (MOEMS)
  - radiation/particle detectors



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Wafer processing

- projection lithography
- high temperature processes
- ion implantation
- spray-coating for 3D
- RIE-, ICP- and Plasma etch
- wet-bench
- LP/PE-CVD
- magnetron sputtering
- Si-fusion bonding
- front and backside processing

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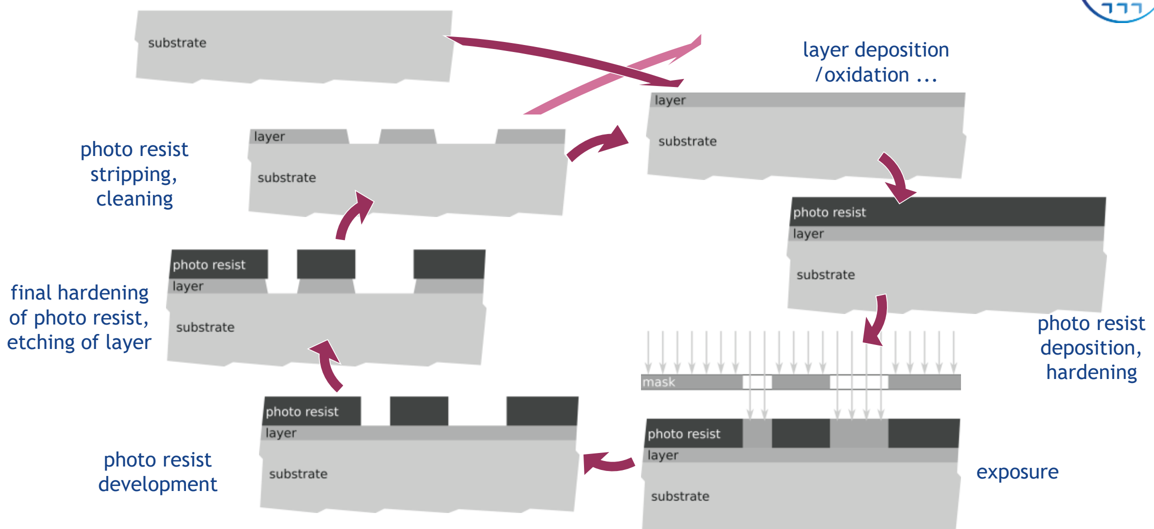
Micro systems technologies
Basics



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Micro systems technologies

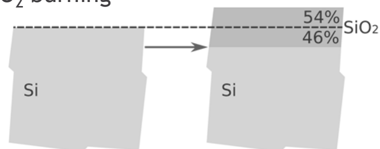
Basics

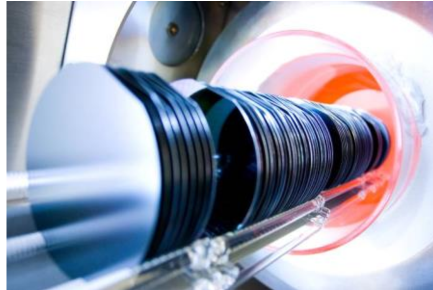
THERMAL OXIDATION

- no deposition of SiO_2
- Si is oxidized
  - part of the surface Si is consumed

DIFFERENT TYPES

- dry → slow, good quality
- wet (H_2O) → fast, poor quality
- H_2O_2 burning





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Micro systems technologies

Basics

CHEMICAL VAPOR DEPOSITION (CVD)

- deposition from gas phase
- e.g. Si_3N_4, SiO_2, poly-Si

low pressure CVD (LP-CVD)

- at 500-1000°C

plasma enhanced CVD (PE-CVD)

- at 200-500°C
- e.g. for final passivation when metal is already present

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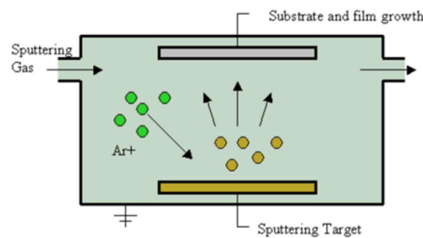
Micro systems technologies
basics

METAL DEPOSITION

EVAPORATION

- in vacuum
- material heated and evaporates to condense on the substrate



SPUTTER DEPOSITION

- ions from sputtering gas (e.g. Ar) are accelerated to sputtering target
- material from the target is ejected to the substrate
- even materials with very high melting points are easily sputtered
- better step coverage than evaporation

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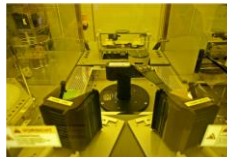
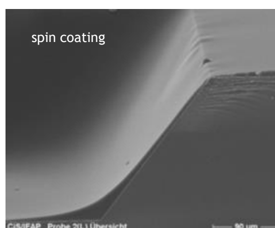
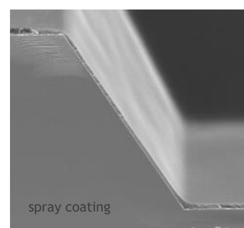
Micro systems technologies
basics

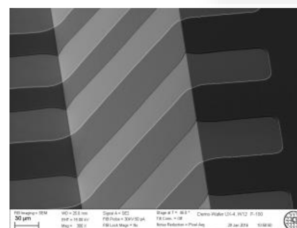
PHOTO LITHOGRAPHY

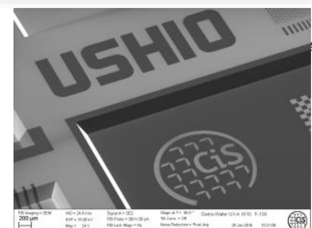
- **photo resist deposition:**
  - spin coating (standard)
  - spray coating for better 3D conformity











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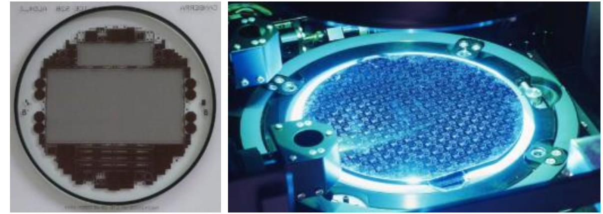
Micro systems technologies
basics

PHOTO LITHOGRAPHY

- **exposure:**
  - optical (UV i-line)
  - 1:1 projection
  - reticles for stepping method
    5:1, 10:1 masks



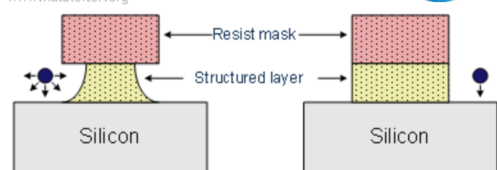
- **direct writing**
  - **laser beam**
    highly flexible, no mask
  - **electron beam**
    higher resolution, no masks

Micro systems technologies
basics

WET ETCHING

- wafers are dipped into chemical bath
- certain layers are chemically etched
  - mostly isotropic
  - high selectivity between different materials
  - silicon: e.g. with KOH, anisotropic etching of <100> and <110> chrystal planes
  - Si_3N_4, SiO_2
  - metal
- wafer cleaning afterwards for etchant removal

www.halbleiter.org



Isotropic etch process,
particles move in each direction:
Under etch of the resist mask,
high selectivity

Anisotropic etch process,
perpendicular orientated:
Exact transfer of the resist mask,
low selectivity

Micro systems technologies
basics

DRY ETCHING - three kinds

- **physical:**

→ e.g. ion beam etching

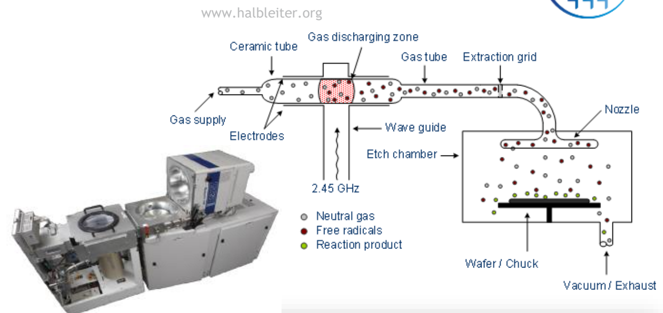
- **chemical(CDE):**

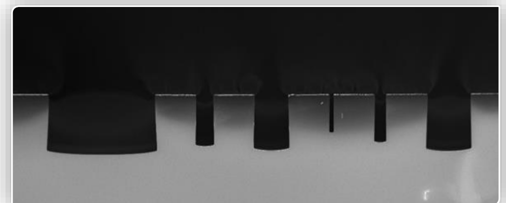
→ e.g. plasma etching
  - etching by neutral radicals (e.g. F)
  - isotropic

- **chemical & physical:**

→ e.g. reactive ion etching (RIE)
  - etching characteristic (selectivity, etch profile, etch rate, uniformity ...) can be controlled very precisely

→ deep RIE (DRIE):
  - alternating process of RIE and passivation
  - aim is a maximum anisotropic etching process
  - aspect ratios of ~50:1 possible





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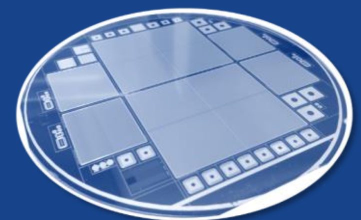
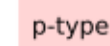
2. How to process a radiation detector



How to process a silicon radiation detector
Step 1: *p-type Si wafer substrate*

- starting with a p-type Si wafer substrate
- thickness ~250...300...500 µm
- high resistivity: ~1...10 kΩcm



How to process a silicon radiation detector
Step 2: *thermal oxidation*

- starting with a thermal oxidation
  - ~100...300 nm
  - preferably dry oxidation (HCl)
  - better quality
  - for larger thicknesses: wet oxidation or H_2O_2 is used
- photolithography of the alignment marks
- etching alignment marks into oxide and silicon

oxide

oxide

oxide

oxide

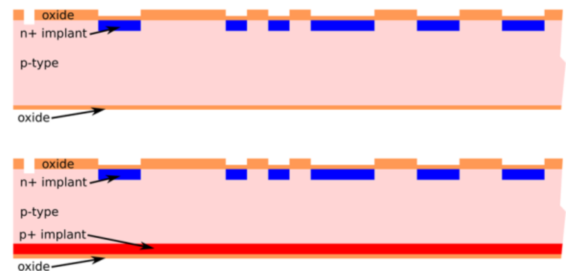
How to process a silicon radiation detector
Step 3: *n+ implantation layer*

- photolithography for the implantation layer
- optionally thinning oxide to preferred target thickness (scattering oxide)

- implantation of n-type (Phosphorus) ions

How to process a silicon radiation detector
Step 4: *p+ implantation layer*

- optionally thinning back side oxide to preferred target thickness

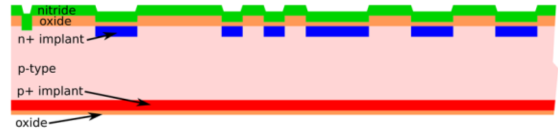


- implantation of p-type (Boron) ions
- annealing in N_2 atmosphere for activation of the doped ions

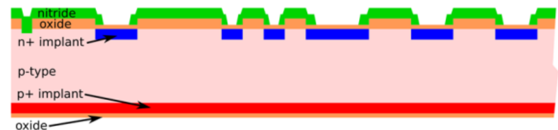
How to process a silicon radiation detector

Step 5: *photolithography for nitride layer*

- optionally nitride deposition on front side (e.g. LPCVD Si_3N_4)



- photolithography for the nitride layer
- wet etching nitride
- optionally p-spray or p-stop implantation possible



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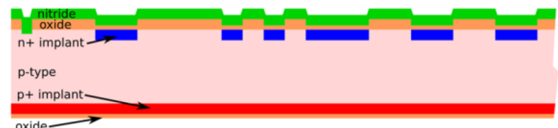
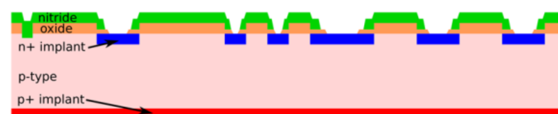
How to process a silicon radiation detector

Step 6: *photolithography for oxide layer*



- photolithography for the oxide layer
- wet etching oxide (contact openings)



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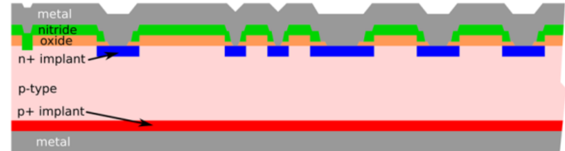
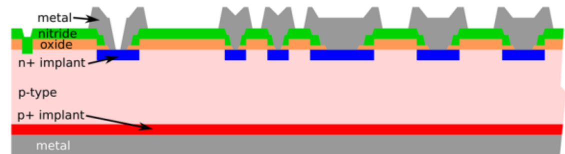
How to process a silicon radiation detector

Step 7: *metal deposition & wet etching*

- metal deposition on front and back side (e.g. sputtering)
- thicknesses ~ 500...1500 nm



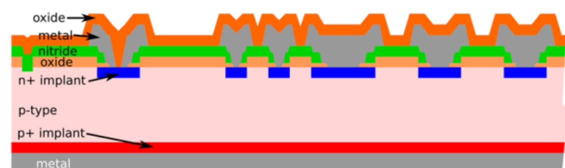
- photolithography for the front side metal
- wet etching of front side metal



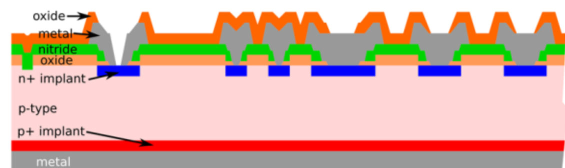
How to process a silicon radiation detector

Step 8: *final passivation*

- deposition of oxide or nitride (e.g. PECVD)

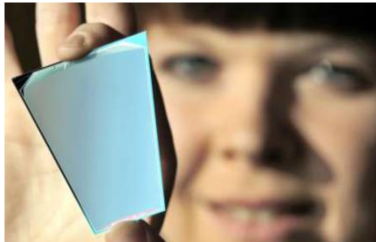


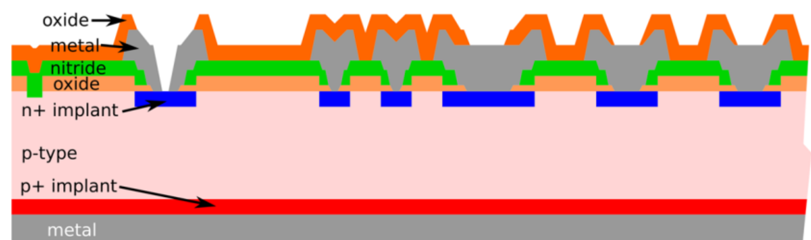
- photolithography for the final passivation
- etching of final passivation (wet or plasma)



How to process a silicon radiation detector

Finally: this is how it should look like





EXAMPLE: single sided, planar pixel sensor, n-in-p
(only relevant steps were shown: no cleaning, photo resist stripping etc.)

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How to process a silicon radiation detector

differences to industrial CMOS processes

INDUSTRIAL CMOS PROCESS

- substrate is mostly inactive
- mostly single sided processing

no back side implantation

- back side thinning can be done at the end of the process
- stepper technology is standard

REQUIREMENTS FOR RADIATION DETECTOR

- substrate is active
- double sided processing required
- thinning of substrate more complicated
- mostly 1:1 lithography
  (e.g. large detector chips)

back side implantation required

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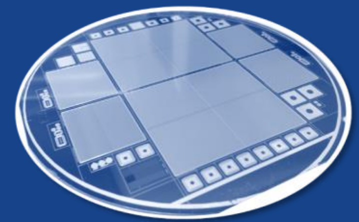
3. Special cases and technologies of radiation detectors



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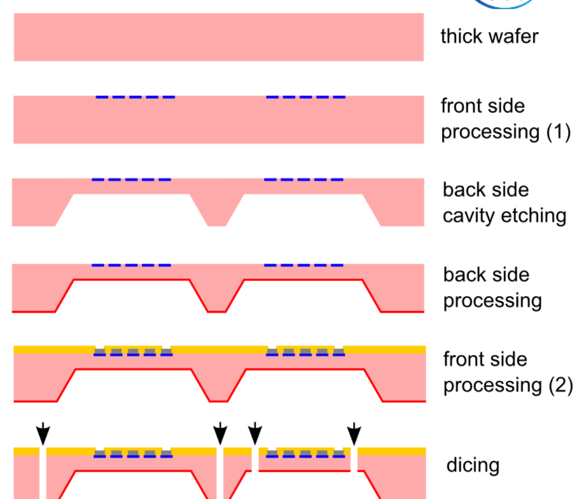
Large area thinning

- thin sensors have advantages in different fields
  - ➔ counteract irradiation induced charge loss in HEP
  - ➔ less charge loss = higher resolution in ΔE-E detectors
- thinning at the end of the process not (only limited) possible
- ➔ using anisotropic KOH etching to locally thin sensor area from back side
- membrane thicknesses of ~50...150µm possible



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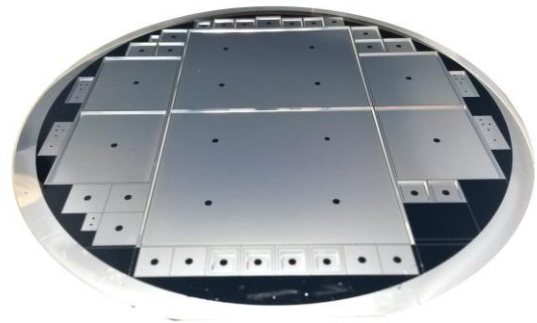
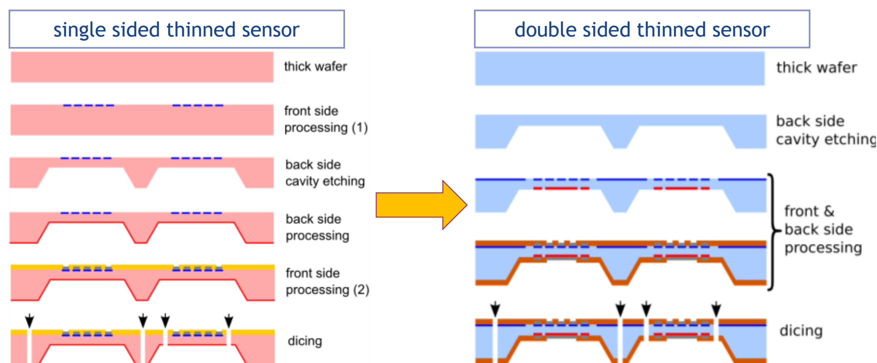


Large area thinning

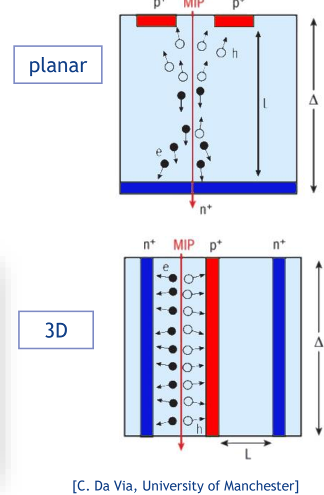
back side thinning is also possible if a double sided processed sensor is needed (e.g. strip sensor)

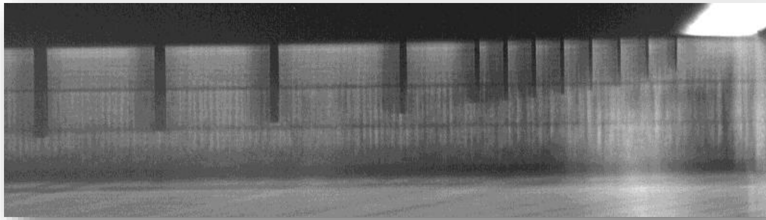
➔ etching the cavity has to be done more or less at the beginning as most steps on front and back side have to be performed alternately



3D sensors

- implanted electrodes are not placed on the surface but within the silicon bulk
  - ➔ 3D processing necessary
- making use of Deep Reactive Ion Etching (DRIE) to drill holes into the bulk
- several challenges are present (s. next slide)

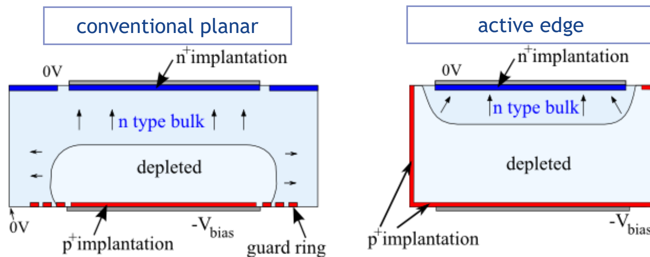


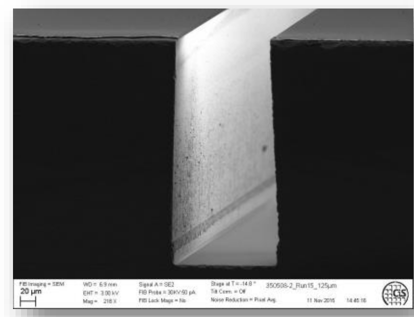


[C. Da Via, University of Manchester]

Active edges

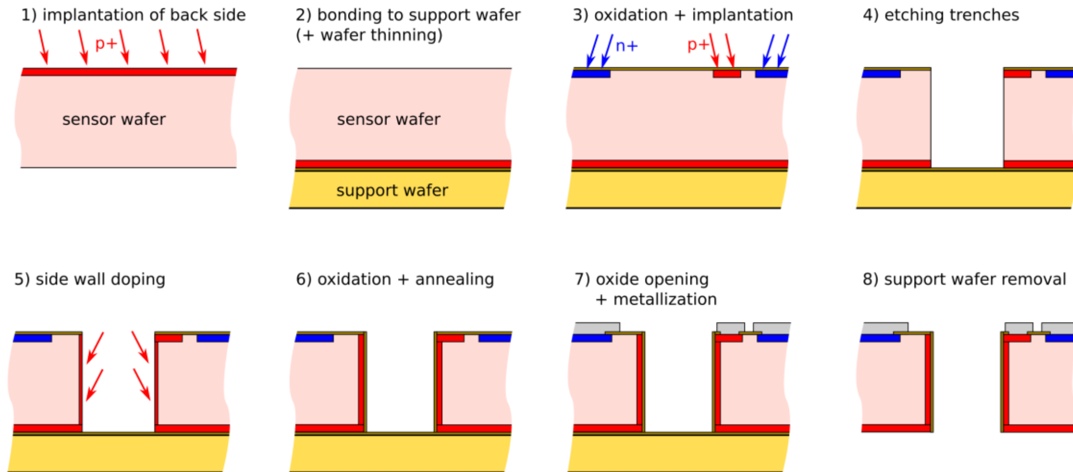
- back side implantation (ohmic contact) should be extended to the sensors side wall
- side wall doping has to be done during the wafer process
  - ➔ etching of trenches around each sensor
  - ➔ usage of a handle wafer is inevitable





Active edges

- process steps:



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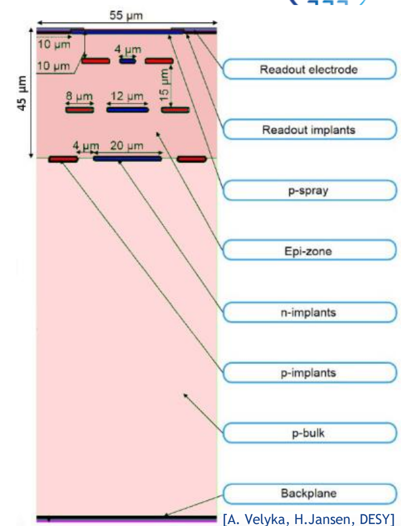
ELAD sensors

- idea: increase the resolution of pixel/strip sensors by **E**nhanced **La**teral **D**rift of the charge carriers
  - ➔ implement buried implantations within the substrate to influence the electric field
- buried implantations have to be exclusive at certain depths
  - ➔ depths down to order of 50 µm
  - ➔ not possible with conventional process
  - ➔ necessity of alternating steps of implantation and Epi-Si growth
    - quite laborious processing
    - alignment marks have to be transferred precisely from one plane to the next
- surface process is a rather conventional planar pixel technology



[A. Velyka, H.Jansen, DESY]

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Thank you very much

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