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# Interconnects and Assembly Technologies for Hybrid Pixel Detectors

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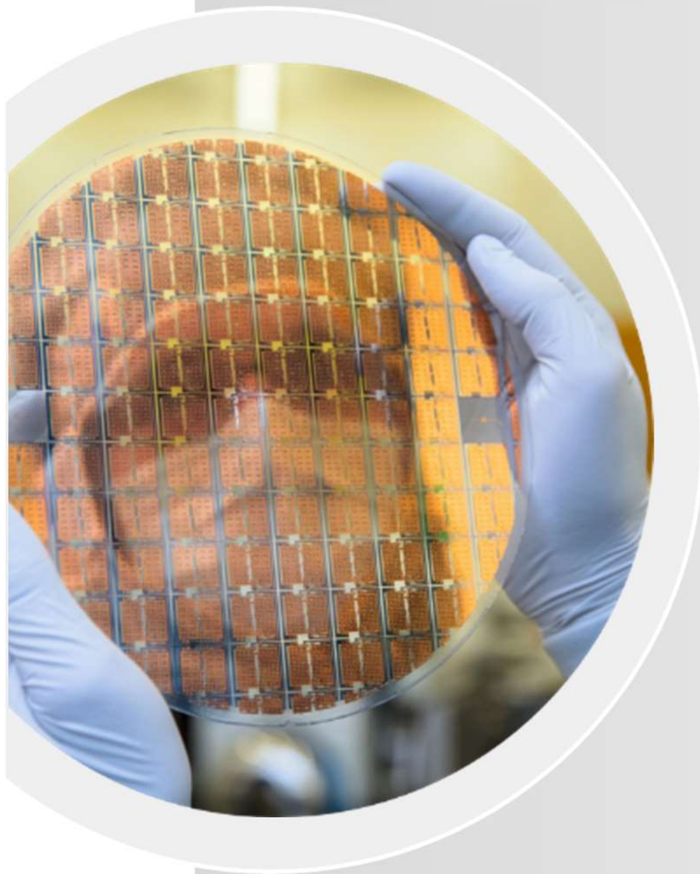
9th Beam Telescopes and Test Beams Workshop, February, 9th, 2021

# Outline



- Introduction
  - Formation of Interconnects and Assembly Process
- Bonding Technologies
  - Solder Bump Bonding
  - Transient Liquid Phase Bonding
  - Metal-Metal Bonding
  - Metal-Oxide Hybrid Bonding
- 3D Integration Technology for Hybrid Detector Modules
  - TSV Process
  - ATLAS FE-I4 TSV Hybrid Modules

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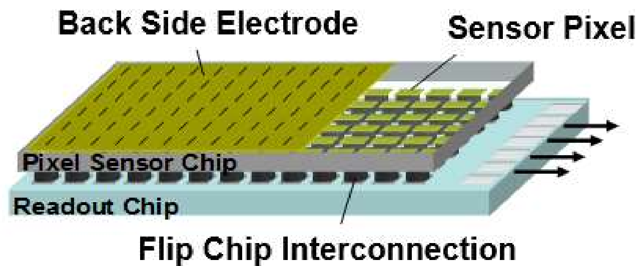
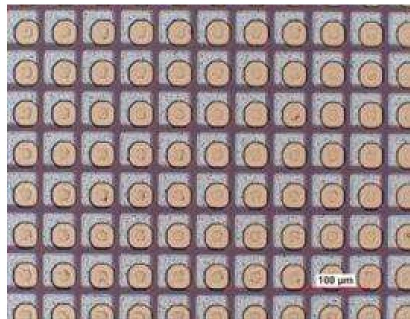
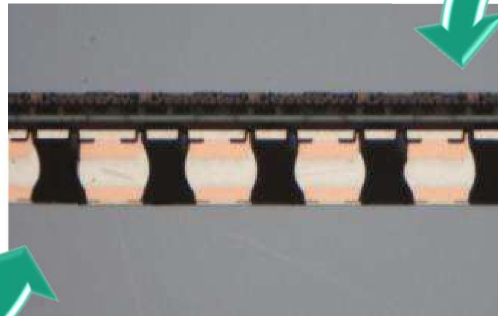
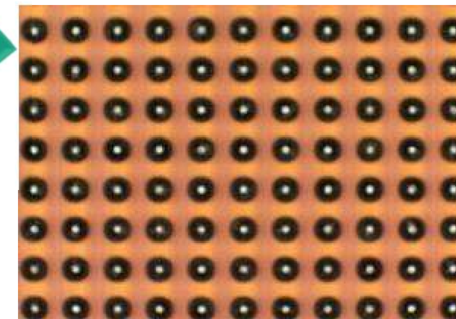
# Assembly of Hybrid Pixel Detectors

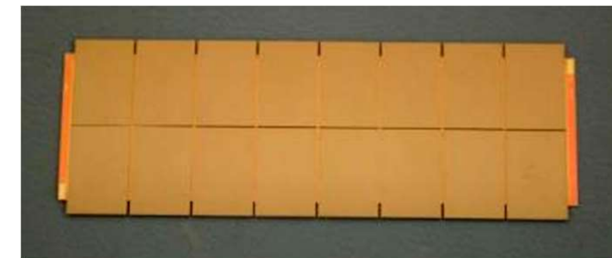



- Step 1: UBM deposition on sensor wafer
- Step 2: solder bump deposition on readout chip wafer
- Step 3: Flip Chip Assembly of readout chip to sensor chip









## Advantages:

- Separate development and optimization of sensor and readout chip
- Variable use of different semiconductor sensor materials

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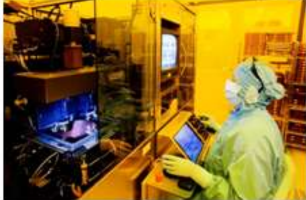
# Wafer Level Packaging: Micro Bumping and Hybridization Process

Seed Layer → Resist Process → Lithography → Plating → Strip / Etching → Dicing → Assembly

Sputter

Spin Coater



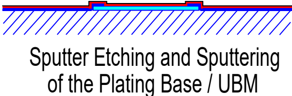
Mask Aligner

Wafer Plating

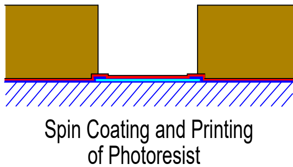
Wet Etching

Dicing

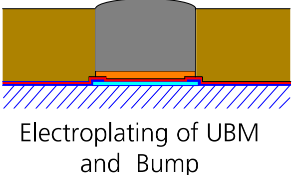
Flip Chip



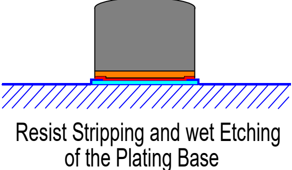
Sputter Etching and Sputtering of the Plating Base / UBM



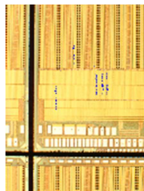
Spin Coating and Printing of Photoresist

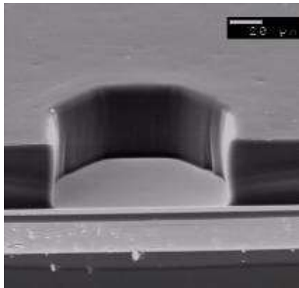


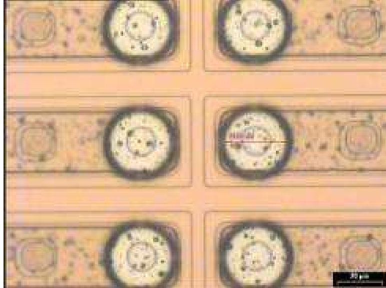
Electroplating of UBM and Bump

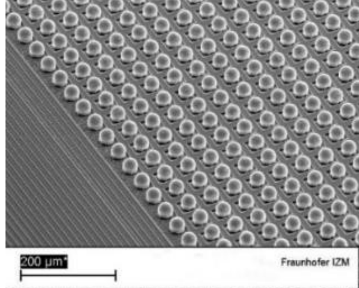


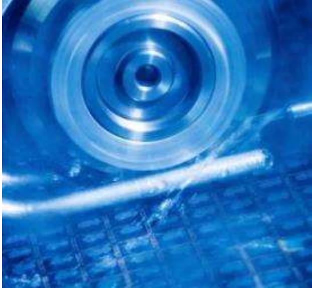
Resist Stripping and wet Etching of the Plating Base









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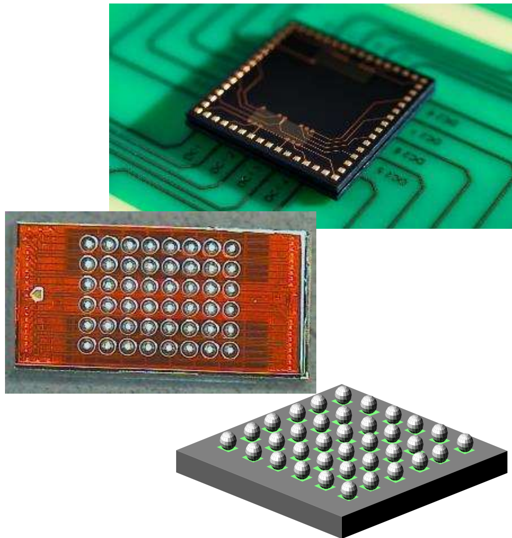
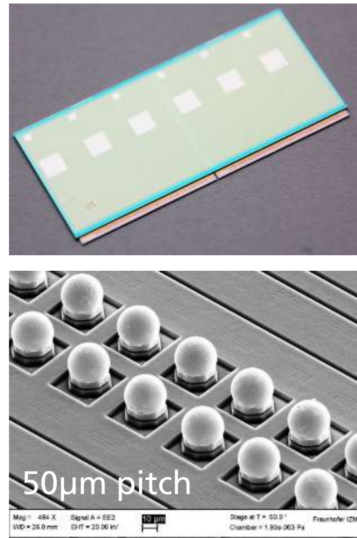
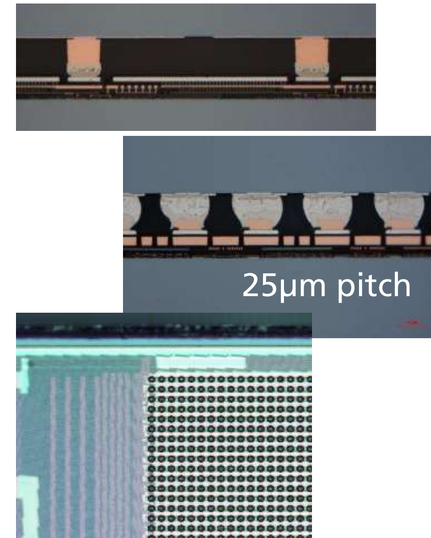
# Key Parameter: Interconnection Pitch



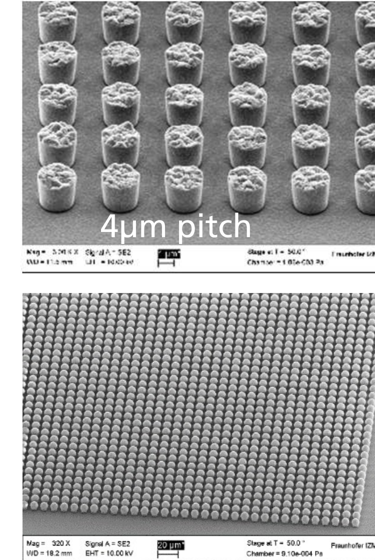
**Solder balls for PCB assembly:**
Pitch 500…300µm
Ball size: 300…150µm
Material: Solder balls




**Fine pitch bumping:**
Pitch 100…50µm
Bump size: 50…25µm
Material: Solder bumps, pillar bumps with solder cap




**µ-bumping:**
Pitch 50…20µm
Bump size: 25…12µm
Material: Solder bumps, pillar bumps with solder cap




**Sub-10µ-pitch:**
Pitch 10…2 µm
Bump size: 6…1µm
Material: pillar bumps with solder cap, pillars, pads

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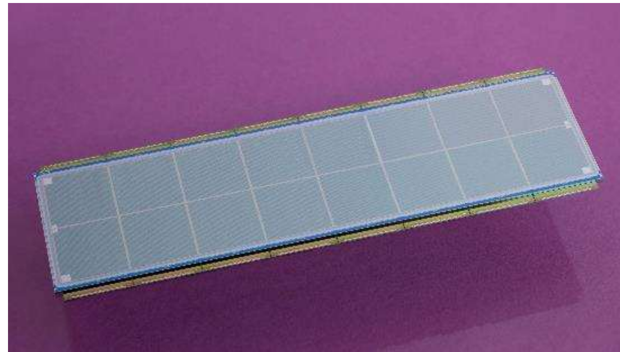
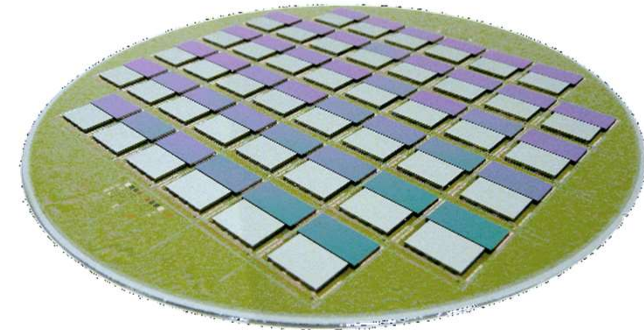
# Assembly by Flip Chip Bonding

**Chip to Chip**



**Chip to Wafer**



*Flip Chip Assembly Bonding Tools:*

- High accuracy chip pick and place process +/- 1.5µm
- Interconnection by temperature and optionally pressure:
  - reflow soldering
  - thermo-compression bonding,
  - thermosonic bonding

*Requirements:*

- Chuck size: sensor chip size (~10cm) or wafer size up to 300mm and corresponding working space
- Load station (from dicing frame or from waffle pack)
- Consistent with subsequent dicing process
- Advantage: Chips/wafers with different size and pattern can be merged

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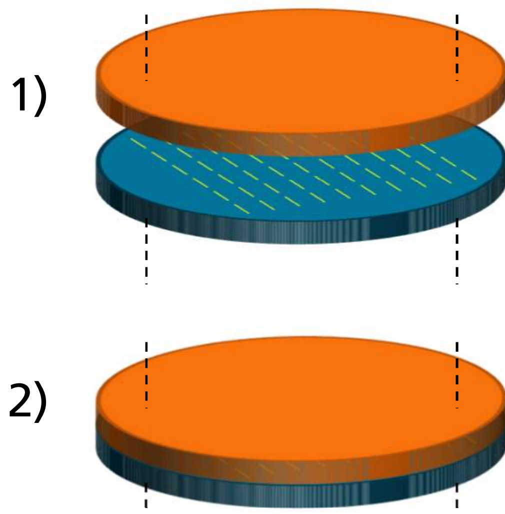
# Assembly by Wafer to Wafer Bonding




*Fully/Semi-Automated Wafer Bonder:*

- Wafer size 200 mm, 300 mm
- maximum force: 60 kN
- maximum temperature: 550 °C
- vacuum: $1x10^{-5}$ mbar
- Wafer to wafer alignment accuracy <1µm

*Applicable Bonding processes:*

- Adhesive bonding
- Silicon direct bonding
- Anodic bonding
- Solder/eutectic bonding
- Thermo-compression bonding
- Metal-oxide hybrid boding

*Requirements:*

- Particle free wafer surfaces
- Top and bottom wafer of the same size
- Top and bottom chip have the same size and/or exactly the same chip step/ repeat pattern (also for different foundries)
- Special processes with pre-assembled wafer possible (hermetic MEMS capping)
- Consistent with subsequent dicing process

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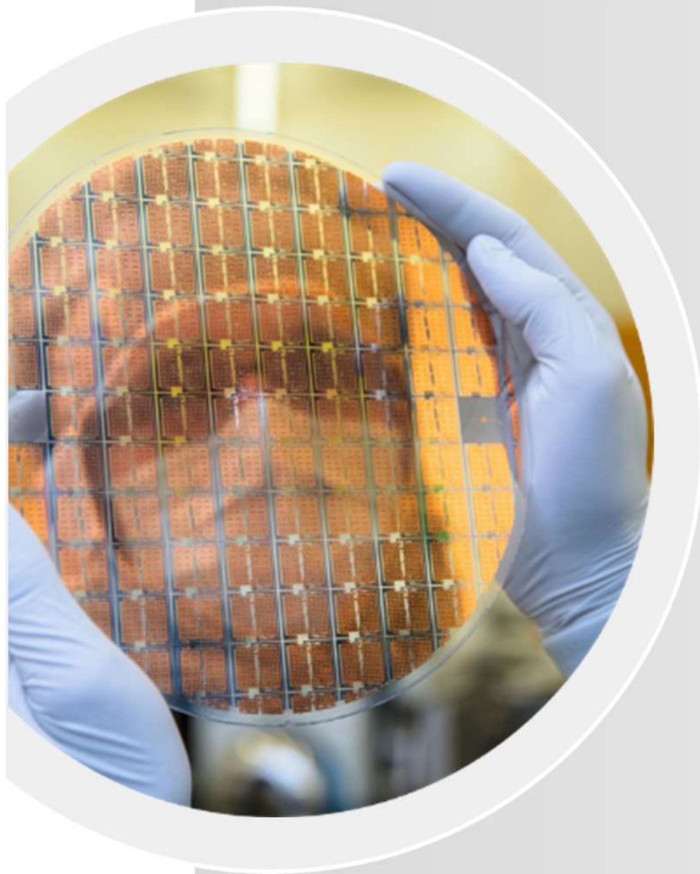
# Overview



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  - TSV Process
  - ATLAS FE-I4 TSV Hybrid Modules

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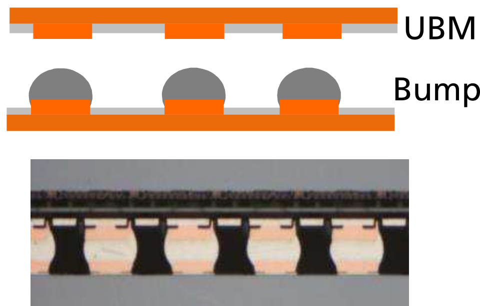
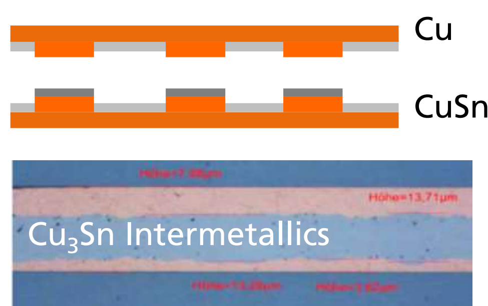
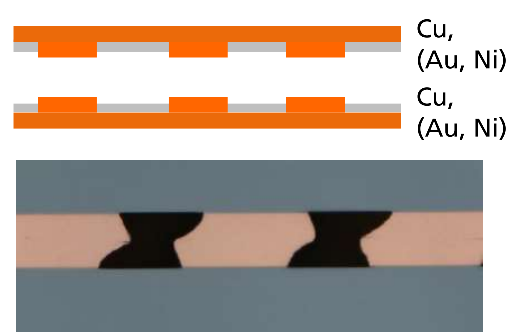
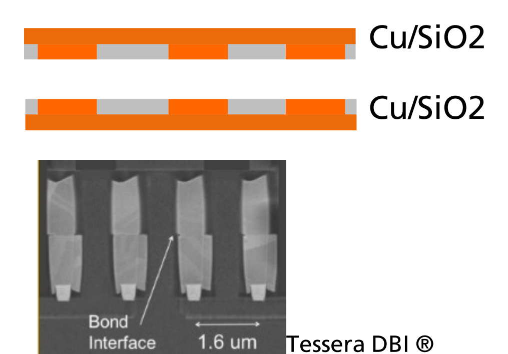
# Bonding Technology

| Solder Bump Bonding | Transient Liquid Phase Bonding (TLPB/SLID) | Metal-Metal Direct Bonding | Metal – Oxide Hybrid Bonding |
|---|---|---|---|




Tessera DBI ®

**Solder Bump Bonding**
- ECD solder bumps (SnAg, In, InSn, AuSn, Cu-pillar/Sn cap)
- Reflow temperature
- without or low pressure

**Transient Liquid Phase Bonding (TLPB/SLID)**
- ECD Cu and Cu-Sn pads
- High melting $Cu_3Sn$ IMC
- Temperature, pressure

**Metal-Metal Direct Bonding**
- ECD pads (Cu, Au, Ni)
- Planarized surfaces, pre-conditioning
- Temperature, pressure

**Metal – Oxide Hybrid Bonding**
- ECD Cu pads (or Ni)
- Surface planarization (CMP)
- Surface activation (plasma)
- Room temperature bond
- Annealing step

| CHIP TO WAFER | CHIP TO WAFER; WAFER TO WAFER BONDING | WAFER TO WAFER BONDING |
|---|---|---|

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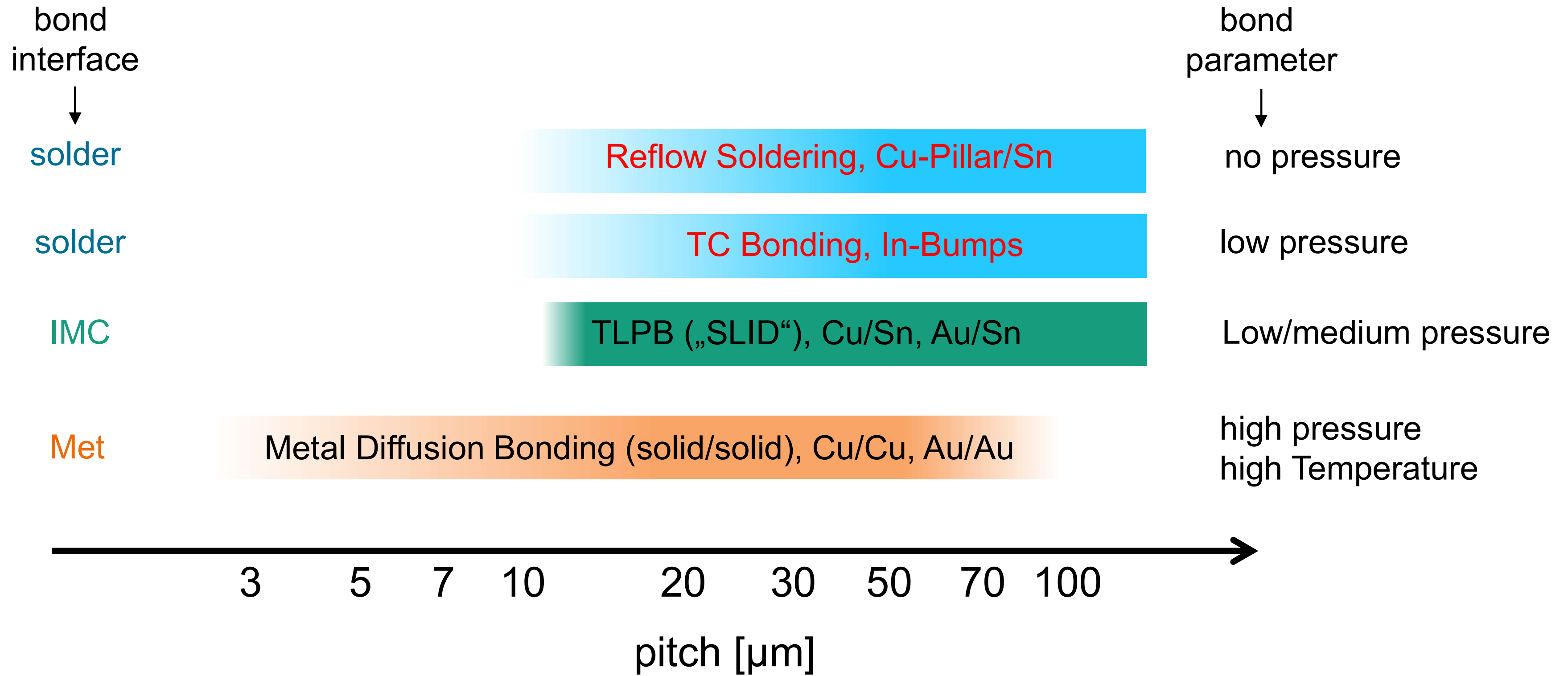
# Assembly Roadmap

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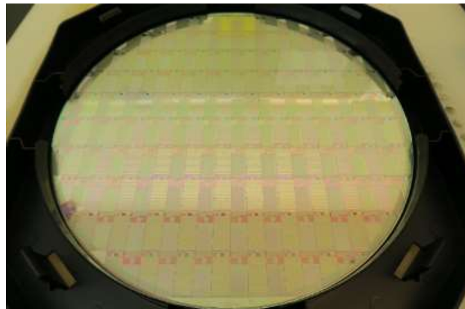
# RD53A/RD53B Solder Bumping on 300mm Wafer

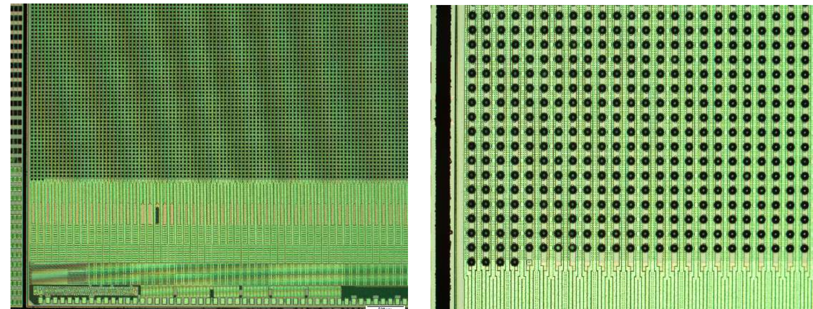
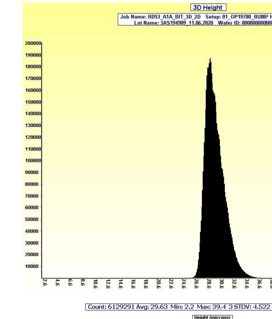
*RD53 collaboration*
*https://rd53.web.cern.ch/RD53/*
*ATLAS collaboration*
*https://atlas.cern/discover/collaboration*
*CMS collaboration*
*https://cms.cern/collaboration*

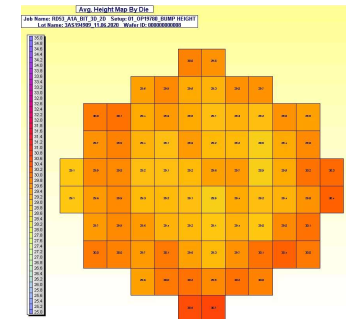
- 300mm wafer, TSMC 65nm technology
- ~ 90/132 RD53A/ITKPix readout chips per wafer
- SnAg solder bumping, reflow temperature ~250°C
- Bump size and height ~25..30µm, pitch 50x50 µm²
- RD53A: 400x192 bumps (76.800 chip / 6.835.200 wafer)
- RD53B: 400x384 bumps (153.600 chip / 20.275.200 wafer)
- Volume production ready

- Wafer thinned thickness:
  - 500µm for setup batch
  - 150µm for qualification batch

**Complete industry standard process line for 300mm wafer process available**


300mm RD53A wafer



Details of RD53A ROC after bumping


Bump height statistics: 29,6µm, 3σ 4,5µm

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# ATLAS/CMS ITK Pixel Detector Upgrade Module Assembly

RD53 collaboration
https://rd53.web.cern.ch/RD53/

ATLAS collaboration
https://atlas.cern/discover/collaboration

CMS collaboration
https://cms.cern/collaboration

- Assembly of single chip, double chip and quad chip modules:
  - 6“ planar sensors
    100µm, 150µm thickness
  - 6“ 3D sensor wafer
  - 8“ CMOS sensor wafer,
    150µm thickness
- Readout chip size:
  - RD53A regular size ~$2x1cm^2$
  - RD53B (ITKPix) size ~$2x2cm^2$

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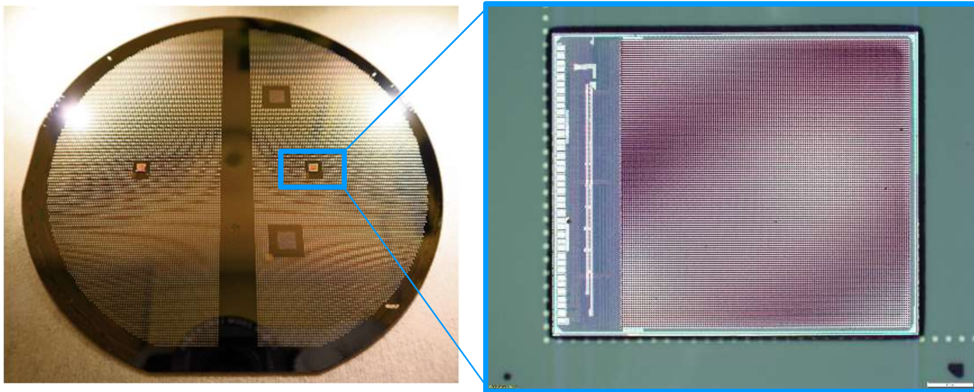
# Single Chip Bumping Using Die Attach on Carrier Wafer

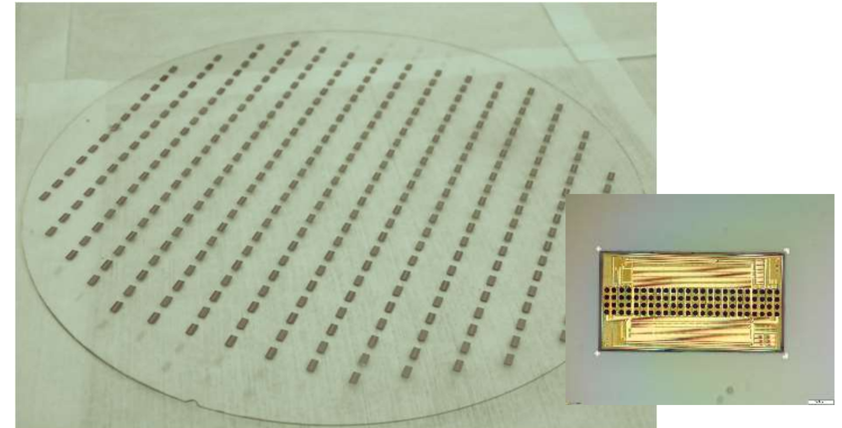
## - Bumping process line can handle only wafer size substrates -

### Prototyping - High Accuracy



- R&D projects with only 2…20 chips available or with economically justifiable effort manageable
- Die bond on carrier wafer
- One or two chips per carrier wafer, high alignment accuracy
- Chip thickness < 500µm
- Minimum structure size so far 12µm bump size / 25µm pitch

### Low/Medium Volume - Medium Accuracy



- 50…1000 Chips available (small volume batch)
- Die bond on carrier, placement accuracy +/-10µm
- Several hundred chips per carrier wafer
- Chip thickness < 500µm
- Minimum structure size so far 90µm bumps / 150µm pitch

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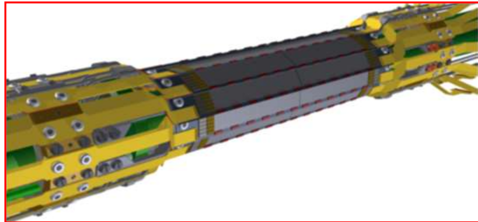
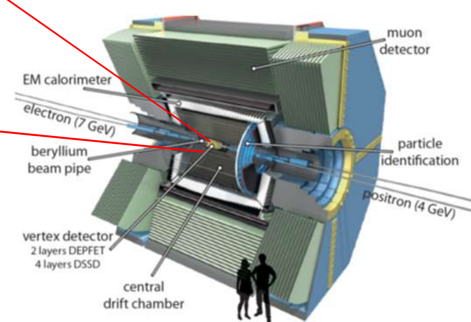
# Application: Switcher Chips for BELLE2 Detektor Modules

Single Chip Bumping for SuperKEKB Linear Collider (KEK, Tsukuba, Japan)

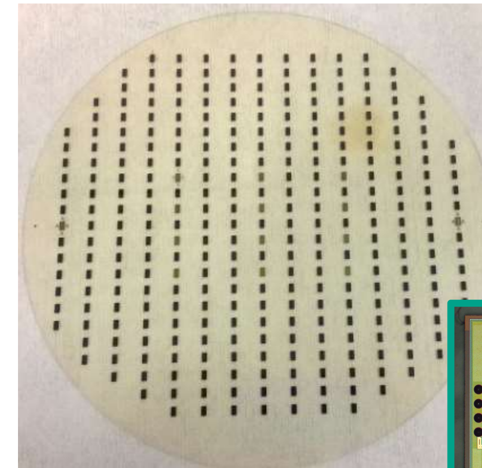


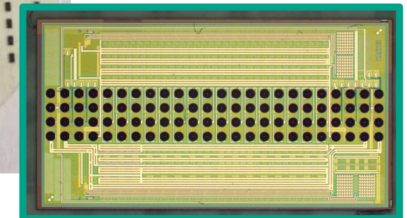
The Belle II Pixel Detector, Jochen Dingfelder University of Bonn Vertex 2017, Las Caldas, Sep. 12, 2017.

BELLE II: PXD - 2 layers of DEPFET- based silicon pixels

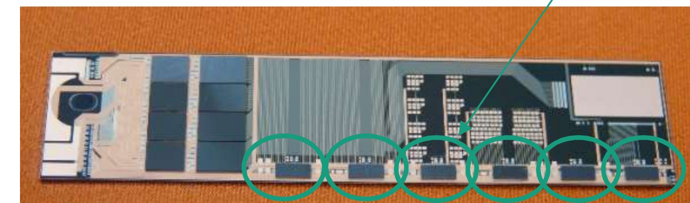



200mm Carrier wafer with Switcher Chips





BELLE II - Module



Project: 2016 – 2019

- Development of a Volume Single Chip Bumping Technology
- Bumping of more than 1000 single dies, SnAg bumping
- Assembly of bumped switcher chips on BELLE II silicon module substrates (6 chips per module)

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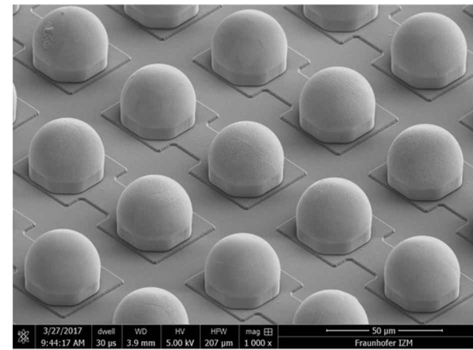
# Low Temperature Flip-Chip Assembly of High-Z Detector Materials

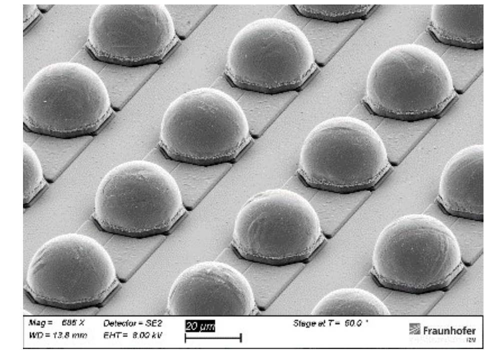
## Indium and Indium-Tin bumping

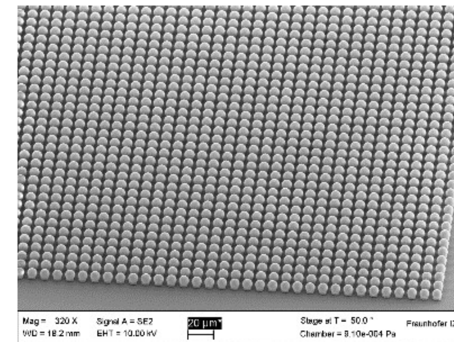
- If bonding process below 200°C / 150°C is required for temperature sensitive sensor materials
- $T_M$(Indium) = 156 °C; $T_M$(In52Sn48) = 117 °C for thermally sensitive bonding processes
- Electrochemical deposition of Indium or Indium/Tin
- Standard Pitch ~50µm, Bump size 25µm
- minimum pitch about 10µm / 6µm bump size
- Flip chip bonding process In to In or In to Au pad surface, bonding temperature at 100°C evaluated

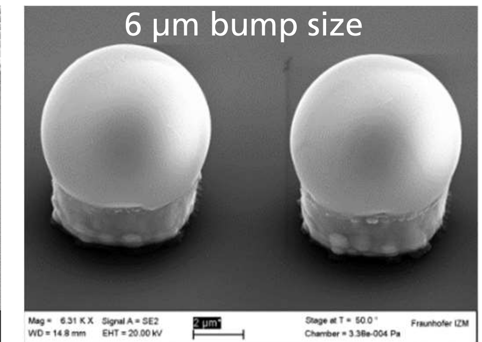
Indium Bumping



Indium-Tin Bumping








Indium Bumping 10 µm Pitch for IR image sensors

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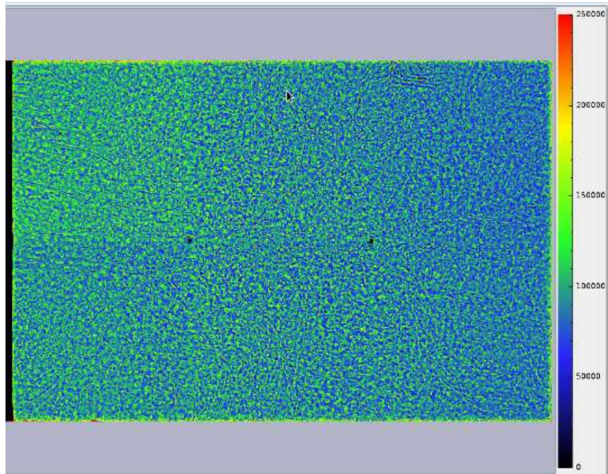
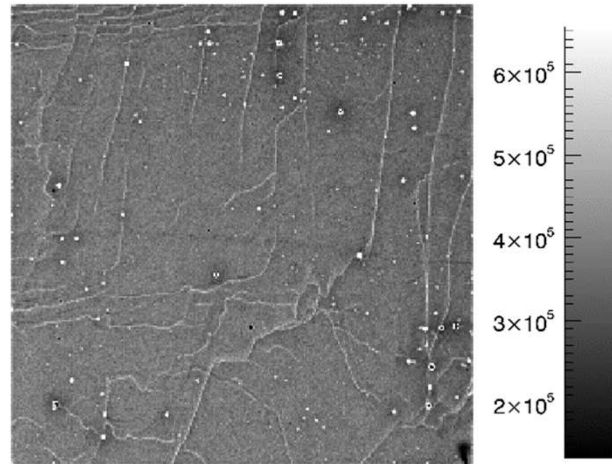
# Detectors with “high-Z” Sensors for Hard X-rays

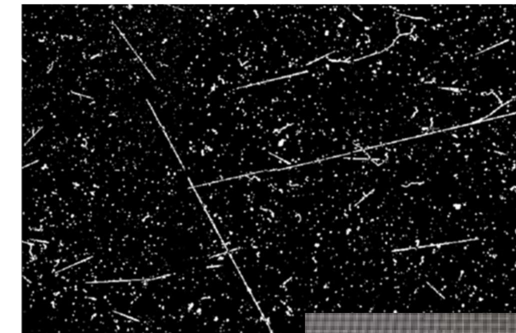
GaAs 3x2 HEXA_Mo35kV



CdTe IZM single 3 (Xn2017_05)




Ge 3x2 HEXA Detector



spot of cosmic radiation

(Sarajilic, 2017 JINST 12 C01068)

All modules with MEDIPIX / TIMEPIX readout chip:

- Photon Counting ROC
- Bump size: 25…30µm
- Bump Pitch: 55µm (x, y)
- Chip Size: ~14 x 16 cm²
- Bump matrix: 256x257 (65792 per chip)
- Module Assembly using In-Bumps

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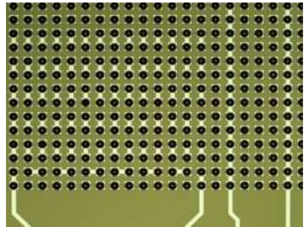
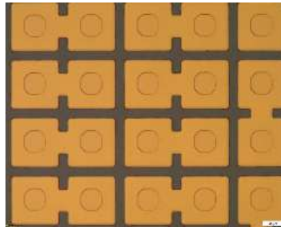
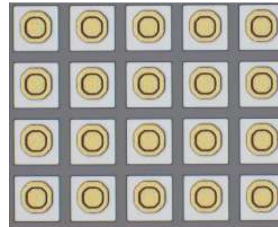
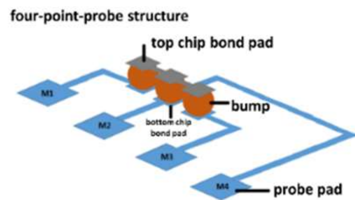
# Process Evaluation: Indium Bump (Thermo)-Compression Bonding

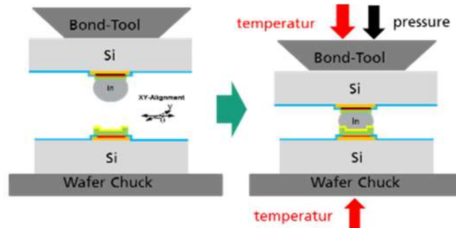
- Bonding temperature below 100°C using a low temperature compression bonding process
- Daisy chain and single bump electrical resistance measurement design on MEDIPIX3 size test chip


In-Bump on Top-Chip


Passivation defined sputterd NiAu UBM


Pad defined electroplated NiAu UBM

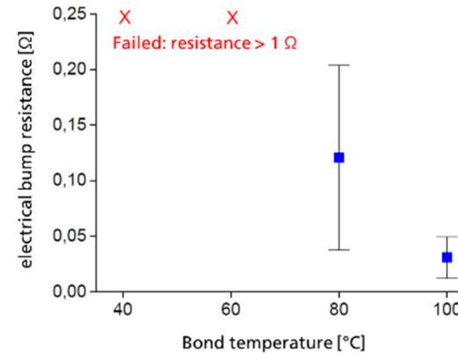


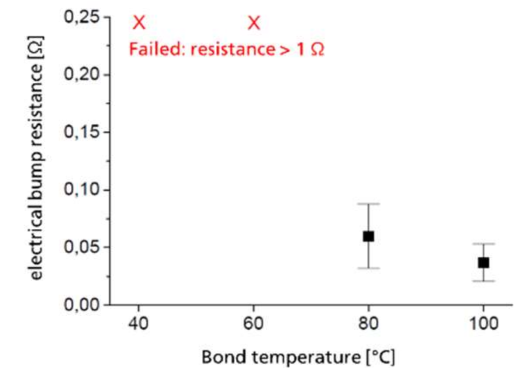



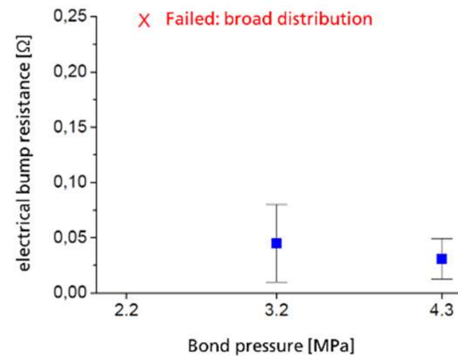

Compression of Indium bumps on

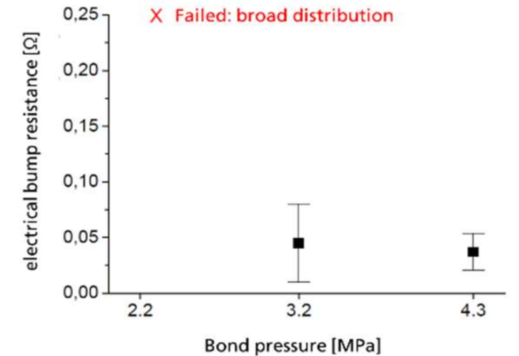
Passivation defined NiAu

Pad defined NiAu metal

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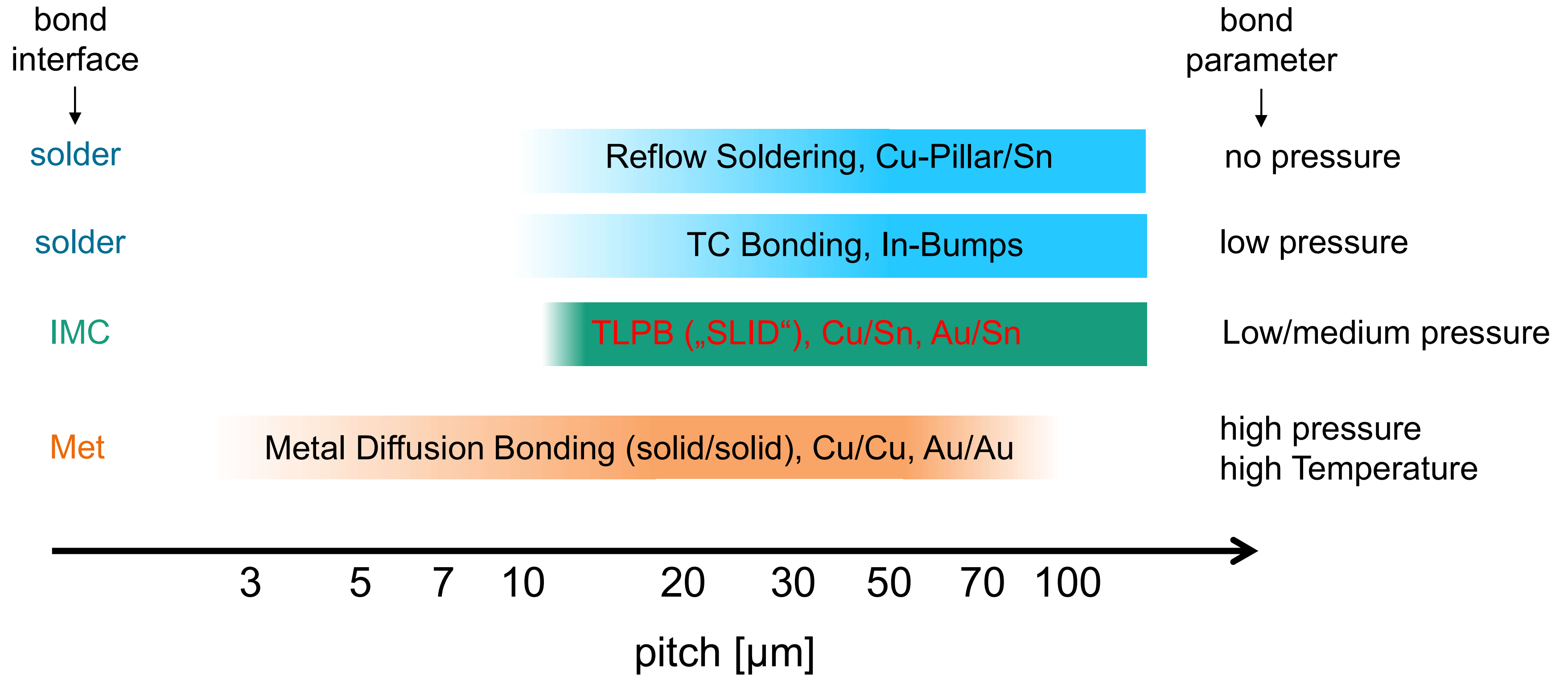


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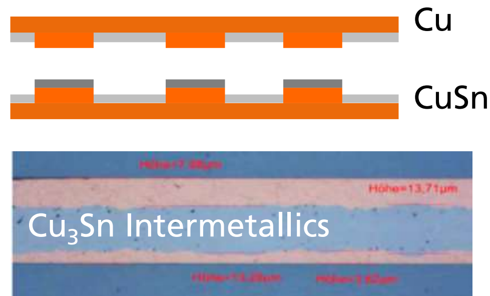
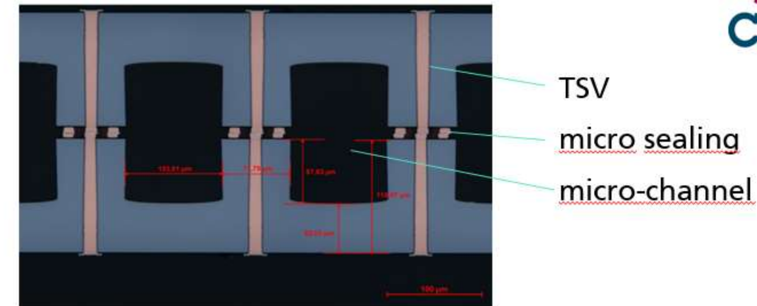
# Transient Liquid Phase Bonding (TLPB) / Solid Liquid Interface Diffusion (SLID)




- ECD Cu and Cu-Sn pads
- High melting $Cu_3Sn$ IMC (676°C)
- Bonding parameters: 220…280°C, 10…50MPa, T= min
- High planarity necessary
- Wafer to wafer assembly
- Chip to Chip in inert atmosphere

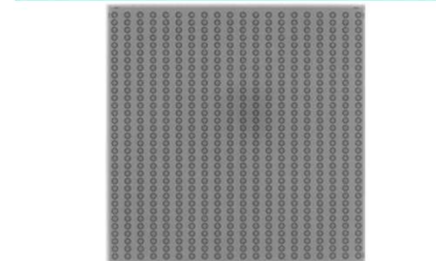
## Hermetic Sealing

Silicon interposer:
2 half-shells forming a microchannel cooler



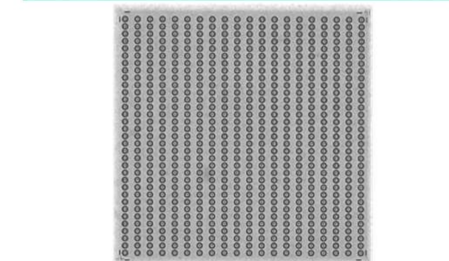

4-port fludic interposer

Results CuSn



remaining Sn left at the edge

Results AuSn



Au Intermetallic compound $Au_5Sn$

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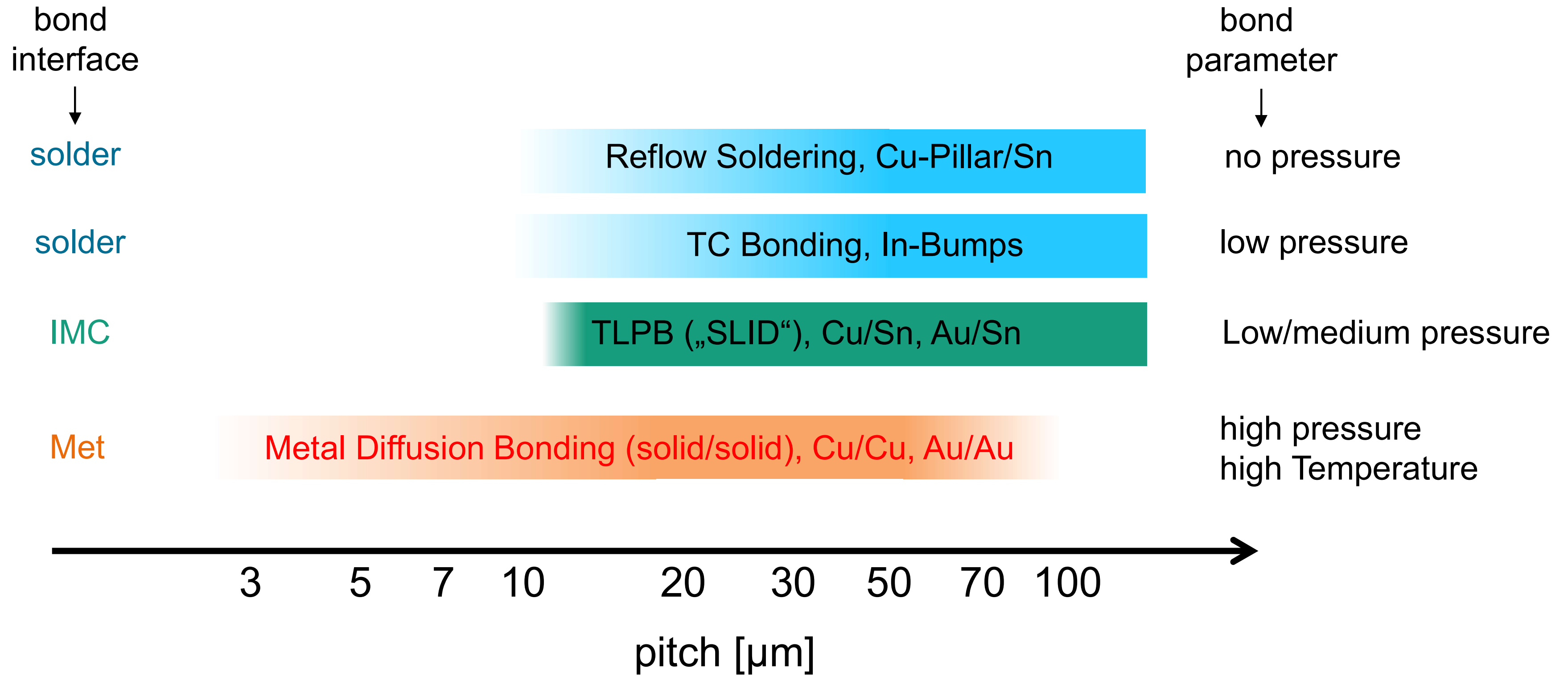
# Assembly Roadmap

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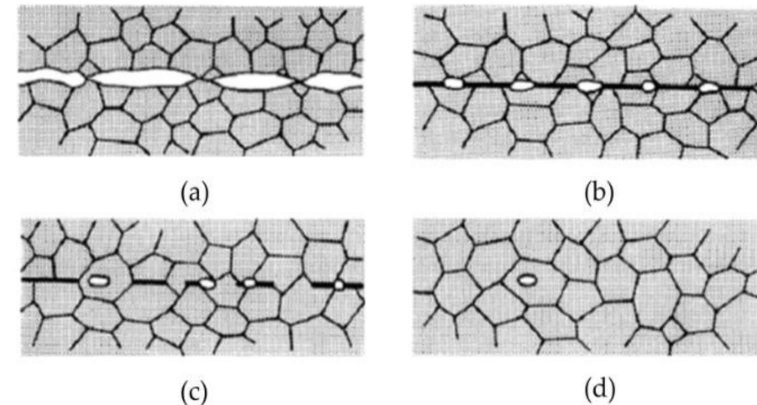
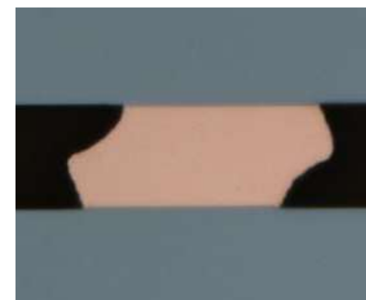
# Metal-Metal Diffusion Bonding

Cu, (Au, Ni)

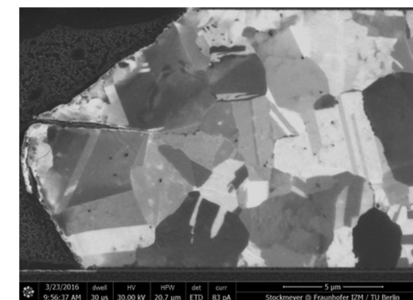
Cu, (Au, Ni)




- ECD Cu pads (Au, Ni)
- Planarized surfaces, pre-conditioning
- Bonding parameters:
  - 250°C…400°C,
  - 50…150MPa
  - t= min…h
  - Vacuum, inert atmosphere
- Available for wafer to wafer bonding
- R&D for Chip to Chip assembly



Cu-Cu bond



Cu-Cu bond
SEM image

Au-Au bond

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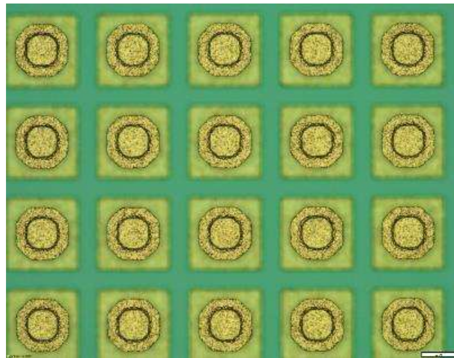
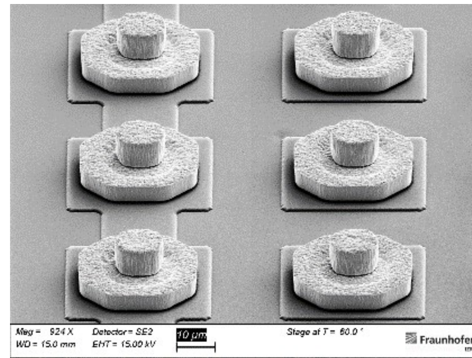
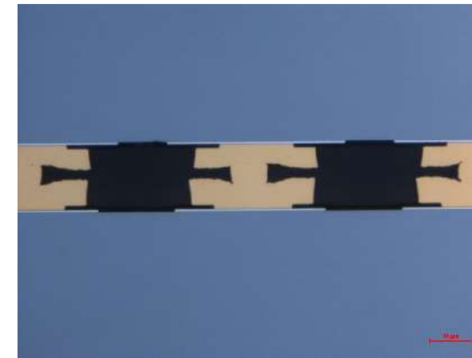
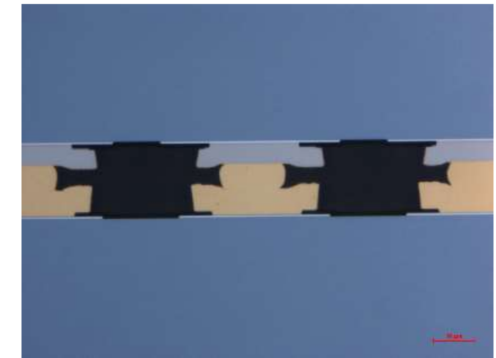
# Gold µ-pillar Thermo-Compression Bonding


Au or Ni/Au pad on top chip



Au µ-pillar on bottom chip


Au µ-pillar after TC bonding onto Au pad


Au µ-pillar after TC bonding onto Ni/Au pad

- evaluation of thermo-compression (TC) bonding process
- Daisy Chain Test Design for MEDIPIX3 chip size, 256x256 bump matrix (65536 bumps per chip)
- Regular pad: 30µm, 150MPa → ~7kN bonding force per chip
- Pillar pad: 10µm, 150Mpa → 770N bonding force per chip

- Chip to chip bonding
- Bonding temperature range: 250°C … 300°C
- Bonding pressure: 100 … 150 Mpa
- Applicable for Au-Au or Au-NiAu bonding

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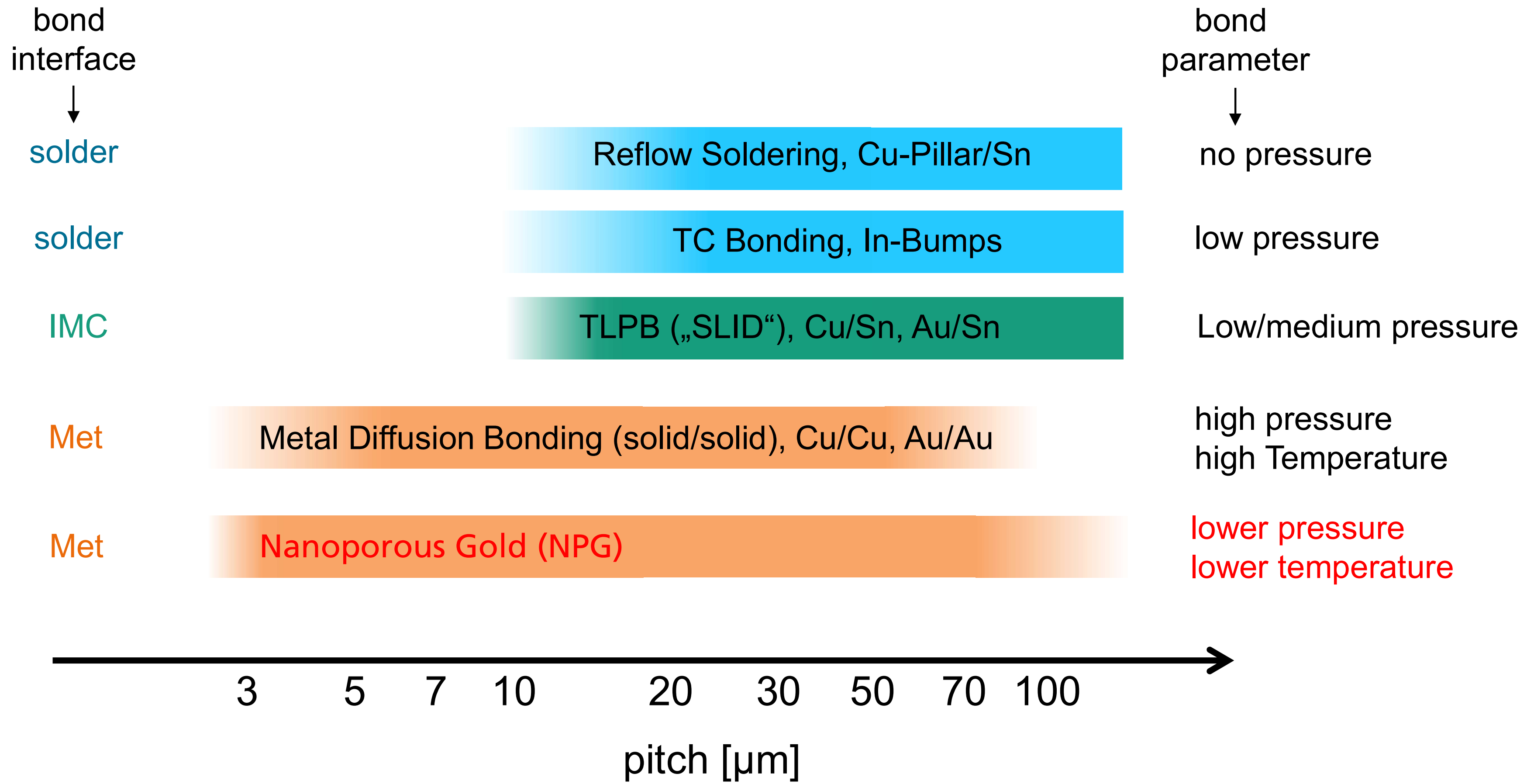


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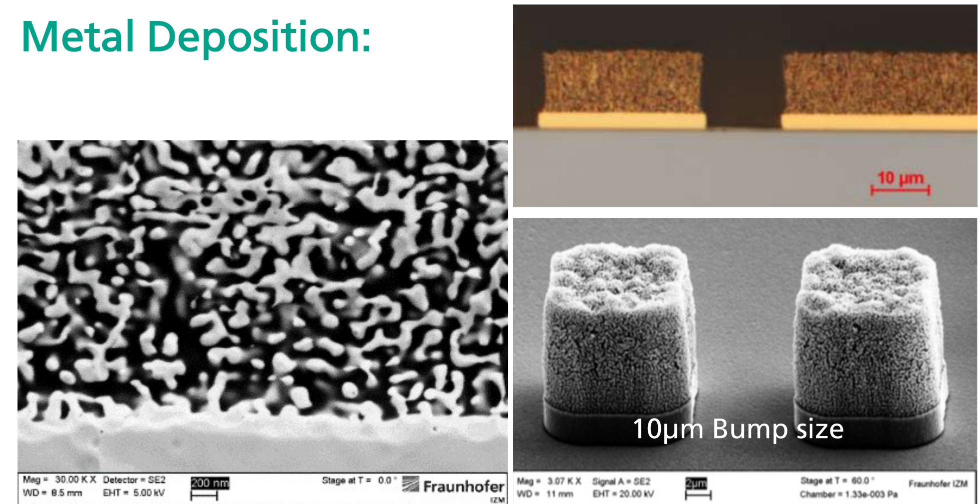
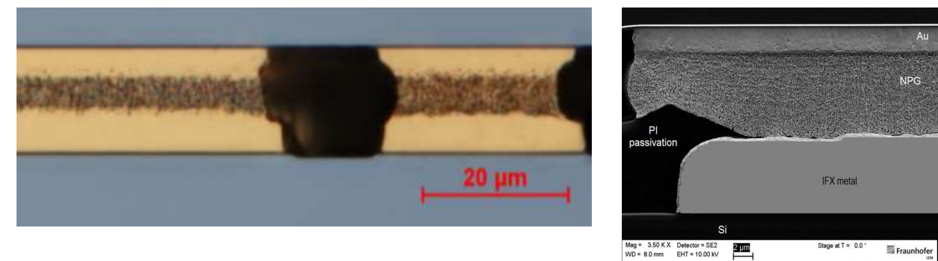
# R&D: Nano-Porous Gold (NPG) Bumps for Chip Interconnections

- Development electro-plating baths for Ag/Au alloy deposition
- Prozess flow similar to conventional Au Bumping
- Skeleton formation due to dealloying by wet etching of Ag
- Average pore sizes adjustable from 20 nm up to 500 nm
- TC-Bonding with reduced bonding parameters possible, typ. 10 MPa @ 200°C or 15 Mpa @ 150°C
- Sponge-like Au is fully compressible and able to compensate topography and inhomogeneity on chip and substrate

## Metal Deposition:




## Bonding:

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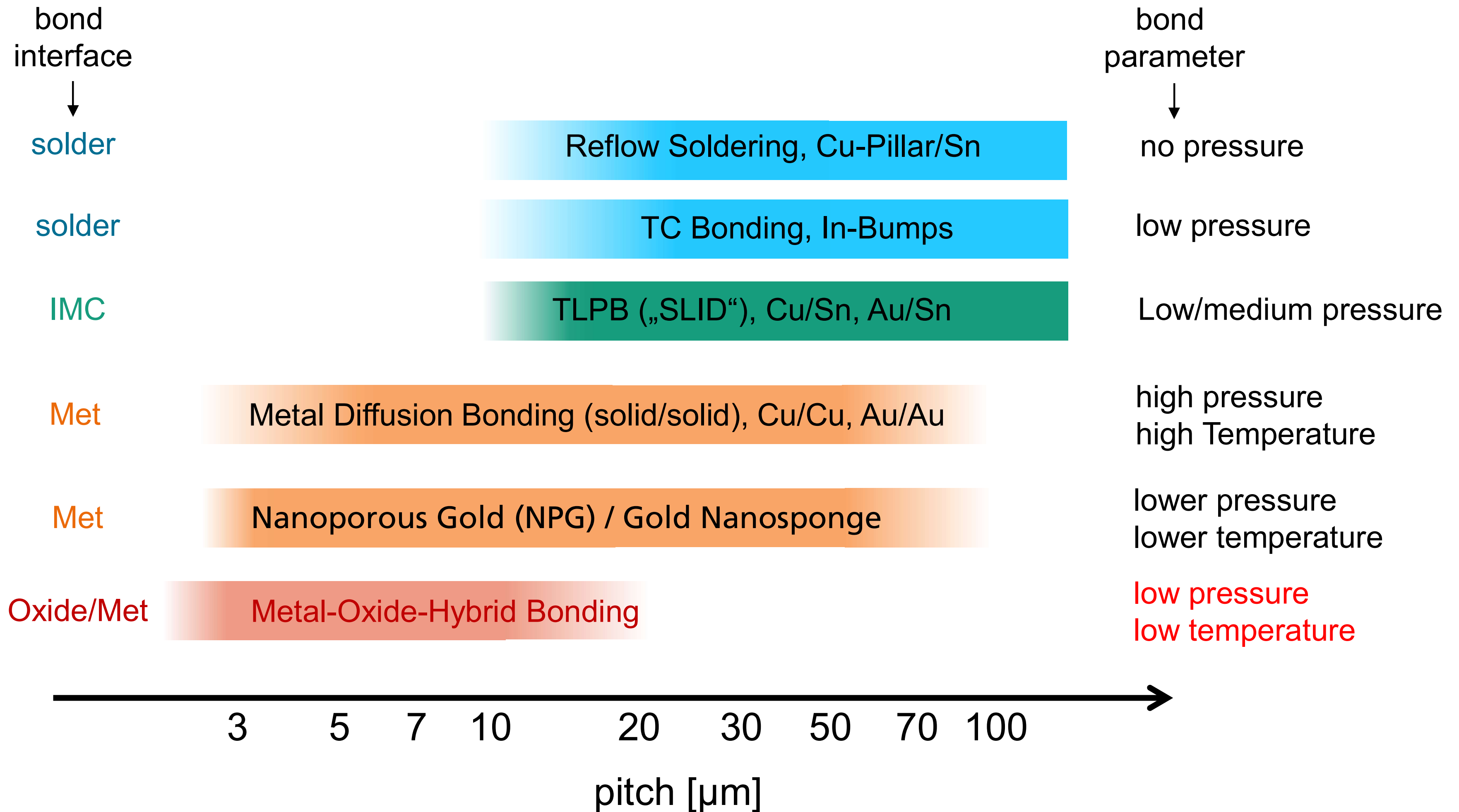


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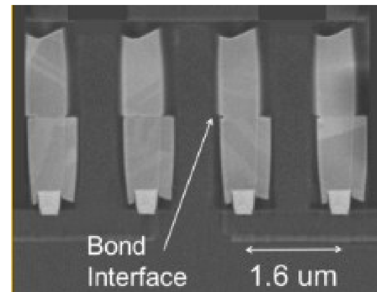
# Metal – Oxide Hybrid Bonding




Source:

Tessera DBI ®

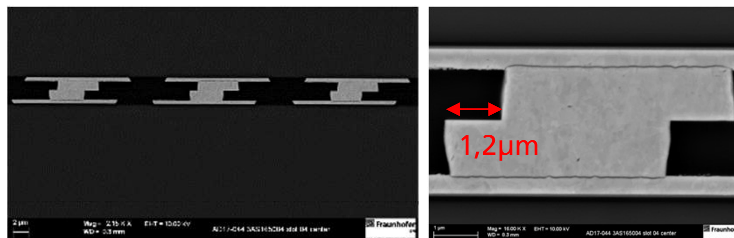
**Process:**

- ECD Cu pads
- Surface planarization (CMP)
- Surface activation (plasma, chemicals)
- Room temperature bond
- Annealing 175°C … 400°C
- Memory Stacking, Image Sensors

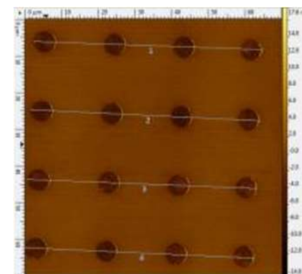
**Motivation for DBI:**

- W2W , (D2W)
- Highest interconnect density
- I/O Pitch down to 1 µm
- High alignment accuracy
- No bumps
- No intermetallics
- No gap – no underfilling
- High reliability

Fraunhofer IZM-ASSID: 300mm W2W Bonding with <5µm alignment accuracy




Fraunhofer test chip with 4 µm pad /18µm pitch, Metal density: 4.5%



| | FhG IZM ASSID (Results) |
|---|---|
| Roughness beside TSV (Oxide) Ra | 0,146 nm |
| Roughness on TSV (Cu) Ra | 0,163 nm |
| Planarization | 5nm @ 100µm |

J. Wolf „3D System Integration Requirements and Potential Solutions", European 3D Summit, 22-24.1.2018, Dresden, Germany.

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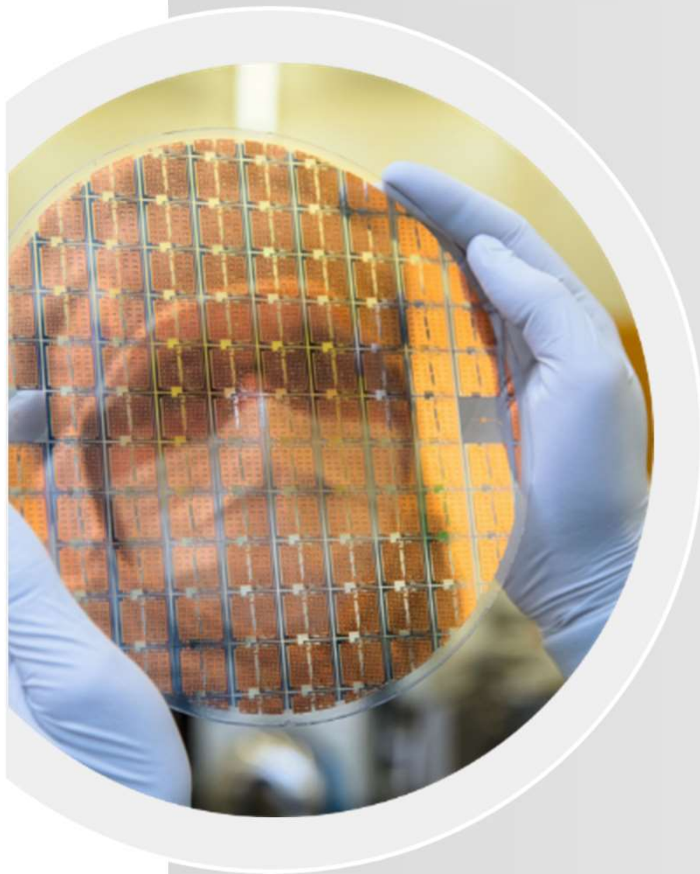
# Overview



- Introduction
  - Formation of Interconnects and Assembly Process
- Bonding Technologies
  - Solder Bump Bonding
  - Transient Liquid Phase Bonding
  - Metal-Metal Bonding
  - Metal-Oxide Hybrid Bonding
- 3D Integration Technology for Hybrid Detector Modules
  - TSV Process
  - ATLAS FE-I4 TSV Hybrid Modules

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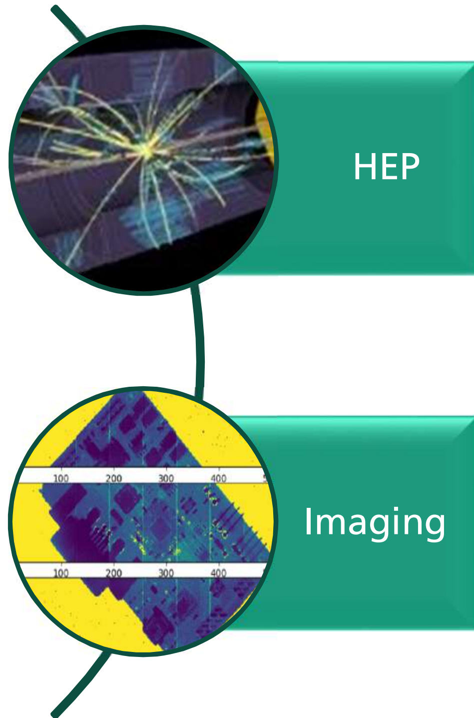
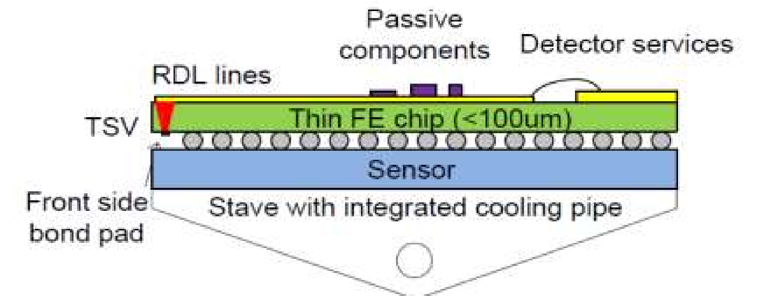
# Adcanced Packaging - 3D Integration with Through Silicon Via (TSV)

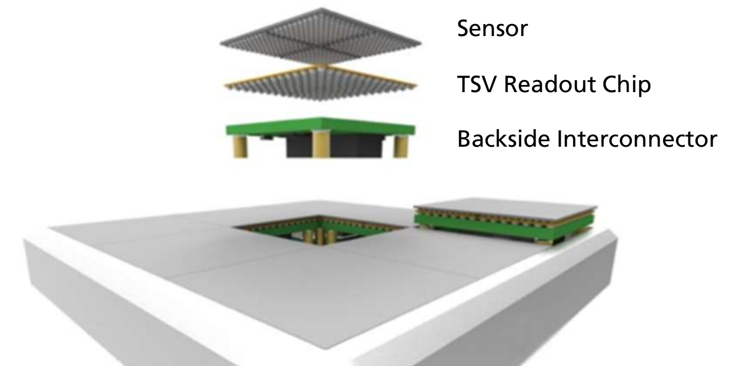



- Low material budget
- Thin chip modules
- Multichip modules
- TSV backside interconnection

- Four side stitchable modules
- Heterogenious sensor integration
- Multichip modules
- TSV backside interconnection




AIDA-2020, F. Huegging




Courtesy of DESY

→ TSVs in readout chip wafer using via last process from wafer front- or wafer backside

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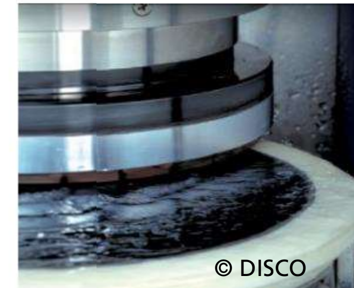
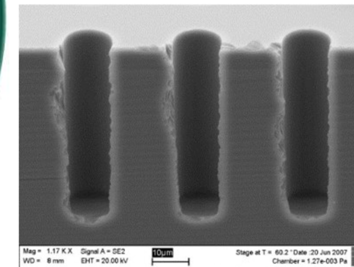
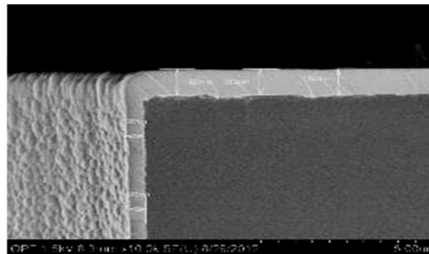
# Basic Process Steps of TSV Formation – TSV via last from wafer backside



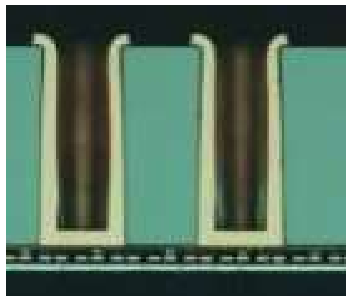

1. Si- wafer thinning



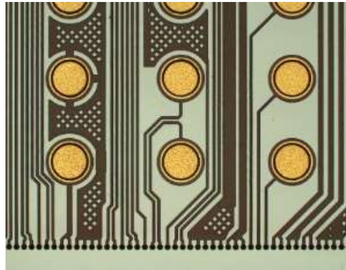
2. TSV silicon etching
   DRIE BOSCH Process



3. TSV and wafer surface oxide passivation
   TEOS, PE-CVD, SA-CVD
4. Oxide Etch at via bottom
5. Barrier-/Seed-Layer
   Ti (TiW, TiN, Ta(N)) / Cu HI-PVD



6. TSV Cu filling by
   ECD



7. Backside Cu RDL by
   ECD + Passivation
   and Bond Pad UBM

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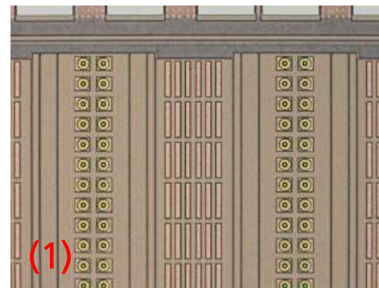
# TSV Process with ATLAS FE-I4 readout chip wafer

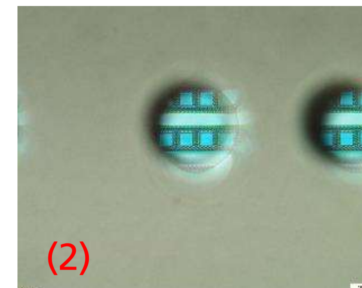
UNIVERSITÄT BONN

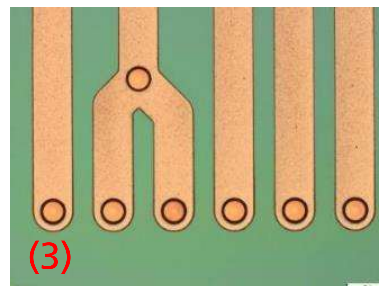
AIDA 2020

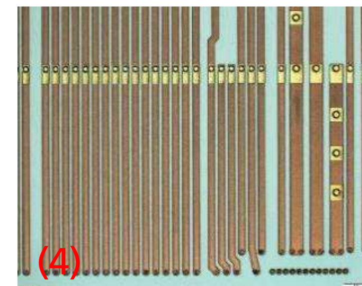
*Backside TSV via last process:*

- Frontside UBM pixel pads (1)
- Frontside carrier wafer bond
- Backside thinning (100µm/80µm)
- Backside TSV Si etch and oxide passivation (2)
- Oxide etch on BEOL-M1-Layer
- TSV/RDL-Cu metallization (3)
- Backside passivation layer
- Backside UBM contact pads (4)

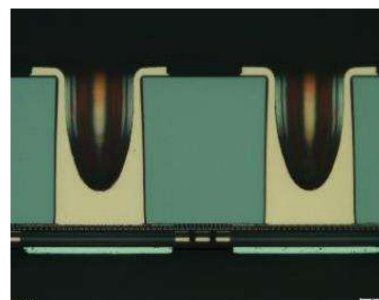


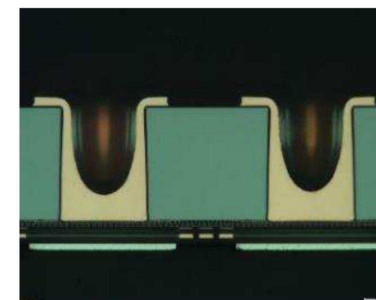




ATLAS FE-I4 after TSV process:
Cross section of backside TSV
Wafer thickness 100µm and 80µm





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# ATLAS FE-I4 TSV Hybrid Module Assembly

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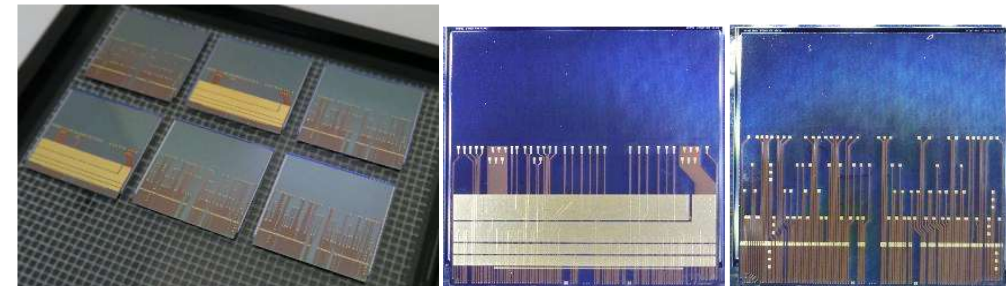
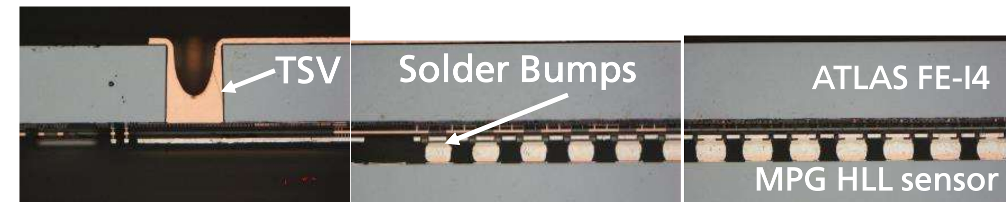
*1st Level Assembly Flip Chip Bonding to Sensor:*

- Assembly onto MPG HLL planar sensor
- Sensor with solder bumps



**Hybrid modules with ATLAS FE-I4 chip s on top:**
2 layer RDL connecting all WB pads for the power nets: VDDD, DGND, VDDA, AGND. Ni/Au layer pad metallization

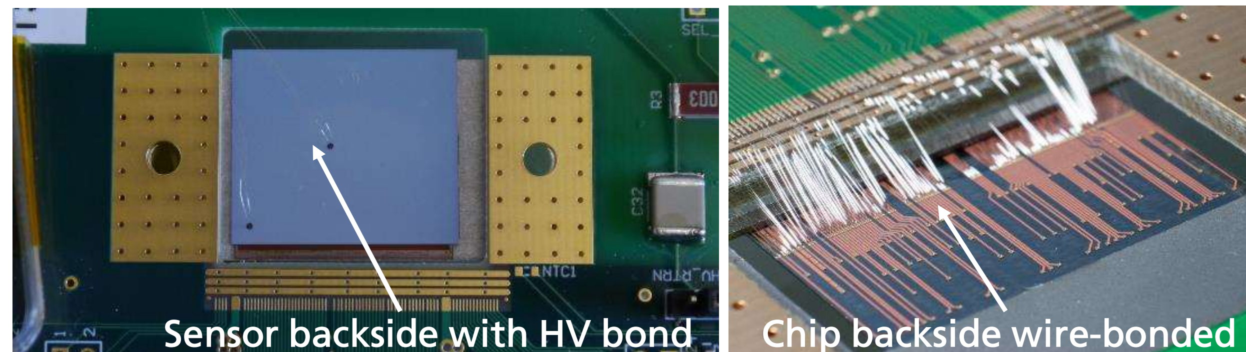



**Cross sections of hybrid module:**

80µm thick ATLAS FE-I4 TSV ROC top, MPG-HLL sensor bottom

*2nd Level Assembly at Bonn University:*

- Module Attach to PCB
- Sensor on top and HV wire bonded to frontside of the PCB
- FE chip connected via TSVs from the PCB's backside through a hole of the PCB

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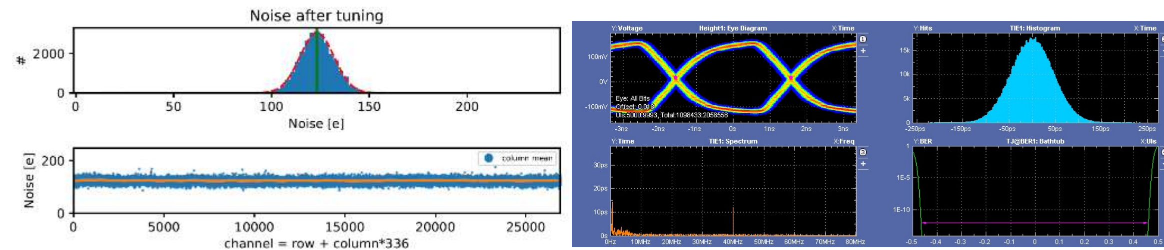
Images 2nd Level Assembly by Fabian Huegging @ Bonn University

# ATLAS FE-I4 TSV Bare Chip and Hybrid Module Test

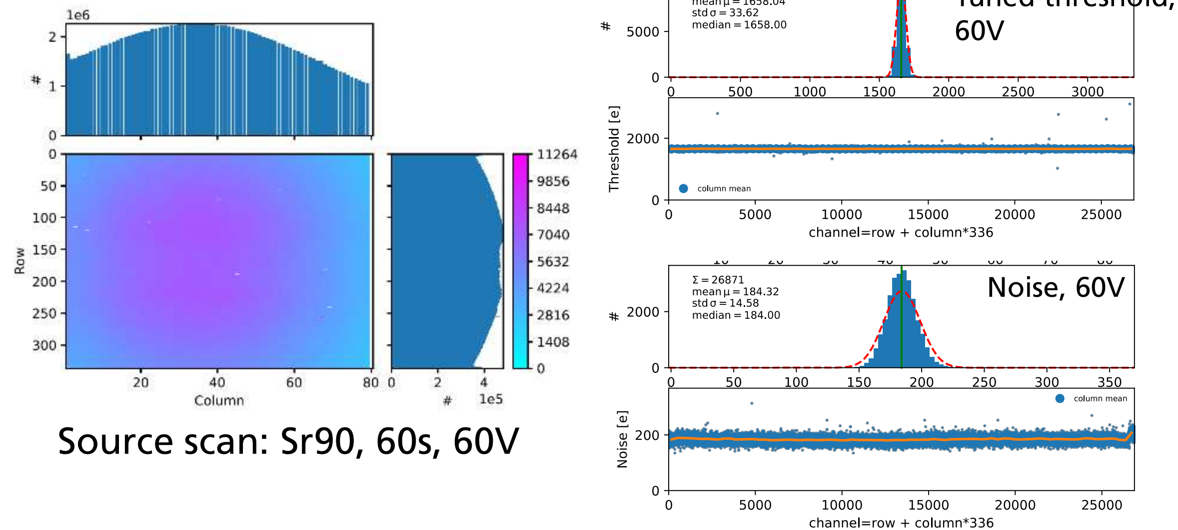
***Bare chips with both RDL types are working well*:**

- Performance in terms of threshold, noise, data transmission is similar to standard FE-I4B chips
- Noise of ~120e- at thresholds of 2000e-
- Data transmission at 160 MBit/s showed no issues with the additional capacitance load of the TSVs




***Hybrid Module Test (2 modules tested):***

- Both modules are working well
- Very good bump connectivity, one module shows a few disconnected pixel at one edge (maybe handling issues during BB)
- Noise is about 180e- at 1650e- threshold with a dispersion below 40e-




*F. Hügging et. al., Advanced Through Silicon Vias for Hybrid Pixel Detector Modules,* DOI: 10.1016/j.nima.2018.08.067

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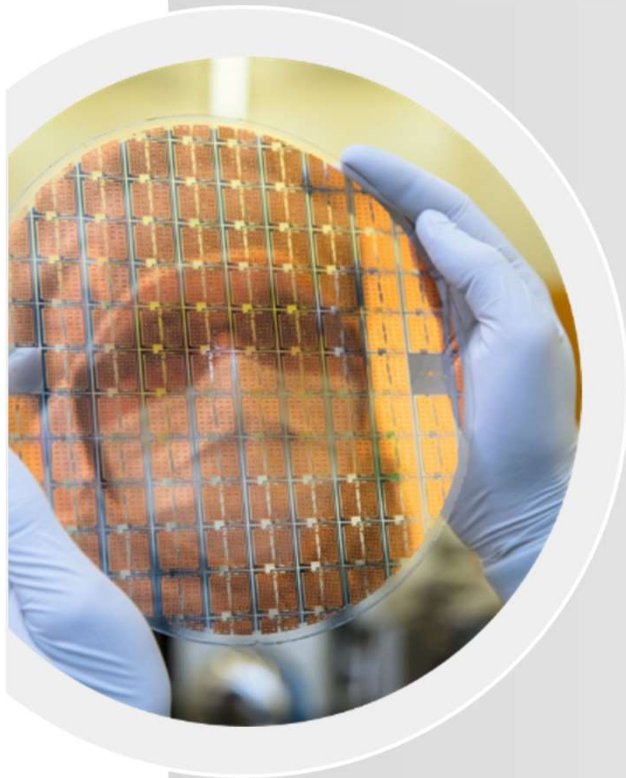
# Summary



- **Hybrid Detector Modules in HEP and Radiation Imaging**
  - Pixel Pitch 50µm → 20…10µm and even lower
  - Readout chip wafer now on 300mm
  - Bonding Temperature: < 100°C for High Z vs. high temp for thermo-compression bonding
  - From C2C, C2W to W2W Bonding
- **Interconnection Technologies:**
  - Reflow Soldering: Solder Bumps, Pillar with solder Cap
  - Solder Compression Bonding: Indium Bumps
  - Transient Liquid Phase Bonding / Solid Liquid Interphase Diffusion: CuSn, AuSn
  - Metal-Metal Diffusion Bonding: Au-Au, Cu-Cu, Nanoporous Gold (NPG)
  - Metal-Oxide Hybrid Bonding: Cu, Ni
- **3D Integration with TSVs**
  - TSV last wafer backside process with ATLAS FE-I4 ROC wafers
  - First functional ATLAS FE-I4 TSV modules

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# thank you for your attention

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