Report of the Final Design Review Part 2

ITk Strip AMACStar

Summary

The final design review part 2 of the ITk Strip AMACStar ASIC was held on July 24th, 2020 with Zoom connection. This report summarizes it and gives some recommendations.

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AGENDA AND AVAILABLE DOCUMENTATION

The agenda and documentation are available at: https://indico.cern.ch/event/932643/

REVIEW OUTCOMES (O: OBSERVATIONS; R: RECOMMENDATIONS; A: ACTIONS)

THE ACTIONS ARE REQUESTED TO BE IMPLEMENTED, WHEREAS THE TEAM MAY – AFTER CAREFUL CONSIDERATION – DECIDE TO IMPLEMENT OR NOT IMPLEMENT EACH OF THE RECOMMENDATIONS. THE TEAM IS ASKED TO TAKE NOTE OF THE OBSERVATIONS.

A FDR of the ITk Strip ASICs (ABCStar, AMAC and HCCStar) was held in July 2019, followed by a FDR-2 in November 2019 with focus on the ABCStar submission and AMAC design status. The FDR-2 of AMACStar (aka AMACv2b) is focused on the readiness of AMACStar for a submission, which is planned together with HCCStar later this year. The goal of this review is to identify actions and recommendations that the team will need to address for AMACStar in coming months, before the HCCStar is ready for FDR-2.

An updated specification document of AMACStar was made available before the review.

AMACStar design

O: The AMACStar has primary functions of monitoring with a 10-bit Wilkinson ADC, control and interlock. It will be used on the Strip Powerboard and PP2. Following recommendations in the November review, various changes have been implemented to improve the robustness against SEE, including triplication of almost all digital blocks, clocks and resets, switching to synchronous resets etc. To cope with the area and power (< 80mA from linPOL12V) constraints, some functionalities are removed (e.g. number of interlock channels generating flags is reduced to 12 from 16, replacing the window by single threshold), nominal clock rate is reduced from 40MHz to 20MHz.

O: A new analog function in AMACStar design is to monitor the supply current, which has a sensitivity of 6 ADC counts/10mA.

O: Reducing clock frequency of ring oscillator to 20MHz lowers the switching power by ~15mW. The current best estimate of the power consumption of AMACStar is ~30mA.

O: An external review of AM comparator has been organized with the support of CERN CHIPS service (Xavi Llopart and Rafael Ballabriga) in April. Various suggestions have been investigated, e.g. cross coupled current source, capacitance at node1, etc. It was concluded the design in AMACStar is robust with better temperature stability and will be kept as is. The team plans to check all analog signals in the final layout for unintended digital buffering by the silicon compiler, and cross check the extracted AM block simulation.

R: The team should verify the protection diode usage in the comparator design, which may introduce offset. The team should check the GF manual for the recommended implementation of the protection diodes.

R: After change of ring oscillator, a careful check of interface between blocks should be carried out. The team may seek support from the CERN CHIPS service (Xavi Llopart) for a better library characterization of some interfaces for full custom cells with Liberate AMS.

R: Interfaces between digital and analog IP blocks must be carefully verified, as this is often the cause of chips not working. It is recommended to make fast Spice simulations of all digital together with analog IP blocks to check basic interfaces. A special fast Spice exists for such simulations where detailed analog performance is not critical. More info on this can be given if needed (Jorgen Christiansen).

R: Since the ring oscillator is regulated by control voltage, the team should perform simulation to check the frequency changes at different conditions, e.g. after AMACStar powers up the power rail is close to 1.4 V, and after AMACStar is configured the power rail is at 1.2V etc.

R: Clock source (ring oscillator) is probably one of the main remaining problematic locations where SET can make the chip go crazy/stuck as digital blocks are now triplicated. SET injection simulations of this are proposed to check that the chip cannot get stuck in cases of glitches on the clock. As clock frequency is quite low it could possibly be investigated if the ring oscillator can be made SET immune by using R-C delays which are already part of the slowed down ring oscillator. This can be verified by injecting short SET current pulses in circuit and check if they are filtered by R-C delays. More info on this can be given if needed (Jorgen Christiansen).

R: The team should clarify if it is possible to reset stuck AMACStar chips without going through a power cycle.

R: The AMACStar has been simulated at corner temperatures between -40 ºC to +40 ºC. Since the AMACStar at PP2 will run in a system coolant which must be above the cavern dew point, so it's not going to be far below room temperature. PP2 also comprises a compact crate with a high power density. It is recommended that the likely AMACStar temperature in PP2 be reviewed to ensure it falls safely within the corner specification. If it looks to be close to 40 ºC one may wish to re-simulate the chip over a slightly wider range.

O: An external review of digital logic triplication has been organized with the support of CHIPS service (Szymon Kulis) in July. It was concluded that the TMRG tool has been used systematically for AMACStar and HCCStar, the general approach to SEE mitigation seems good. The potential issues and questions about the TMRG tool, triplication strategy and circuits have been clarified during the meeting.

R: For clock TMR fanout, the team should understand the impacts of the chosen fanout in terms of: 1) enabling/enabling clocks for production. 2) SEE robustness (the block itself and to pulses coming from the ring oscillator). 3) clock tree balancing between A/B/C branches. A set of scripts used to verify the triplication (https://gitlab.cern.ch/tmrg/tmrverif) has been forwarded to the team (Pedro Leitao).

A: eFuses has been used to define the chip serial number. The issue of eFuse for defining chip address needs to be clarified, what happens if eFuse reading becomes unreliable after TID, how to get out of "lock" states due to SEE. SEE simulations could be used to prove the recovery mechanism works properly. The team should check with the GBT team to clarify the eFuse issue that has been seen in GF 130nm technology. Can chip address be defined by wire bonding as a reliable emergency option? If this is not possible given various constraints (limited space on pad ring, limited space on Powerboard, impossible to set address before loading etc.), one shall check the potential failure modes and consequence, then develop mitigation measures and verify with radiation test.

R: Power estimate of AMACStar from Spectre simulation shows ~31mA current draw, which will be fully validated with AMACv2a lab measurements. The team should use Voltus to perform dynamic and static power analysis, check power grid and IR drop in the full chip, which will be

beneficial for the team to get familiar with the tool and set the flow for the HCCStar. A set of tutorials has been forwarded to the team (Pedro Leitao).

R: For the physical design of AMACStar, the team should verify that all reports, including the lint report from Genus is well understood.

AMACStar verification

A: Cocotb has been used for chip verification, which covers all of the functionalities in working conditions, and tests of radiation-hardness in terms of SEU and SET. Module level simulation will be set up with AMACStar, HCCStar and ABCStar, and results shall be presented in the HCCStar FDR-2. In addition, verification simulation of multiple AMACStar chips shall be carried out, since they will share a single bussed differential pair for command to/from AMACStar and this can't be tested with the current prototype.

O: Recent work on SEE simulations revealed one design vulnerability on endeavor internal FSM register and it was fixed. Overall the SEE simulation has increased the confidence in Star chips design.

R: The team should clarify what process corners are used for final verification simulations. It is recommended to use at minimum best, typical and worst corner cases. Best case is critical to verify possible hold time issues. Other corner combinations should be checked with static timing verification.

R: As digital blocks are now fully triplicated with triplicated clocks, simulation should be made where one of the three clocks is stopped and the chip should continue to work. This should be done for each of the three clocks.

AMAC testing and production

O: AMACv2a has gone through a slow (1.1kRad/hour) TID test at BNL for ~2000 hours, the current bump (from ~41.5mA to ~47.5mA to ~43.5mA) is comparable with previous AMACv2 test results.

O: Wafer probing of AMACv2a shows the average yield over 12 wafers is ~96% for Grade A dies which pass all vital functions tests and all performance functions tests, most failing dies are on the perimeter of the wafer as expected. All test data has gone through detailed analysis, and results are stored in the ITk Production Database.

O: AMAC has been exercised heavily during Powerboard tests, it has survived over 100 thermal cycles between +40ºC and -50ºC during the COVID-19 lockdown. All major circuits are exercised and work well, calibration procedures run and give good results. Zener diode has been added on the Powerboard to prevent large transients when rapidly turning off HV and avoid damage of AMAC. Main concern from the Powerboard side is to monitor AMAC current to stay below 80mA, which will be addressed in the AMACStar design.

O: AMACv2a has been used on all recent modules, all of the AMAC functionalities have been demonstrated at the module level. AMAC usage has also been validated on the stave. 14 powerboard stave demonstrated functionality of AMAC communications on the stave with lpGBT. AMAC monitoring has also been exercised during the stave testing.

O: AMACv2a functionalities have been successfully demonstrated for PP2 usage with an adapter board and GBTx test vehicle. AC coupling rectifier-based circuit has been verified for communication in both directions (controller <-> AMAC). A simple fix in software or firmware will be used to eliminate the erroneous bit being picked up. New version of the system will use lpGBT, and PP2 demonstration with lpGBT is expected in early 2021 after the EMCI board becomes available by the end of this year.

O: AMACStar will be produced together with HCCStar on the same wafers. Total production order of 56 wafers will give ~25,400 ASICs, to cover ~21,100 ASICs needed for module production and allow ~17% of production loss. QC includes TID and SEE irradiation tests, pre-irradiations of ASICs before will be carried out to mitigate TID bump. UPenn is the only probing site for AMACStar, plans for AMACStar production are well advanced.

CONCLUSIONS AND RECOMMENDATIONS

The review panel acknowledges the effort to produce the document and presentations, and warmly thanks the team for the well-prepared review, and the open and in-depth discussions. The AMACStar design looks good and solid, the team is congratulated for the progress made so far. The panel considers the review as **passed with recommendations**. The team shall clarify the impact of potential eFuse issue and mitigation measures, perform module level simulation and simulation of multiple AMACStar chips. Actions and recommendations should be addressed by the HCCStar FDR-2.