



# Mohammed Imran Ahmed

## 1 Some past background:

- 1 Graduated in July 2009 at Faculty of Biomedical, University of Luebeck, Germany
- 2 Master thesis topic: Volume estimation of object from an image using 3D Time Of Flight Camera.
- 3 Home country: India

## 2 Present status:

- 1 Host Institute: IFJ-PAN and AGH-UST
- 2 MC-PAD project: P10- Monolithic Detector
- 3 Supervisor: Dr. Henryk Palka and Dr. Marek Idzik
- 4 Thesis advisor and University: Dr. Marek Idzik, AGH-UST



# Contents

- Own work and Technical progress
- Milestones and Deliverables
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# Own Work and Technical Progress

- Test and Analysis of monolithic SOI pixel detector prototype INTPIX3 using ROOT (software developed at CERN)
- Test of back-gate effect on front-end electronics and confirmation that BPW(buried P-well) eliminate the effect.
- Test and measurement the detector with Am-241 source.

# Milestones and Deliverables



## (M)Milestones

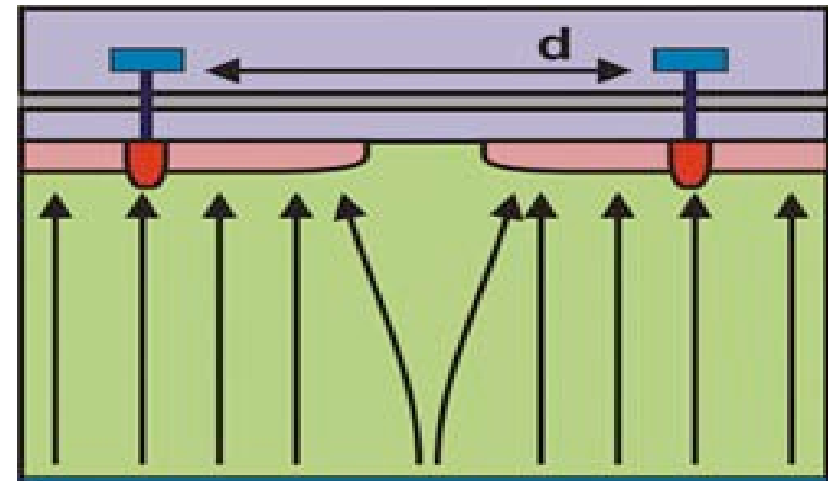
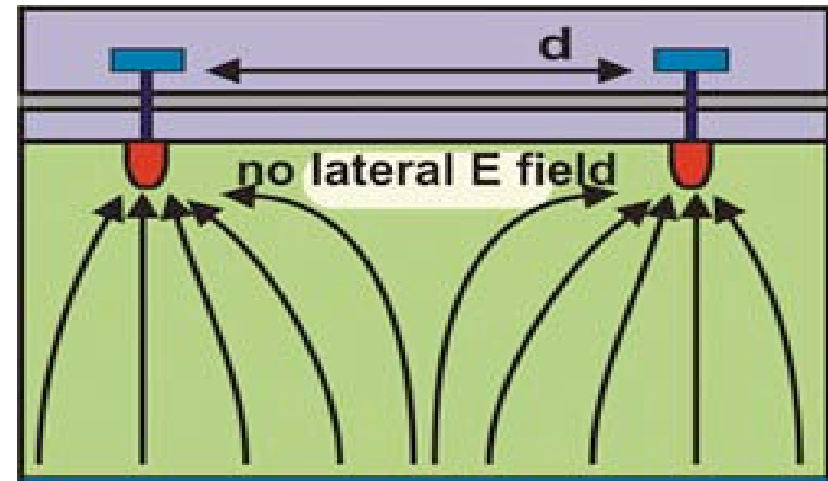
- MAPS SOI functionality (m25)
- MAPS SOI radiation hardness test (m31)

## (D)Deliverables

- MAPS SOI technology assessment (m12)
- Characterization of MAPS SOI prototypes (m24)

# BACK GATE EFFECT

- **Back-gate effect:** The top silicon circuitry is influenced by back potential, when back voltage is increased.
- As back gate voltage is increased the threshold voltage of NMOS transistors are decreased and PMOS are increased.
- **Buried P Well (BPW)**
- Introduction of BPW eliminate the Back-gate effect (can be seen in results).

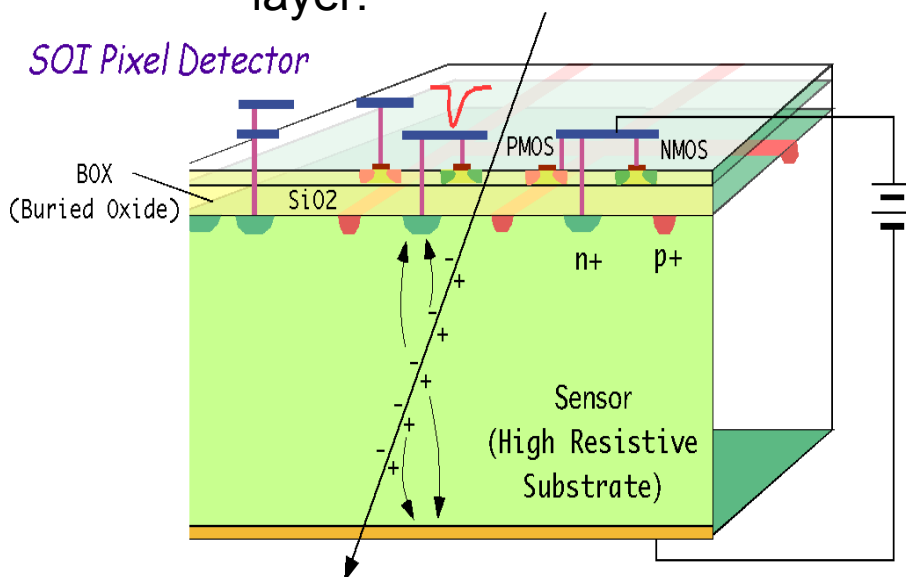


# Results

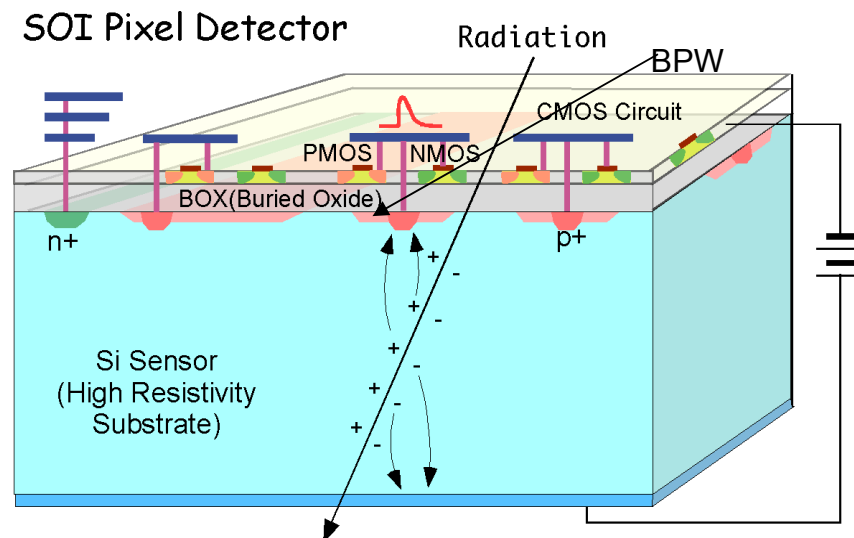
## (D)MAPS SOI technology assessment



- The back-gate effect was investigated in the last MPW run with INTPIX2 which effect the top Silicon i.e. front-end electronics of the detector.
- A Buried P-Well is introduced underneath the BOX (Buried Oxide) layer.



INTPIX2 without BPW



INTPIX3 with BPW

# Leakage Current

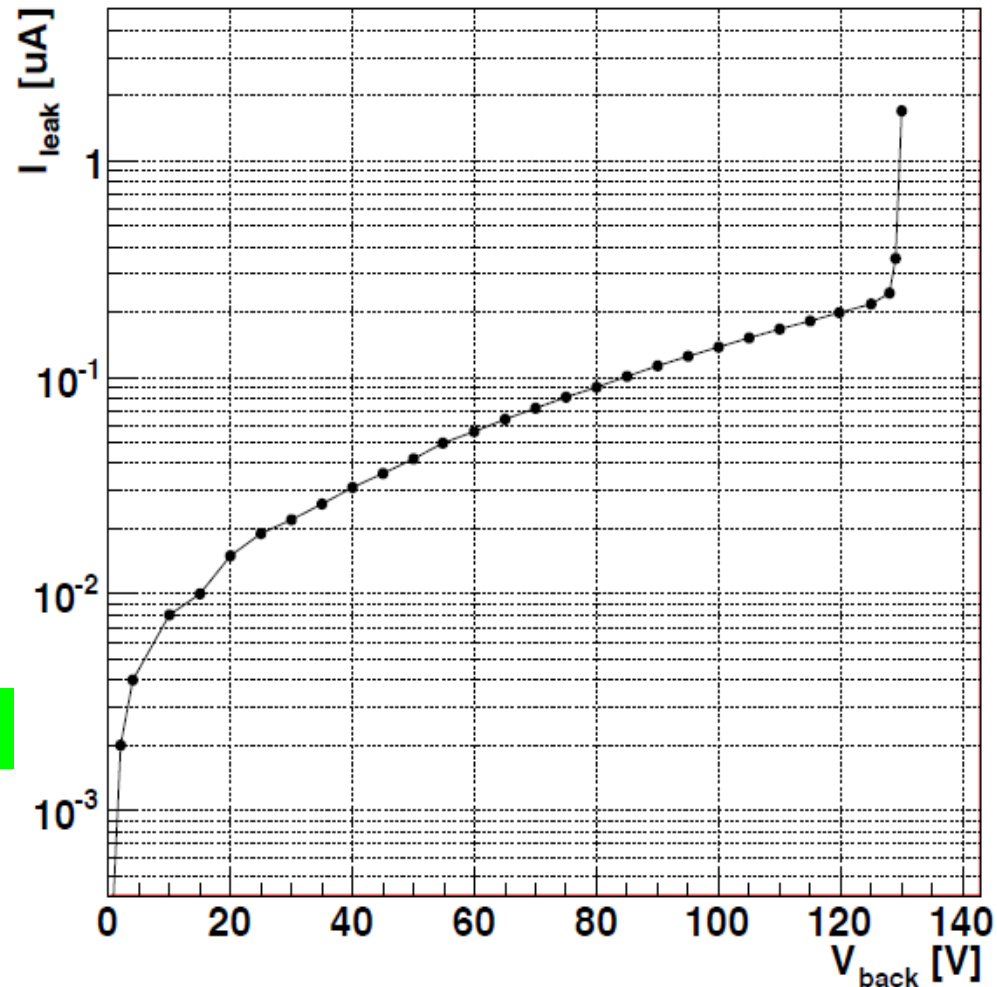


$$W_{calc} = \sqrt{\frac{2\varepsilon_S(V_{bi} + V_{back})\rho\mu_n}{qN_B}} = \sqrt{\frac{2\varepsilon_S(V_{bi} + V_{back})}{qN_B}}$$

$\mu_n$ : electrons mobility  
 $\varepsilon_S$ : silicon permittivity  
 $N_B$  = doping  
 $V_{bi}$  = V built-in  
 $\rho$  = Resistivity

$V_{back}$ (V)	$W_{dep}$ ( $\mu\text{m}$ )
0	10
10	45
20	64
30	78
50	100
100	141
120	154
200	199
250	223
300	244

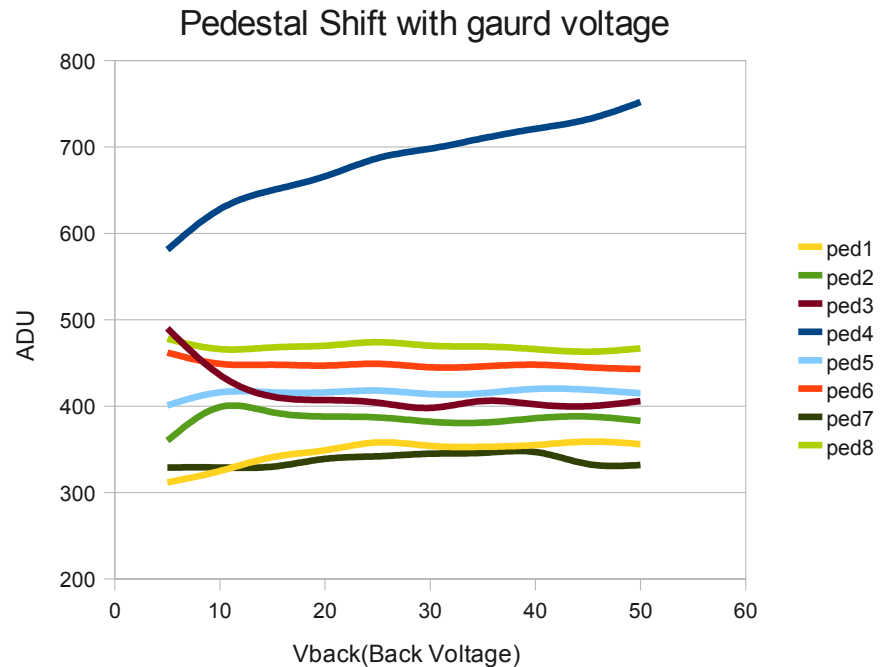
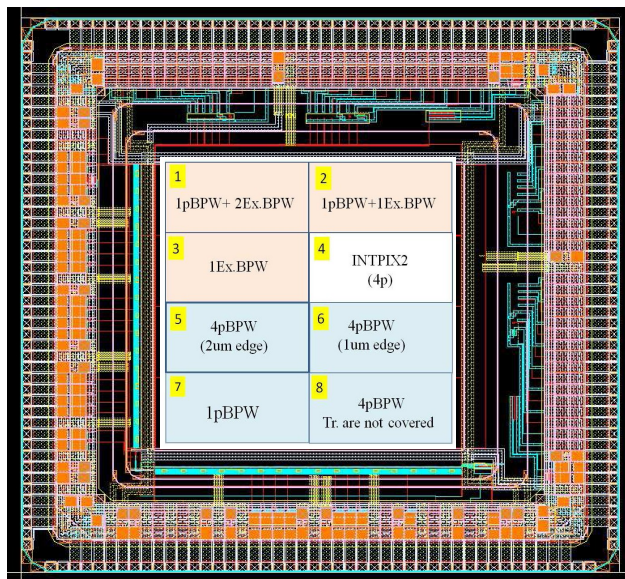
I-V characteristic (INTPIX3)



# Pedestal Shift



- Chip size 5x5mm, 128x128 pixels each of 20x20  $\mu\text{m}$ .
- 8 regions, 32x64 pixel each
- Each pixel has about 5 $\mu\text{m}$  square “no metal” window enable us to test with visible light laser.



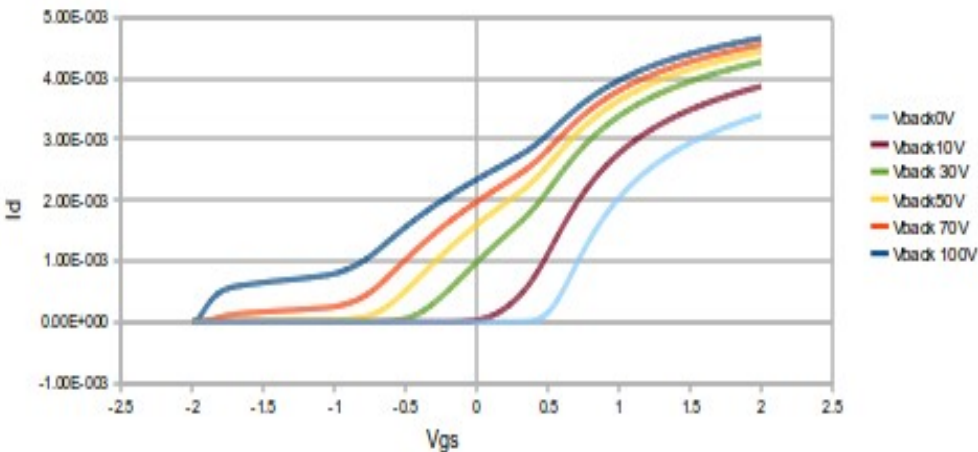


# Transistor Characteristic



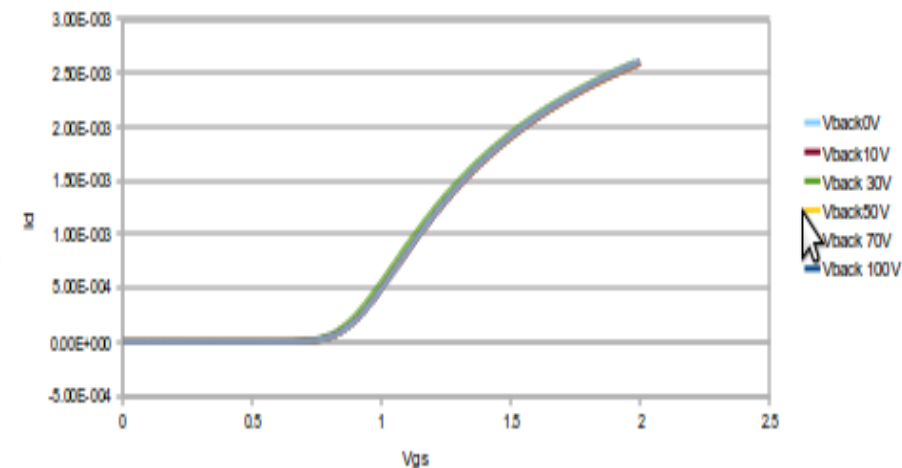
- $I_d$  vs  $V_{gs}$  characteristic of test transistor which shows the back-gate effect with and without BPW.

Pre Irradiation Nmos without BPW  
 $I_d$  Vs  $V_{gs}$  ( $V_{drain}=100mV$ )



Pre Irradiation Nmos with BPW

$I_d$  Vs  $V_{gs}$  ( $V_{drain}=100mV$ ,  $V_{guard1,2}=0V$ ,  $V_{bias}$  and  $V_{io}$  is ground)



- BPW removes the decrease in threshold with respect to back voltage.

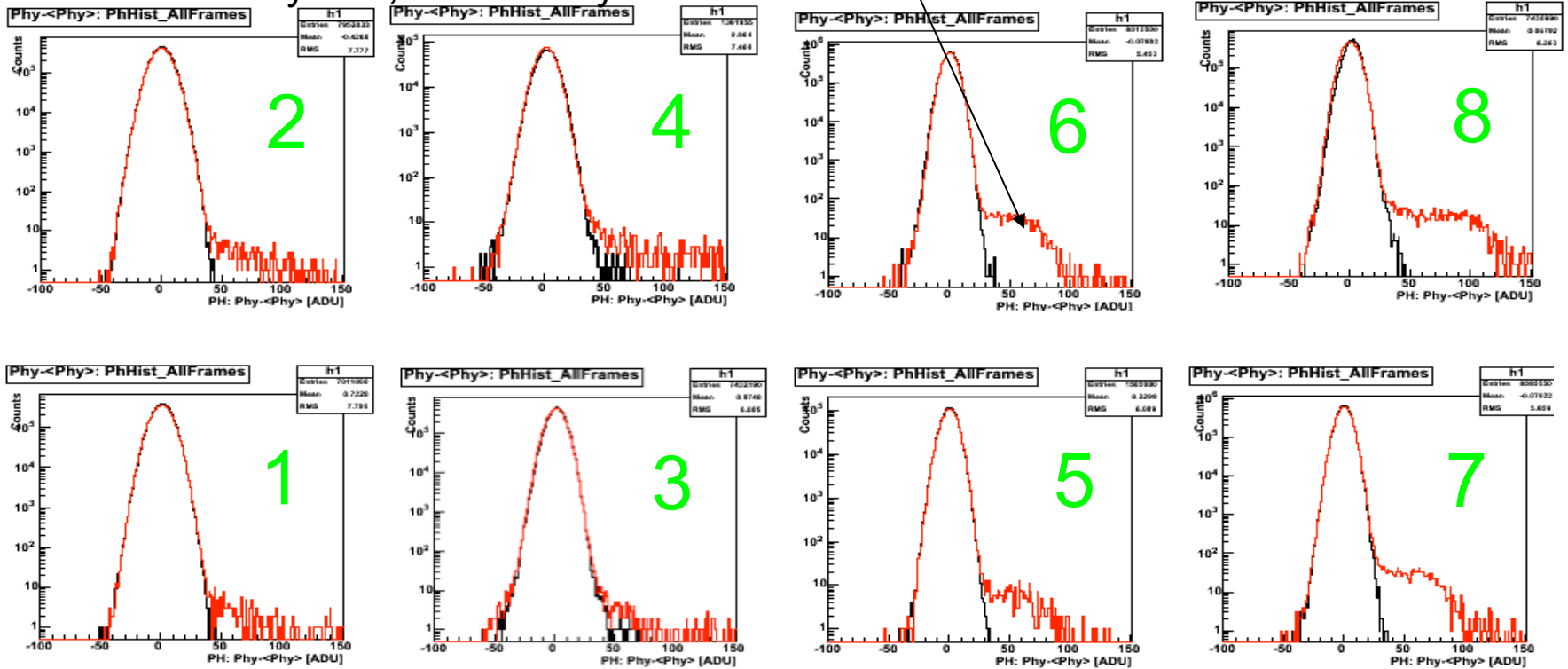
# Americium (Am-241)



## INTPIX3: Am-241(13.9keV)

Black- X-ray Off ; Red- X-ray On

One Block: 32x64 Pixel



$V_{back}/RSTV$   
100V/750mV

Exposure Time  
0.5ms/frm x 4900 frm

X-ray Source  
Am-241 (13.9KeV)

# Impact of my work



- **On me:** I learned new detector technology (SOI), got familiar with FPGA based readout electronics and learned ROOT
- **Science:** Monolithic SOI pixel detector is being developed to construct high granularity and thin vertex detector layers for Belle II experiment (starting from 2014) and for other experiment.

# Overview

## Training and Presentation

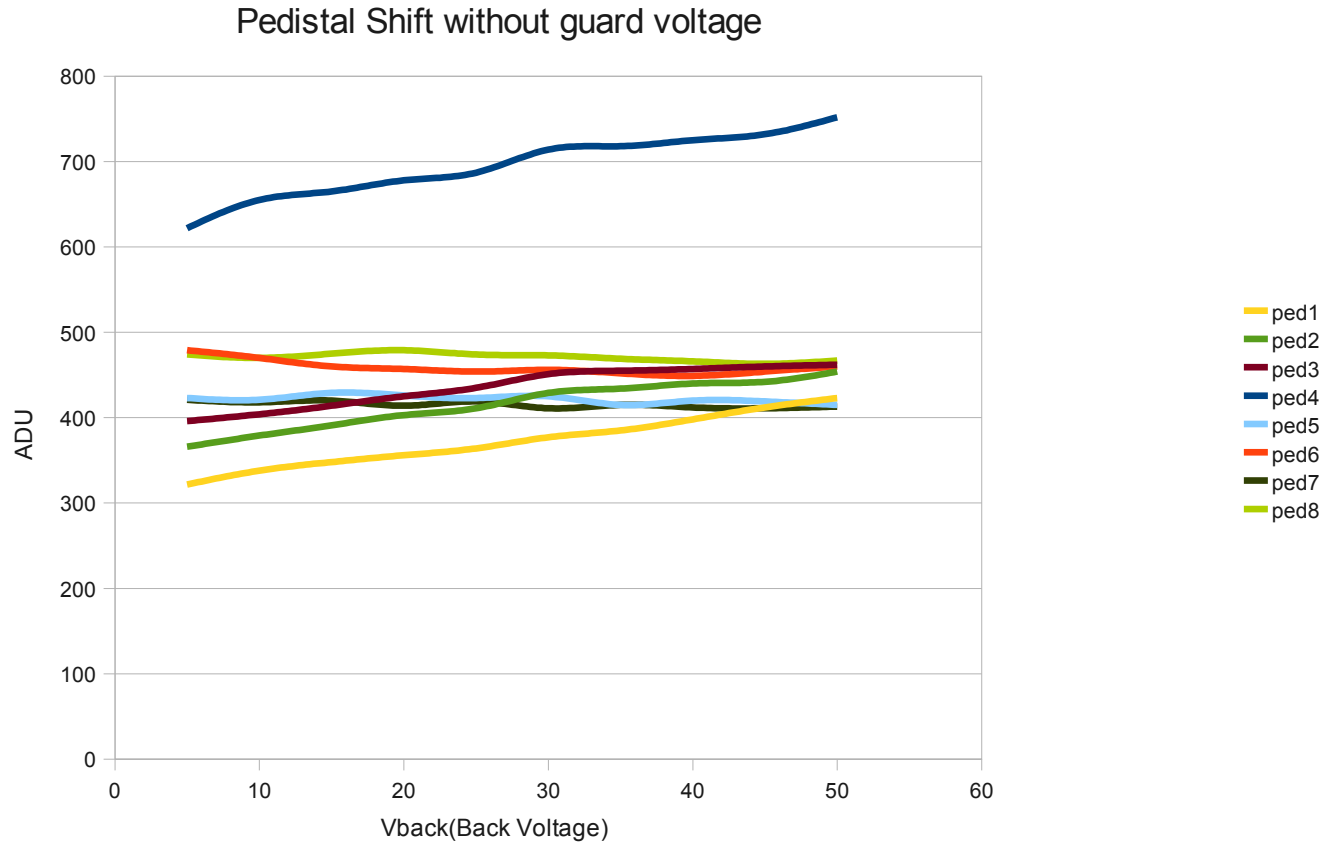


- **Courses:**
  - Polish language course
  - PhD related course work
- **Training Events:**
  - MC-PAD Training
    1. Readout Electronics in Krakow Poland
    2. Simulation and Data analysis in Hamburg Germany
- **Other Activity:**
  - Cloud Computing workshop in Krakow Poland
- **Presentations:**
  - FNAL SOI Collaboration Meeting 5<sup>th</sup> march 2010, talk on INTPIX3 back-gate effect test results.  
([http://www.fnal.gov/pub/today/archive\\_2010/today10-03-18.html](http://www.fnal.gov/pub/today/archive_2010/today10-03-18.html))
  - AGH-UST weekly group meeting talk on test results of INTPIX3.

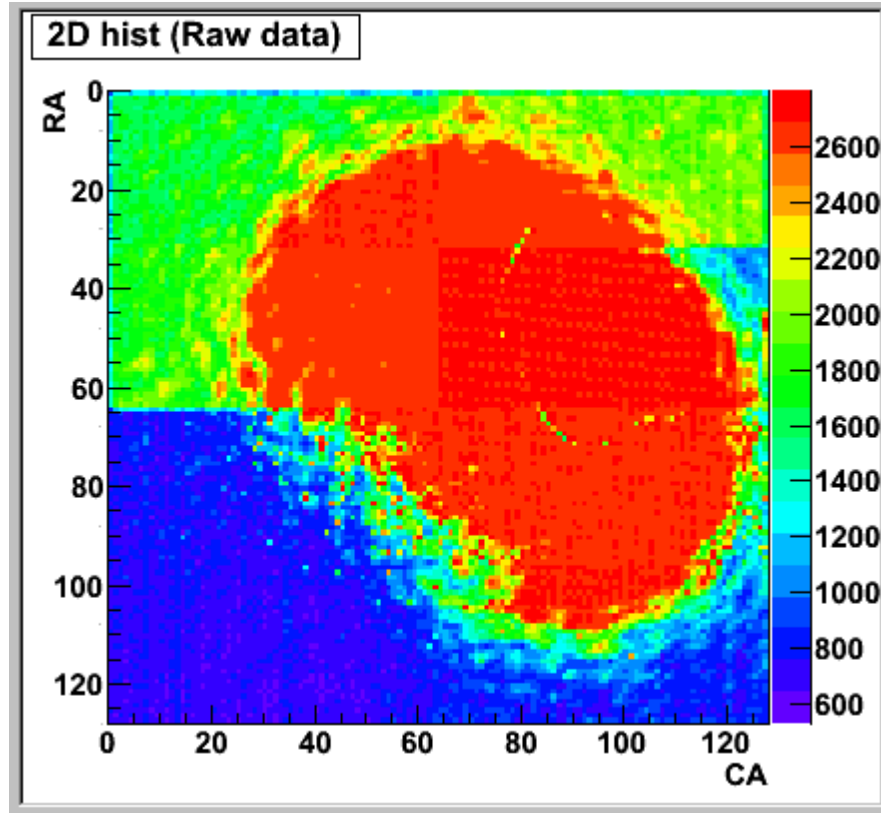


Thank you for your attention

# Backup



# Backup



Application of guard Voltages

# Backup

