Silicon detector processing and technology: Part II

Manuel Lozano CNM (CSIC) Barcelona, Spain







- Most simple detecting structure
- No segmentation
- Simple processing
- Direct connection to readout electronics
- **Guard ring is bisased at the same potential as central diode**





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- Initial wafer
 - FZ silicon <100>
 - N-type, 10¹² cm⁻³





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- **Field oxide 1,000 nm**
- Wet oxidation, 1100°C)





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$$\downarrow \downarrow \downarrow \downarrow UV radiation \downarrow \downarrow \downarrow \Box$$

1st Photolithography

Junction area definition





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- **SiO**₂ wet etching
 - Front and backside





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Photoresist removal





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- **Thin oxide growth**
 - Dry thermal oxidation, 36.5 nm





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N+ ion implant

□ 4.2×10¹⁵cm⁻², 100KeV

$\downarrow \downarrow \downarrow \downarrow \downarrow Boron \downarrow \downarrow \downarrow \downarrow$





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P+ Ion implant

□ 1×10¹⁵cm⁻², 50KeV



$\uparrow \uparrow \uparrow Phosphorus \uparrow \uparrow \uparrow$



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Impurity drive-in
950°C, 30 min





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2nd Photolithography

Contact opening



- Oxide wet etch
 - Front and back sides





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- Front side metal deposition
 - 1µm Al/Si/Cu (98.75%/0.75%/0.5%)





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3rd Photolithography

Metal patterning



Metal wet etching





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Photoresist removal





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- Back side metal deposition
 - 1µm Al/Si/Cu (98.75%/0.75%/0.5%)
- Metal sintering
 - **350°C, 20 min**
 - H₂/N₂ mixture (forming gas)





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Other types of detectors

- **We have seen the fabrication sequence for a very simple pad detector**
- There are other more complex detector geometries: Pixel and Strip detectors
- Pixel detectors are similar to pad detectors, but segmented in many individual diodes in a two-dimensional array
- Pixel size: 50 µm 1 mm. Number of pixels: 16×16 up to 256×256 (65,000!)



Strip detectors are by far more complex

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Strip detectors

- Diode shape: thin and long strips
 - Width: 20-100 μm
 - Length: 100 µm 20 cm (or more)
- Many channels in a single chip
 - From 10 to 1,000
- Wire bonded to read-out electronics
 - Hybrid or multichip approaches
- Applications
 - Particle tracking
 - Position measurement



- Diode: strips
- Bias: Polysilicon resistors
- <u>Coupling: AC</u>
- Position sensitivity
 - Resolution 5 µm
- Technological options
 - Single side, Double side







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Read out

chip

P-on-N strip detector fabrication technology





- Field oxide
 - 800 nm
 - 1100 °C



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- **1st Photolithography**
- **Definition of P⁺ junctions**
 - Wet etching
 - Photoresist etching



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- **Thin oxide**
 - 36.5 nm
 - 950 °C



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SiO₂

- **Boron ion implant**
 - 10¹⁵ cm⁻²
 - 50 keV



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- Phosphorus backside ion implant
 - 4.2 · 10¹⁵ cm⁻²
 - 100 keV
- Without mask



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D Polysilicon LPCVD deposition

- 600 nm
- 630 °C



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- Boron ion implant for poly doping
 - 1.5×10¹⁴ cm⁻²
 - 100 keV



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- **2nd Photolithography**
- Low resistivity poly region definition
- **Boron ion implant**
 - 10¹⁵ cm⁻²
 - 50 keV



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Photoresist removal



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- **3rd Photolithography**
- Polysilicon patterning
 - Photolithography
 - Dry etch
 - Photoresist etching



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Impurity activation

• O₂, 950 °C, 30 minutes



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4th Photolithography

- Contact definition
 - Wet etching
 - Photoresist removal



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Backside etching

- Front side protection with photoresist
- Poly etching
- SiO₂ etcihng
- Protective photoresist removal



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Front side metallization

- Al/Si/Cu
- 1.5 μm



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- **5th Photolithography**
- **Front side metal patterning**
 - Wet etching
 - Photoresist removal



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- Back side metallization
 - Al/Si/Cu
 - 1.0 μm
- Metal sintering
 - N₂/H₂, 350 °C, 30 minutes



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- Passivation layer deposition
 - SiO₂ 400 nm, PECVD
 - Si₃N₄ 700 nm, PECVD



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6th Photolithography

- Passivation layer patterning
 - Wet etching
 - Photoresist removal



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Strip detectors





RD50 wafer of baby strip detectors

ATLAS barrel module



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P-on-N technology

- **D** P junctions on N substrate
- It is the simplest and more used technology
- 6 photolithographic levels
 - P+ implant
 - Polysilicon
 - Low resistivity poly
 - Contact opening
 - Metal
 - Passivation
- Worse electrical performances
 - Hole collection in the amplifier

$$W = \sqrt{\frac{2\varepsilon_{si}\varepsilon_{0}V_{Bias}}{qN}} = \sqrt{\frac{2\varepsilon_{si}\varepsilon_{0}}{q}}\sqrt{\frac{V_{Bias}}{N}}$$





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Radiation damage

- Radiation sensors are subjected to radiation (obviously)
- Radiation causes damage in silicon:
 - Particles produce atom displacements
 - Create vacant-interstitial pairs (Frenkel pairs)
 - Also combinations of defects and clusters
- Increase of deep level and trap concentration
- Variation of doping concentration
 - Vacancies behave as donors
 - N-type substrate is less n and eventually becomes P-type
 - P-type is more P
- Increase of full depletion voltage
- Finally full depletion is not reachable and detectors have to operate in partial depletion
- Along with higher leakage current







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P-on-N technology and radiation damage

Shows the smallest radiation hardness

- N-substrate type inversion (to P type)
- Bulk inversion to p-type at around 2x10¹³ 1 MeV neutron equivalent



- After substrate type inversion junction moves from top to bottom
- Operation in partial depletion problematic
 - High resistivity zone close to electrodes

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N-on-P technology

- **N** junctions on P substrate
- No substrate inversion due to radiation
- Possible operation in partial depletion
- More radiation hard
- Electron collection
- Simple layout does not work due to inversion layer
- More complex technology
 - 7 layers
- Oxygenated P-type wafers difficult to process
- Still sufficient signal (7000e-) in p-type FZ strip sensors after 10¹⁶ neq/cm² for 900V







Insulation schemes in N-on-P

- All insulation schemes have pros and cons
- P-stop is the most reliable
 - Lower breakdown voltage
 - Noisy operation (microdischarges)
- P-spray
 - Reverse relationship between insulation and VBD
- Moderated p-spray
 - Intermediate solution
- Although it seems that N-on-P is the selected technology for upgraded experiments, insulation schemes is still a question under discussion





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N-on-N technology

- Before irradiation junction is on the back side
- Type inversion under radiation
 - Junction moves to the top surface
- The highest radiation hardness
- Accumulation layer on top side
 - No need for p-stops before irradiation
 - Needed after
- But, short circuit on the bakside
 - Located along the edges
- Need two side processing
 - Very difficult and expensive
 - 10 photolithographic layers
 - Also, difficult to test and bond





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P-on-N strip detector layout

P-on-N layout Simple strips





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N-on-P strip detector layout

N-on-P layout Similar to P-on-N But with P-stop structures between strips





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- Thick oxide growing
 - H₂0
 - 800 nm
 - 1100 °C



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- **1st Photolithgraphy**
- P-stops
- Wet etching
- Photoresist removal



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- **Front side Boron ion implant**
 - P-stops
 - 10¹² 10¹⁴ cm⁻²
 - 50 keV



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Back side Boron implant

- Backside contact
- 10¹⁵ cm⁻²
- 50 keV





- **Thick oxide re-growing**
 - 800 nm
 - 1100 °C



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- 2nd Photolithpgraphy
 - N+ junctions
 - Wet etching
 - Photoresist removal



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- Phosphorus implant
 - Strips junctions
 - 4.2 · 10¹⁵ cm⁻²
 - 100 keV



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 From this point the rest of the processing is similar to P-on-N devices

Photolithographies

- 3rd) Polysilicon
- 4th) Low resistivity poly
- 5th) Contact opening
- 6th) Metal
- 7th) Passivation



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- There is one standard technology missing to study
- N-on-N technology is very complex
- In P-on-N and N-on-P all the photolithographic processes are performed on the front side
 - (P-stops)
 - P+ or N+ implants
 - Polysilicon
 - Low resistivity poly
 - Contact opening
 - Metal
 - Passivation

- In N-on-N it is necessary to structure the backside, and there are 3 photolithograpic steps to be performed on the backside
 - P+ implants with SiO₂ mask
 - Contact opening
 - Metal
- It is necessary to use a double side aligner
- The cost is high, and it is not commonly used in LHC experiments



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Epilogue

- There are other advanced micro fabrication techniques:
 - RTP: Rapid Thermal Processing
 - CMP: Chemical Mechanical Polishing
 - Wafer bonding
 - DRIE: Deep silicon etching
 - Metal via formation
 - Bump bonding
 - DWA: Direct wafer attachment

- And many other advanced detectors:
 - Double side detectors
 - 3D detectors
 - Slim edge
 - Thin detectors
 - Trenched detectors
 - Depfets
 - MAPS

...

We had not time to study them today Maybe we can continue in another occasion



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