Silicon detector processing and technology: Part I

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Birth of Microelectronics

1947

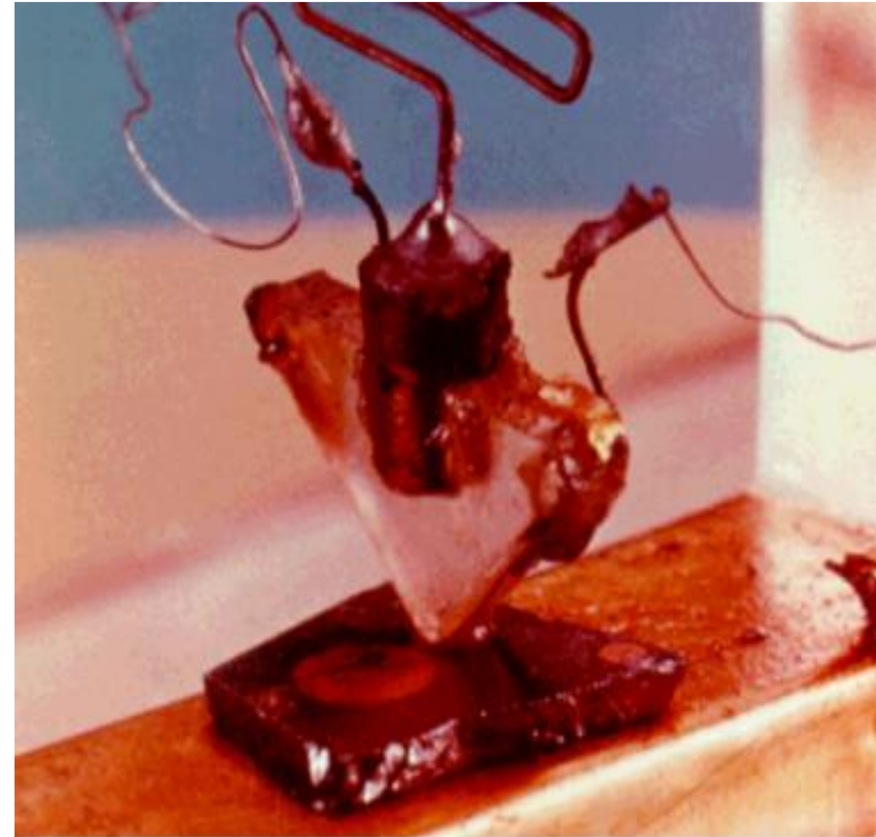
considered the born of Microelectronics

W.Shockley
J.Bardeen
W. Brattain

discovered the transistor effect in Germanium

First transistor

- **Original device**
  - **Bipolar transistor**
  - **Germanium N**
  - **3 electrodes**
  - **2 contacts metal-semiconductor like the used for rectifiers and another large area at the base**
- **Junction transistor development**
  - **Impurity diffusion techniques**
    - **Reduce cost**
    - **Increase reliability**
    - **Improve frequency response**



Integrated circuit

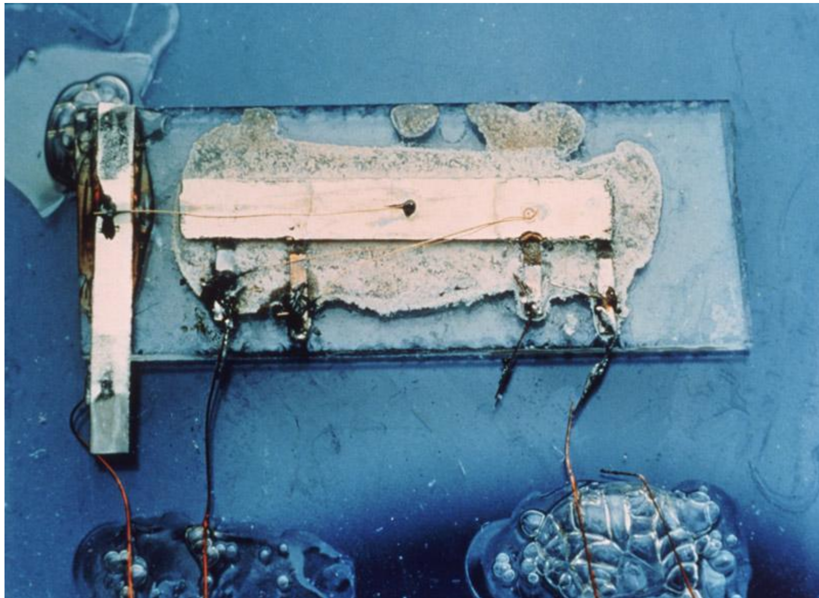
- **Planar technology development (1958)**
- **Processes to produce a large number of devices simultaneously on a wafer**
  - **Difusion, oxidation, deposition, photolithography**
- **Reduced cost**

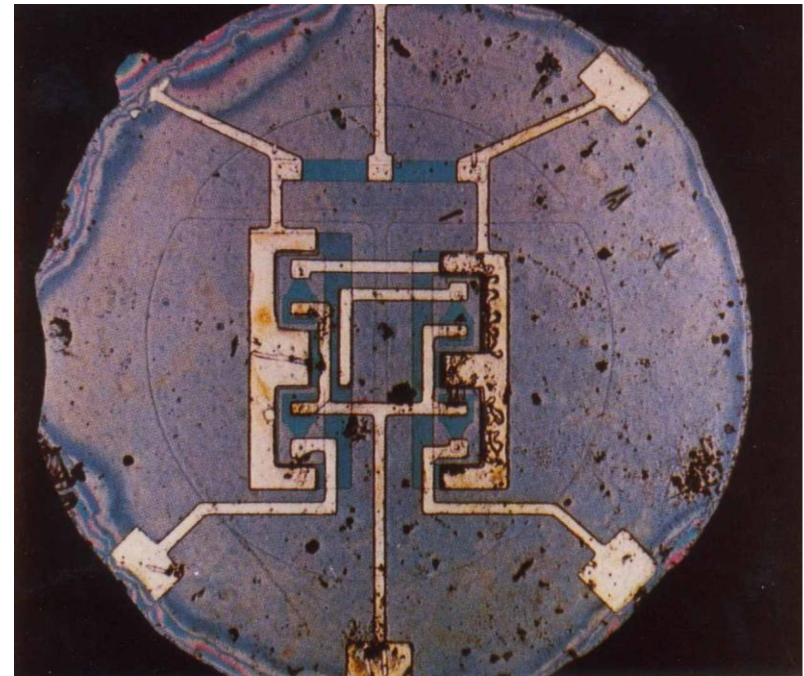
- **Silicon Valley birth**
  - **1957 Fairchild Semiconductors**
  - **1970 INTEL**
  - **...**

Integrated circuit: 1958

- J. Kilby, Texas Instruments
- made a circuit with transistors joined by metallic wires

- R. N. Noyce, Fairchild Semicond.
- first monolithic integrated circuit with devices isolated by reverse biased PN junctions and interconnected with aluminum tracks



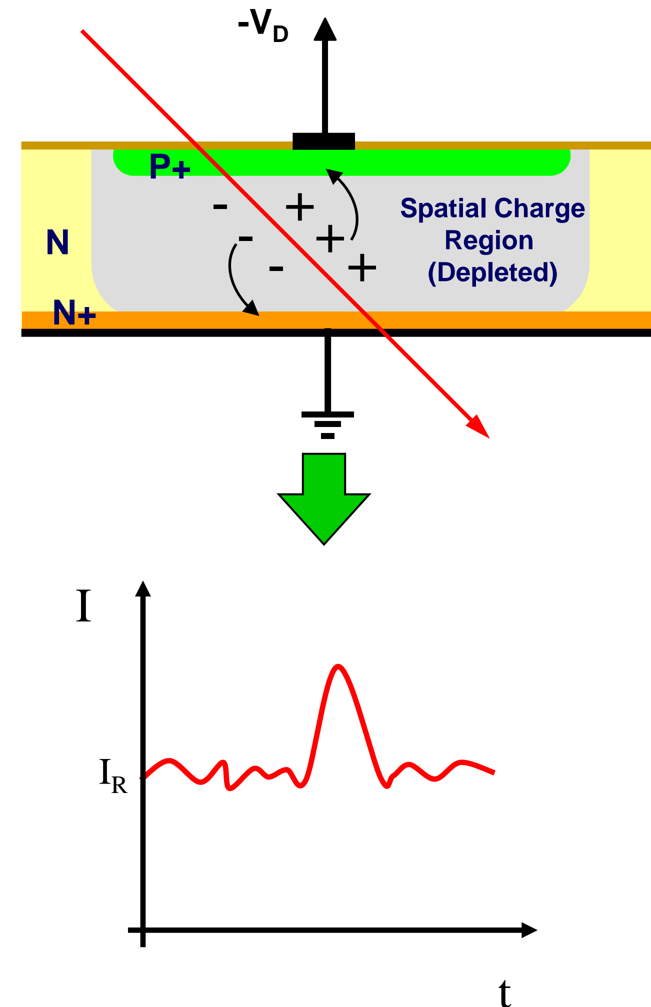


Particle detectors

- The same devices (and some new others) used in microelectronic industry can be used to detect charged particles and photons
- In 1980 J. Kemmer proposed the use of silicon devices for HEP experiments.
  - * J. Kemmer: “Fabrication of a low-noise silicon radiation detector by the planar process”, NIM A169, pp499, 1980
- The basic detecting device is a diode
- In 1990 pixel detectors were developed

Radiation Sensor – the concept

- **Radiation detection:**
  - **Reverse biased PN diode**
  - **Fully depleted so that the electric field extends to the full detector bulk**
  - **Maximize detection volume (~300 µm)**
  - **Need of very low doped Si for a reasonable depletion voltage (VD) and a low "dark current" (IR)**
  - **Radiation generates electron-hole pairs in the semiconductor**
  - **Charges drift to the electrodes under the electric field**
  - **Need to minimize recombination**
  - **Current pulse at the terminal**

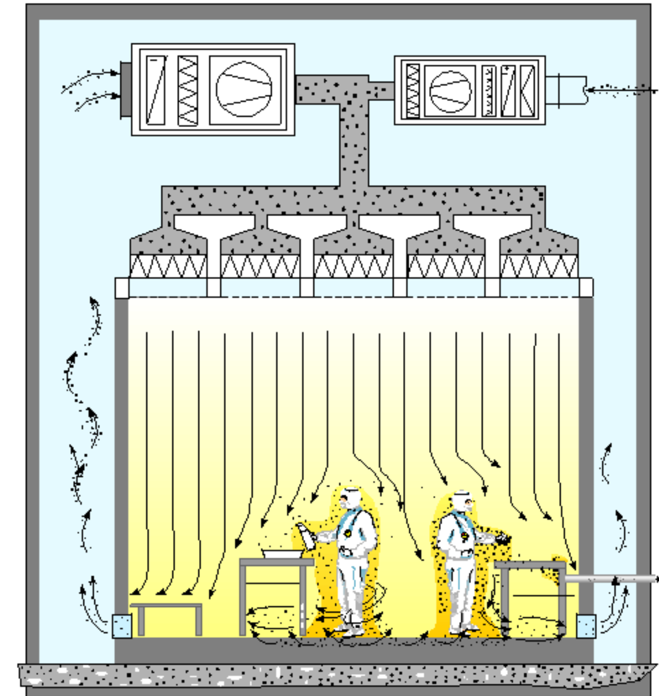


Fabrication processes

- Clean Rooms
- Substrates
  - Silicon wafers
  - SOI substrates
  - Epitaxial growing
- Junction formation
  - Thermal impurity diffusion
  - Thermal oxidation
  - Ion implant
- Dielectric and conductive layer formation
  - CVD layer deposition
  - PVD metal layer deposition
- Image transfer
  - Photolithography
  - Chemical wet etching
  - Chemical dry etching

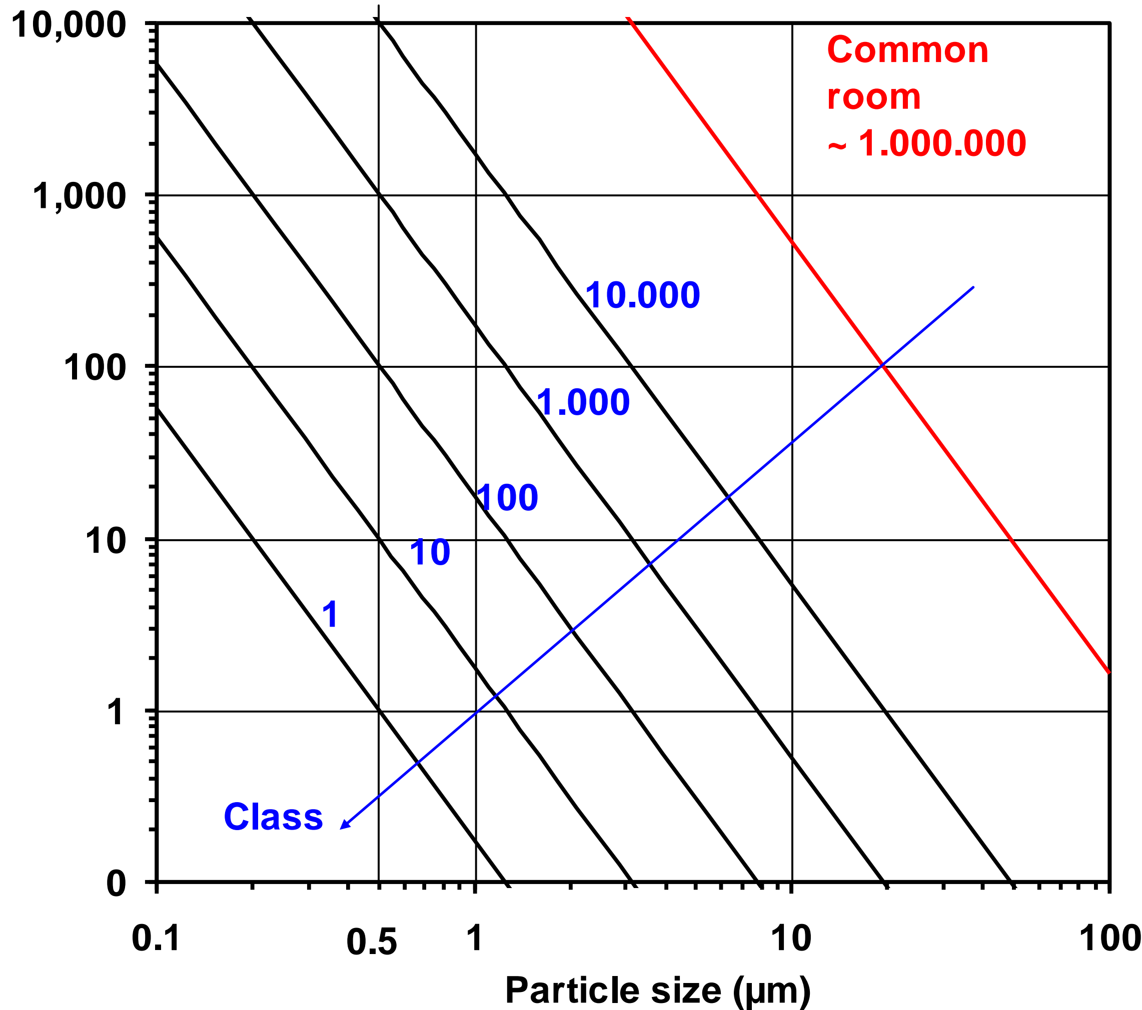
Clean Rooms

- **Control**
  - **cleanliness: dust particles**
  - **temperature: 21 ± 1 ºC**
  - **humidity: 40 ± 10 %**
- **Special clothings**



- **Services**
  - **Air conditioning**
  - **Compressed air**
  - **Vacuum**
  - **De-ionized water**
  - **Ultrapure gases**
  - **Waste treatment**

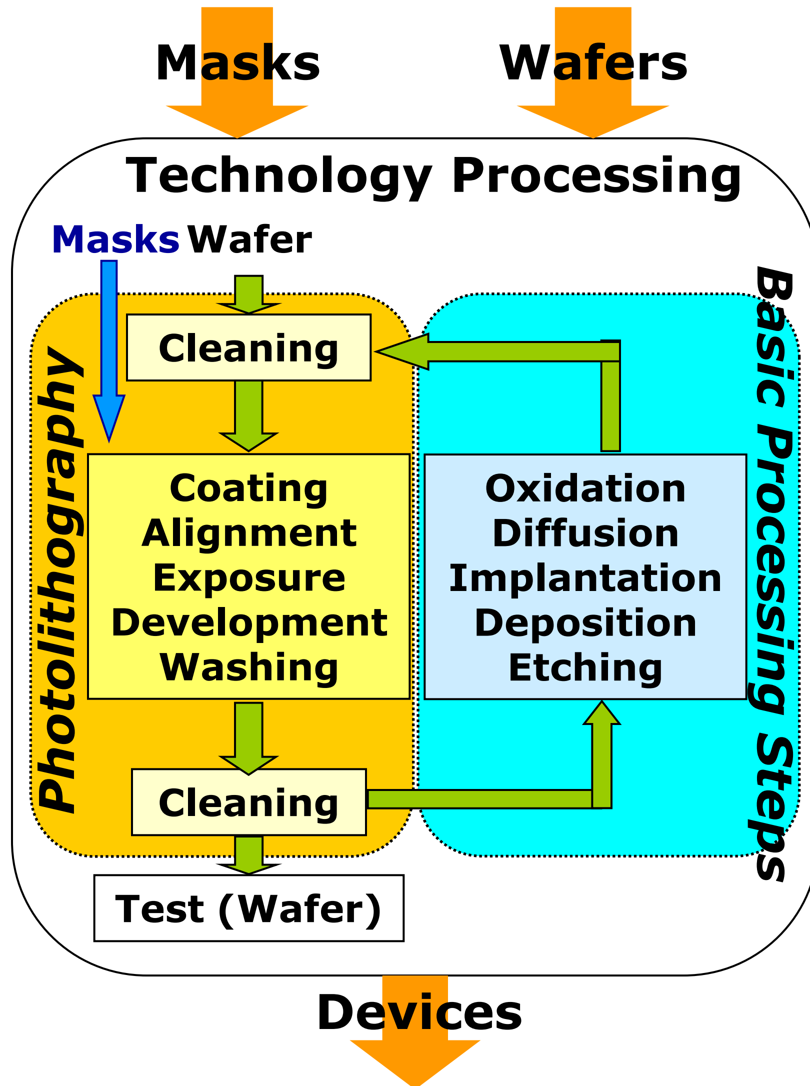
Clean Room class

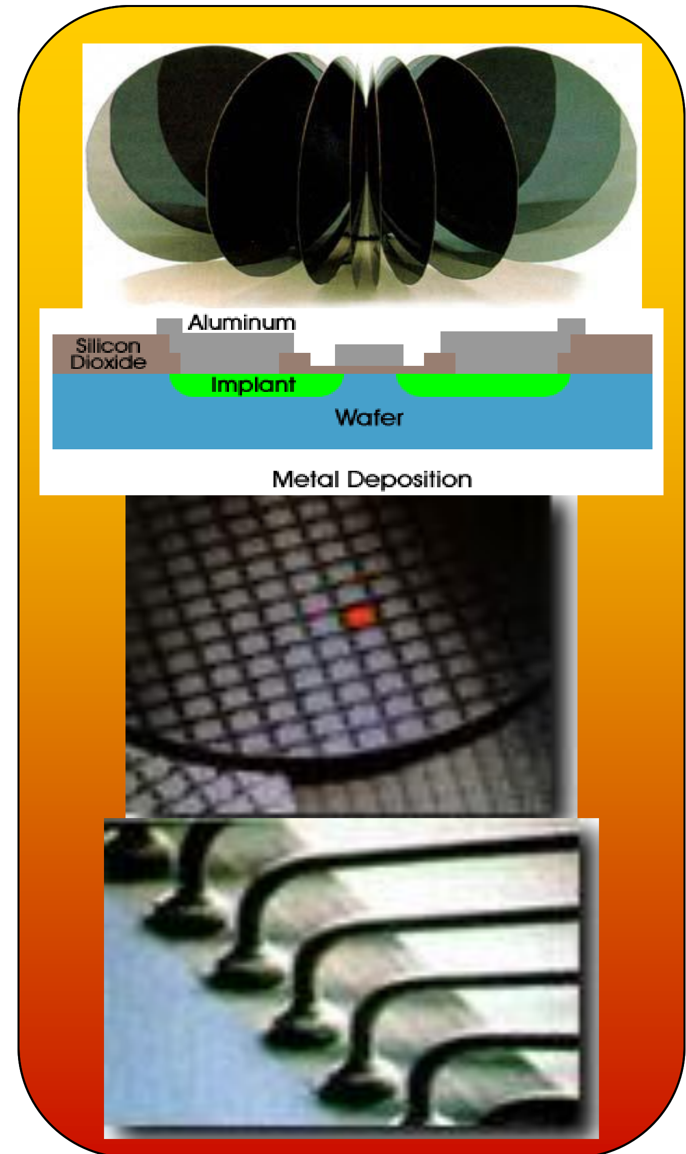


Equivalence

ISO 14644-1	US FED STD 209E	
ISO 1		
ISO 2		
ISO 3	Class 1	mid 90's
ISO 4	Class 10	beg. 90's
ISO 5	Class 100	mid 80's
ISO 6	Class 1,000	mid 70's
ISO 7	Class 10,000	
ISO 8	Class 100,000	
ISO 9	Room air	

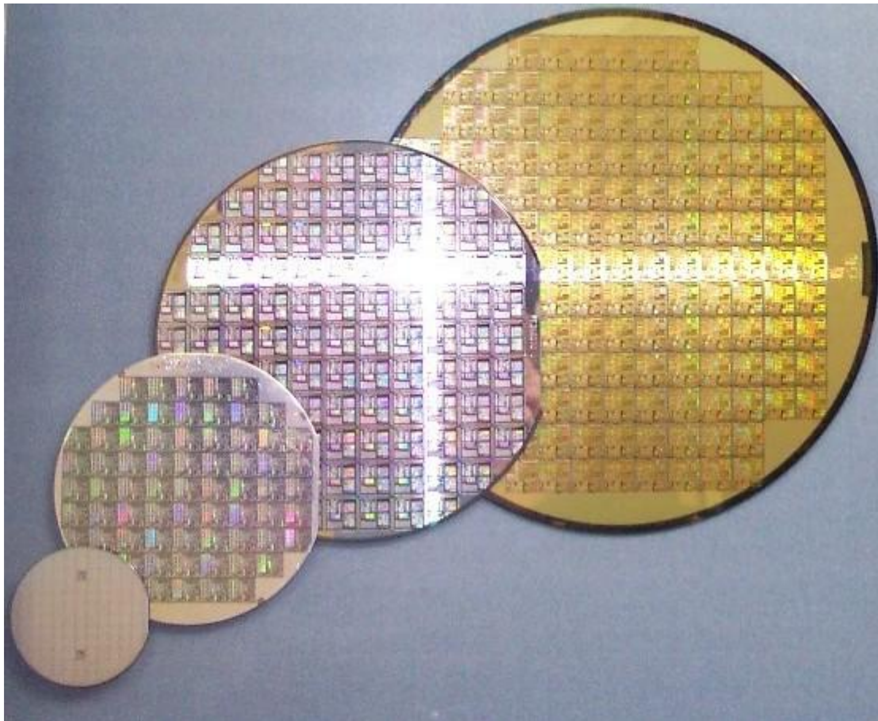
Basic fabrication processes





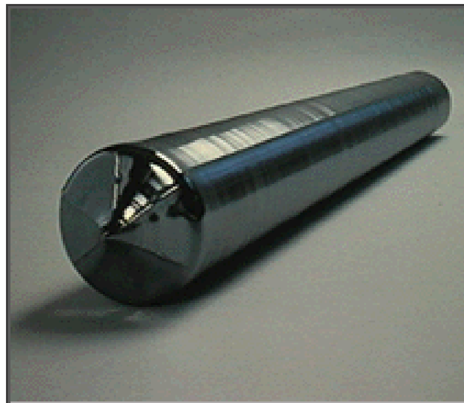
Silicon substrates

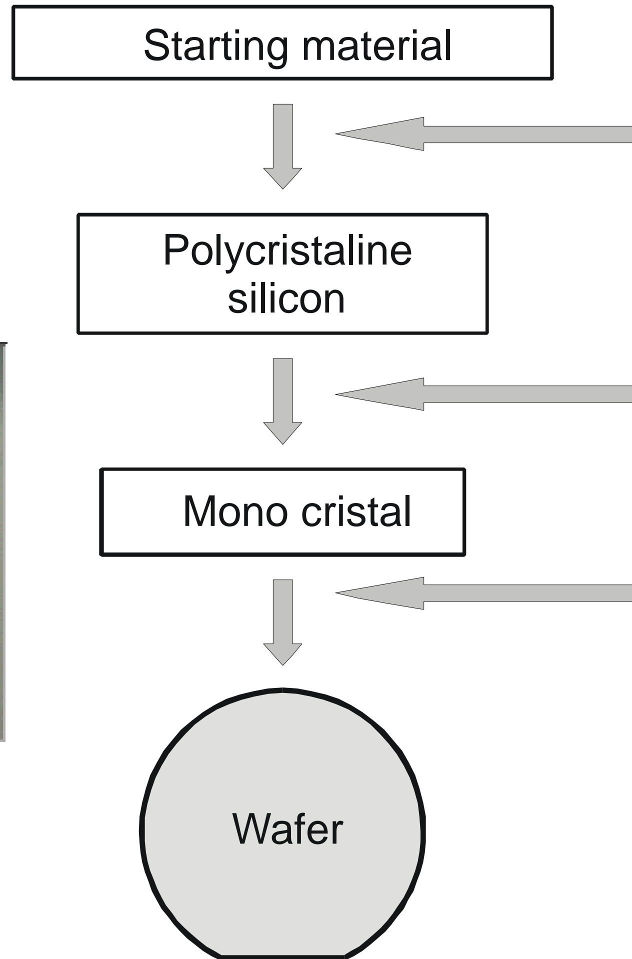
- **Silicon wafers**
  - **Monocrystalline silicon**
  - **Orientation: (100), (111)**
  - **Type (doping): P, N**
  - **Size: 10 (4''), 15 (6''), 20, 25, 30 cm**



- **Fabrication method**
  - **CZ (Czochralski)**
    - **Res: 0.002 - 50 ohm*cm**
    - **Dop.: 1e14 - 1e19 cm-3**
  - **FZ (Floating Zone)**
    - **Res: 20 – 10,000 ohm*cm**
    - **Dop.: 5e13 - 1e15 cm-3**
- **Problems**
  - **Impurities**
    - **Oxygen < 1e14 cm-3**
    - **Carbon: 1e12 - 1e14 cm-3**
    - **Heavy metals**
  - **Doping variation**
    - **Wafer to wafaer**
    - **axial inside wafers**
- **Gettering:**
  - **Impurities and defect deactivation**

Wafer fabrication





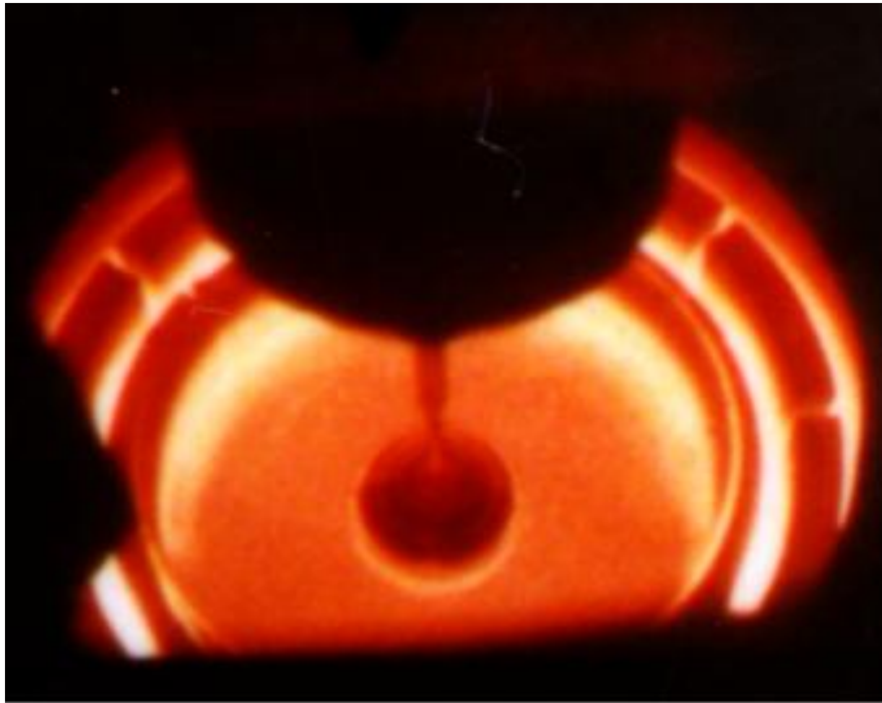
Si	GaAs
SiO2	Ga, As
Distillation and reduction	Synthesis

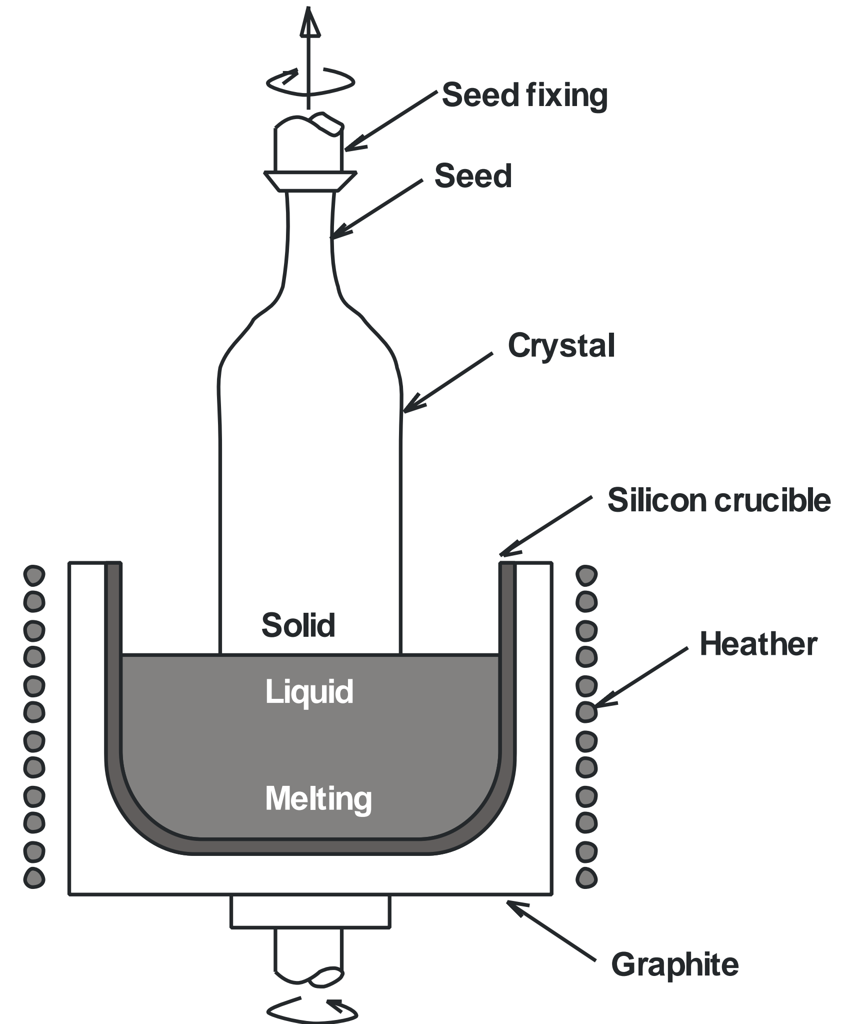
Cristalline growing

Shaping, Cutting Polishing

Wafer fabrication: Czrochralsky Method

- Pure silicon is melt in a crucible
- Pull Si crystal seed from the melt, as Si solidifies, the crystalline orientation is kept.



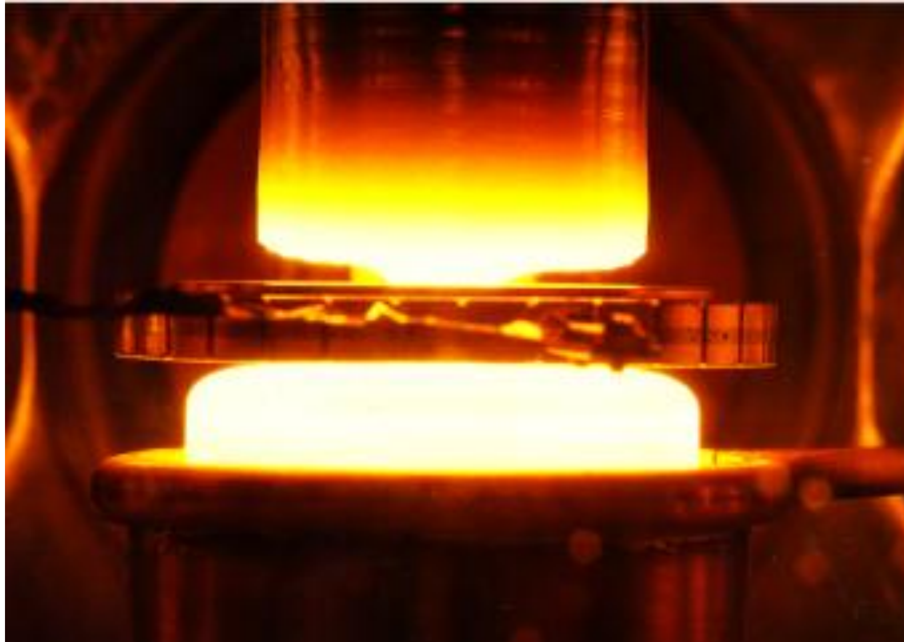


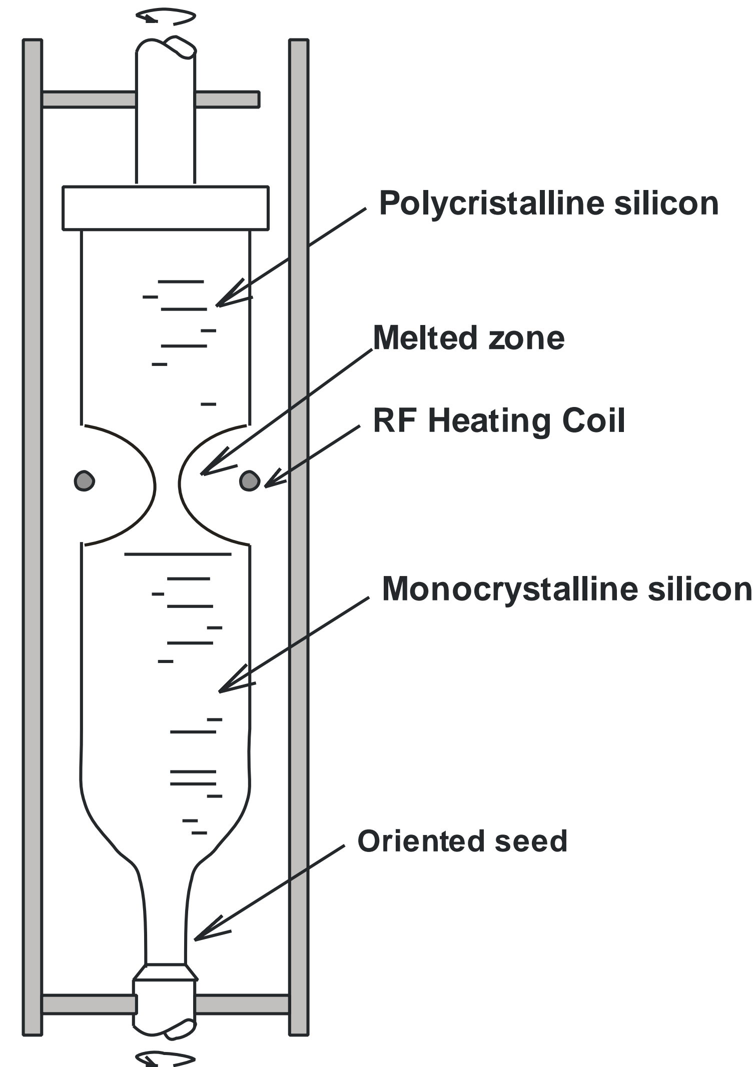
Wafer fabrication: Czrochralsky Method

- **Fused silicon is in contact with crucible: Dissolves oxygen from silica and also other impurities.**
- **CZ-Silicon is not suitable for very low doping (<10^{13} cm^{-2}), or conversely, for very high resistivities, as needed for particle detectors**
- **CZ is the most common method used by IC industry, and therefore cheap (10 cm wafer < 50 €)**
- **Use of magnetic fields can help in containing impurities far from solidifying surface. Since few years there are CZ available in sufficiently high purity (resistivity) to allow for use as particle detector. The technology is named Magnetic Czochrlasky (MCZ).**

Wafer fabrication: Float-zone Method

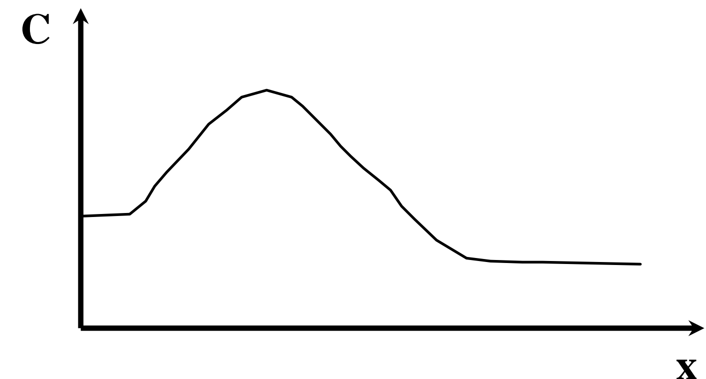
- **Silicon ingot is passed through a ring-shaped furnace. Silicon melts locally, impurities are segregated to the melted zone, and is purified.**
- **Several passes are possible, achieving ultra high purity.**



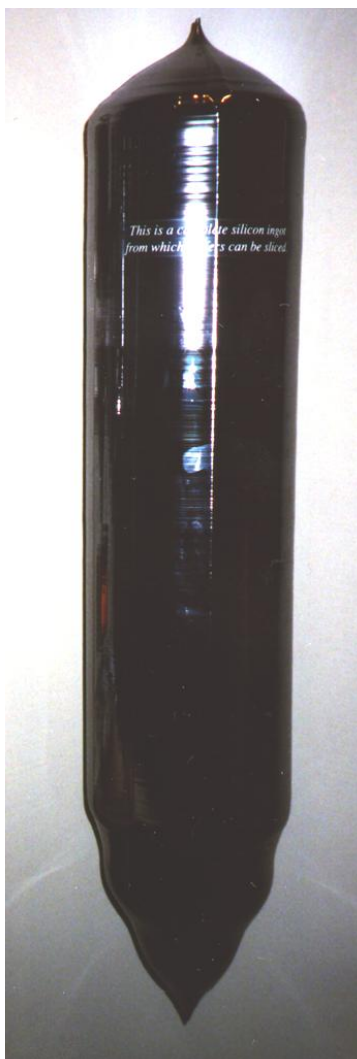


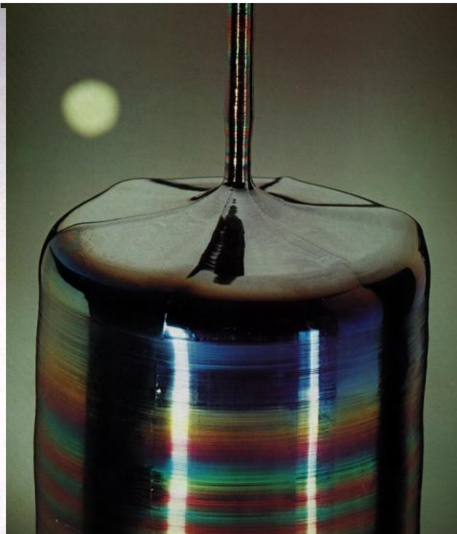
Epitaxial growth

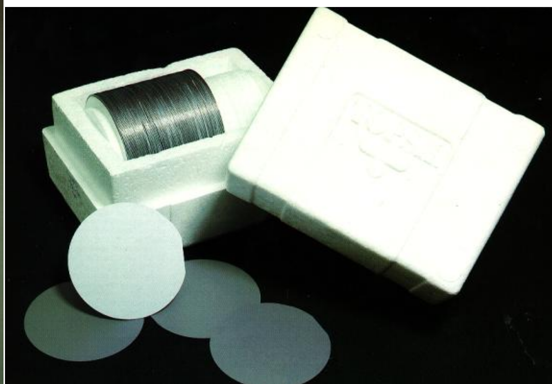
- **Monocrystalline silicon growth over Si wafer.**
  - **Growth rate about 1mm/min**
  - **excellent homogeneity of resistivity**
- **Main application:**
  - **High resistivity silicon over low resistivity substrate**
  - **Highly doped buried layers (same or different type)**
- **High temp. process**
  - **950 - 1250 ºC**
- **CZ silicon substrate used ⇨ in-diffusion of oxygen**
- **up to 150 mm thick layers produced**
- **price depending on thickness of epi-layer but not exceeding 3 × price of FZ wafer**

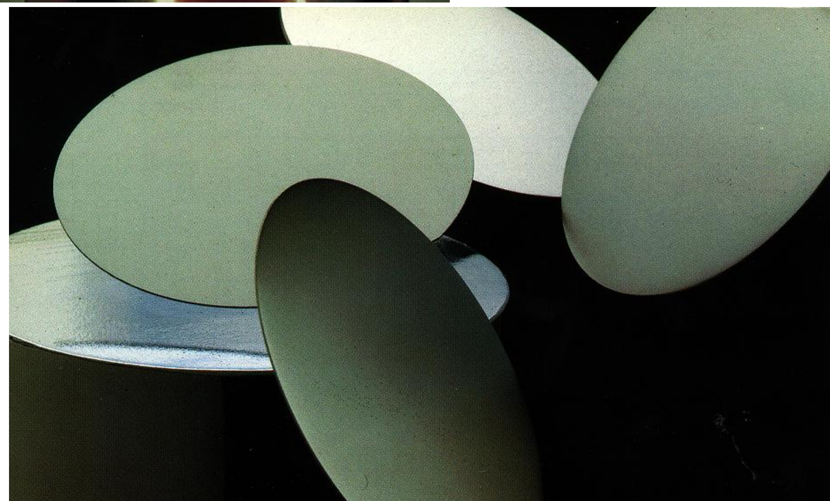


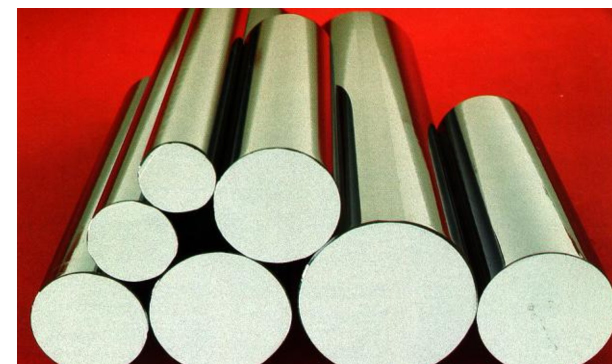
Images of wafer fabrication



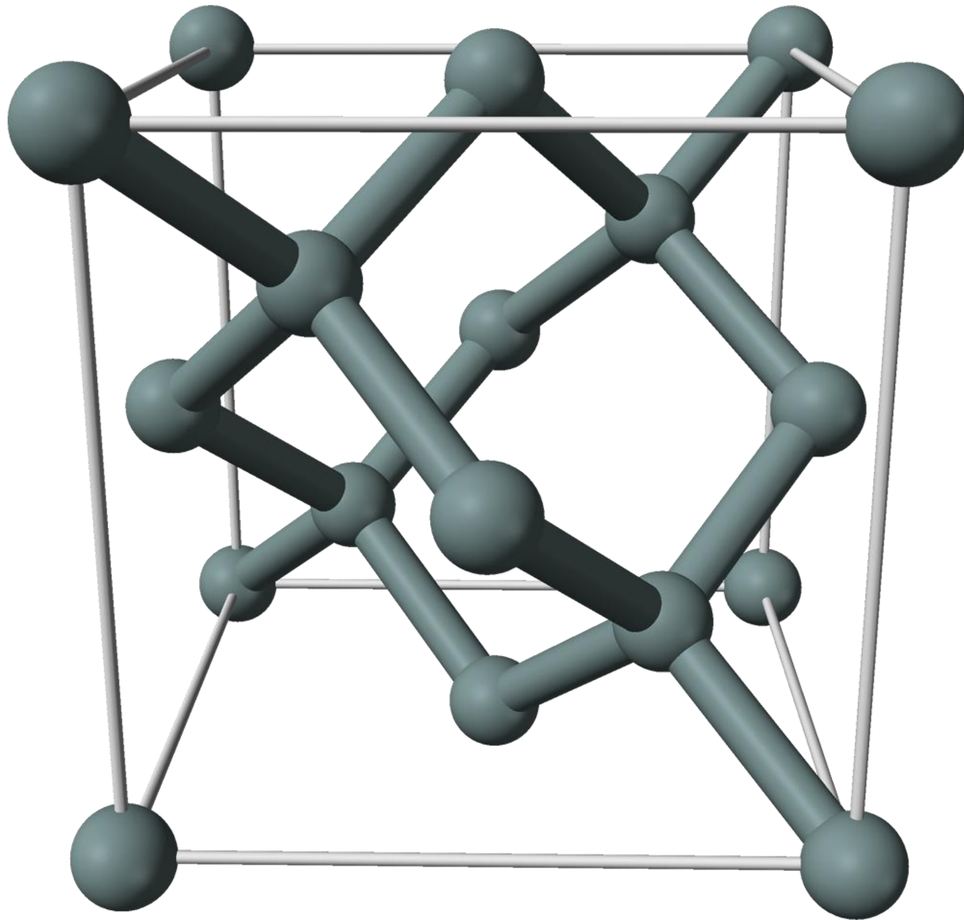


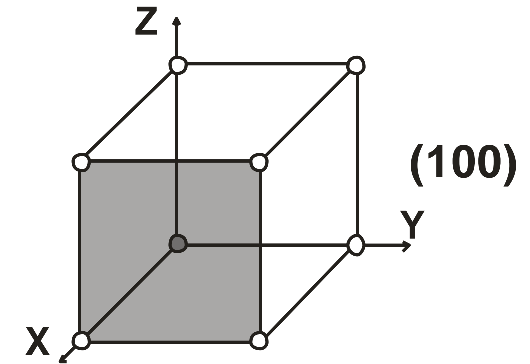


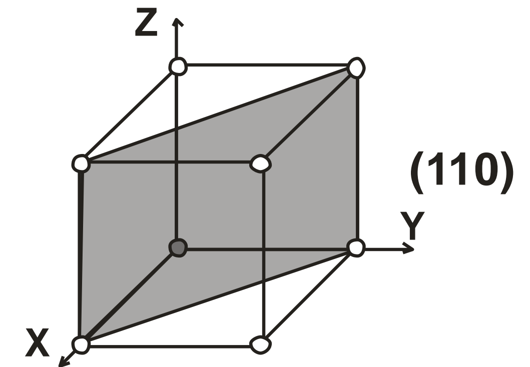


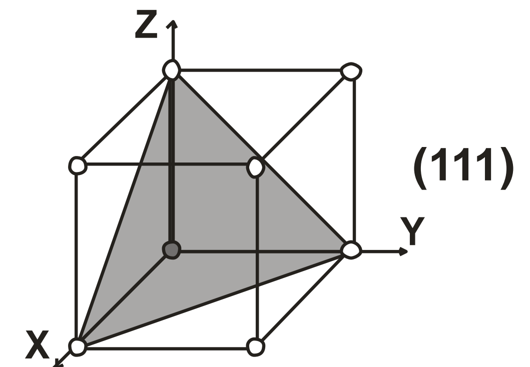


Silicon crystal lattice

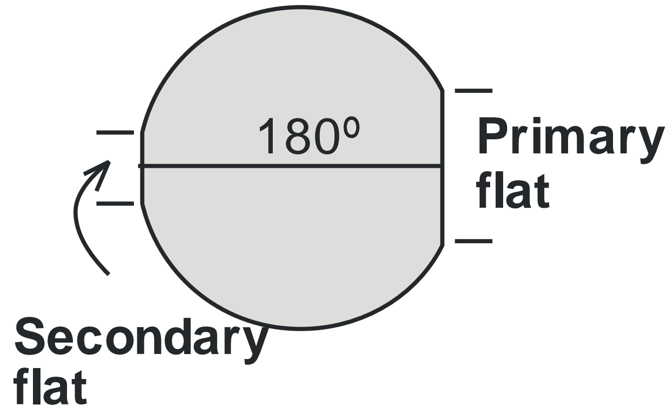


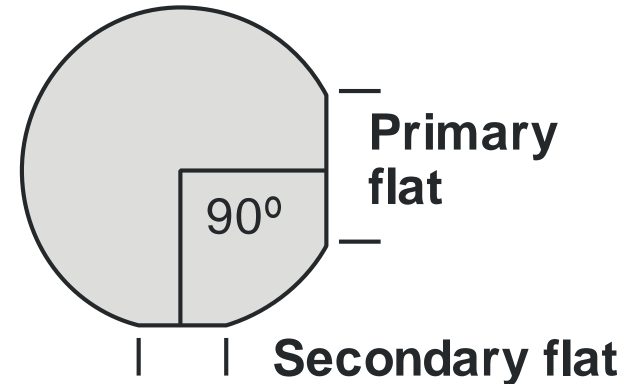


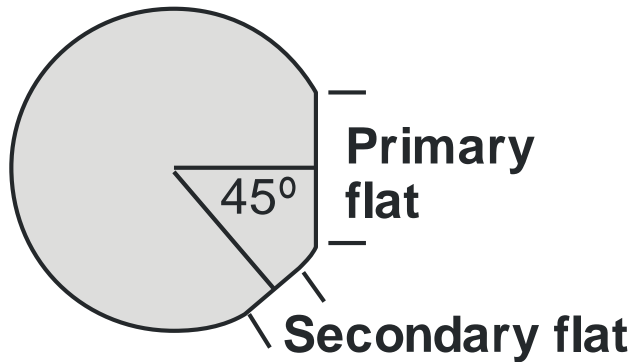


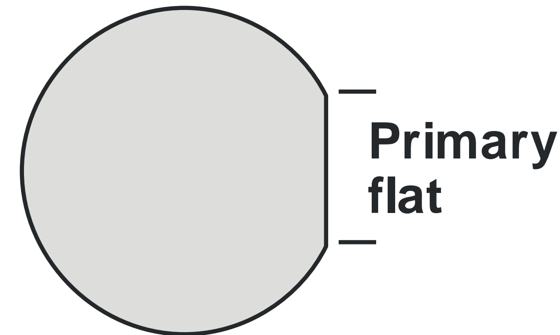


Wafer orientation

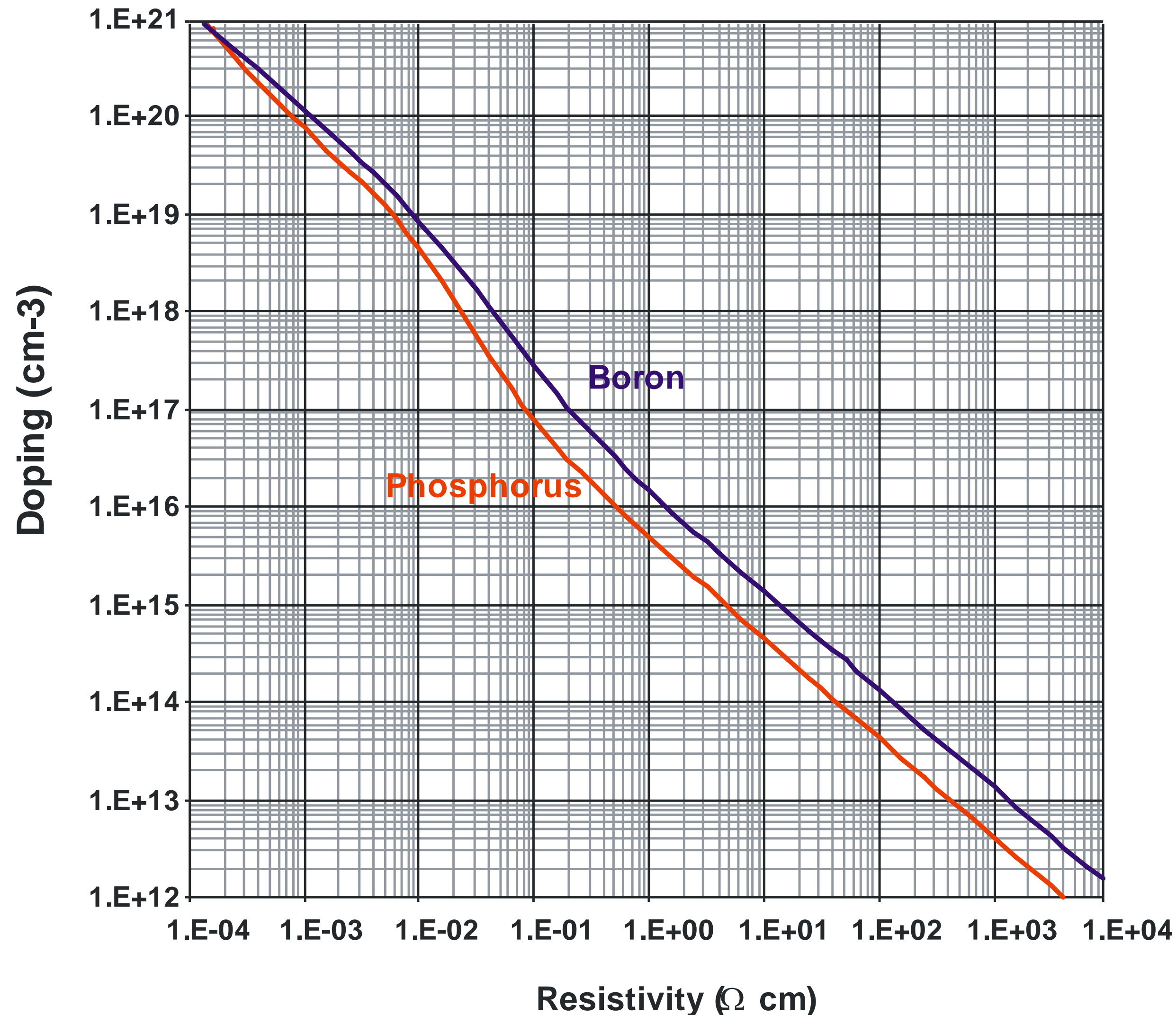








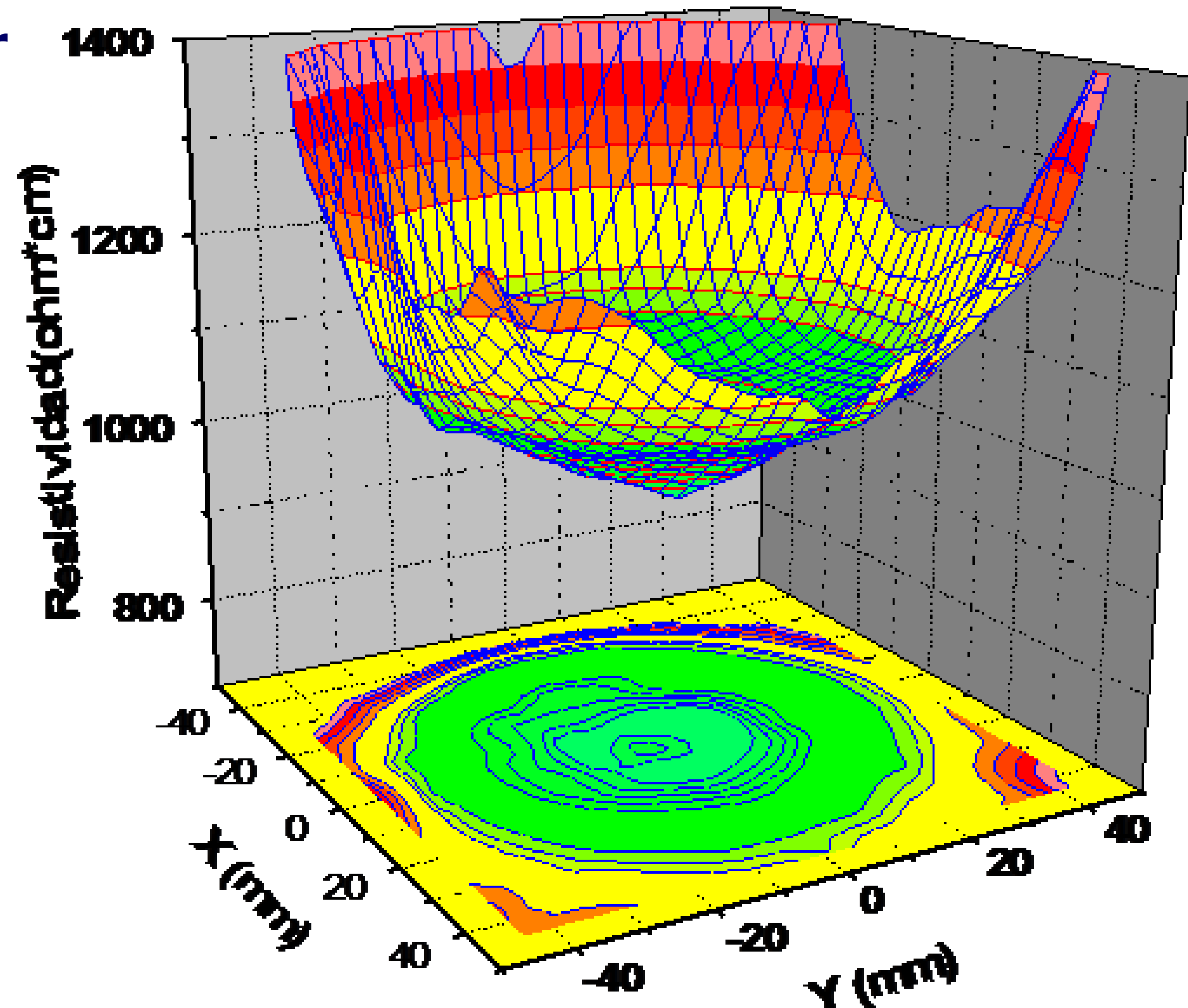
Doping-resistivity relationship (Thurber curves)



Resistivity variation

- From wafer to wafer
- Intra wafer

Example: Surface resistiviy mapping of a MCZ wafer measured by 4-point probe method.



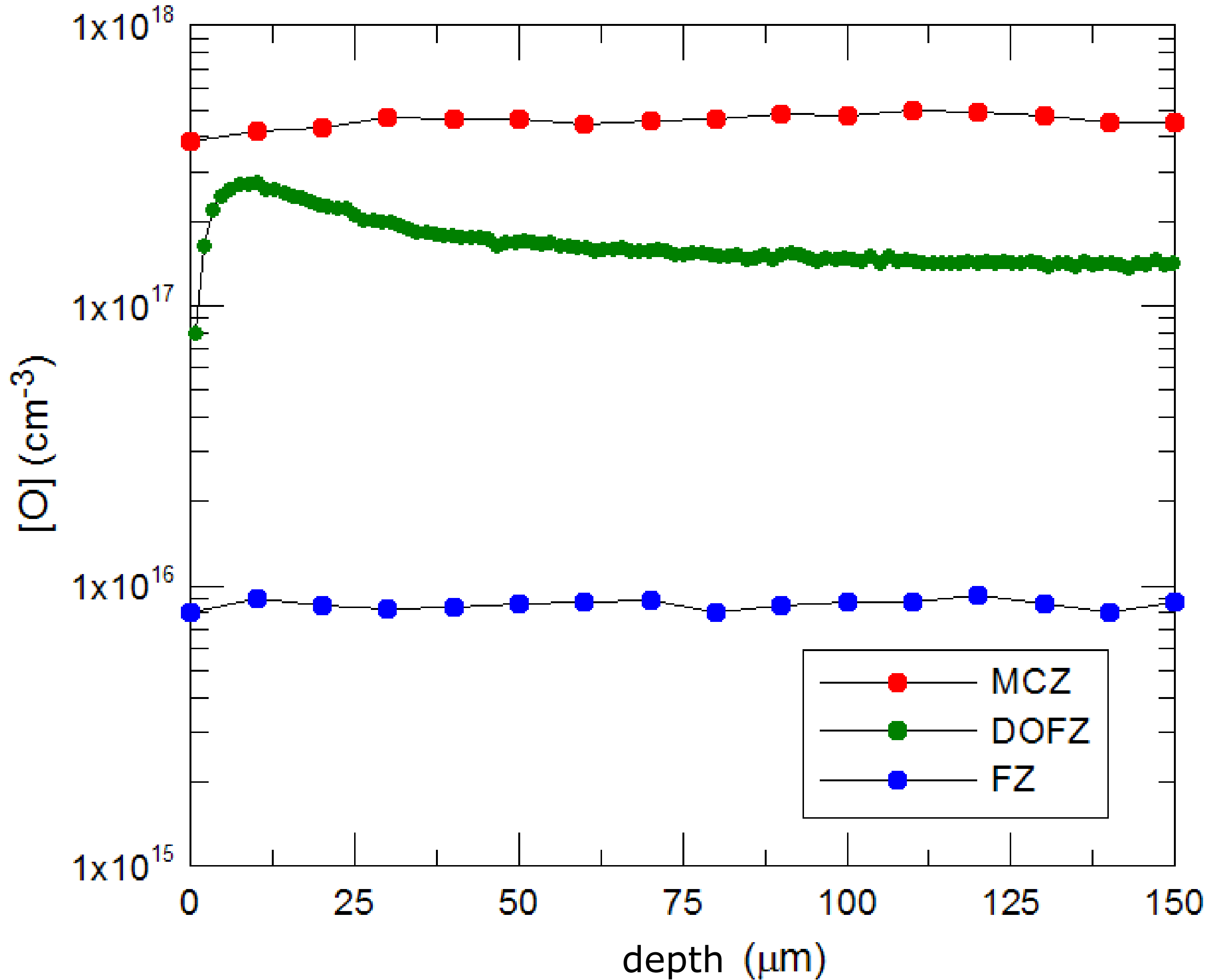
Oxygen in silicon

- It is known that high concentrations of interstitial oxygen ($>10^{17}$ cm^{-3}) in siicon wafers increases radiation hardness of detectors

- There is no the perfect wafer available
  - CZ silicon has [O]↑ but low resistivity
  - FZ is the opposite
  - Magnetic CZ allows high resistivity keeping high oxygen
  - It is also posible to diffuse oxigen in FZ wafers

Substrate	Resistivity	[O] (cm^{-3})
Float Zone (FZ)	High	$< 10^{16}$
Czochralski (CZ)	Low	10^{17}-10^{18}
Diffusion Oxygenated FZ (DOFZ)	High	Up to 10^{17}
Magnetic CZ (MCZ)	High	10^{17}-10^{18}

Oxygen content

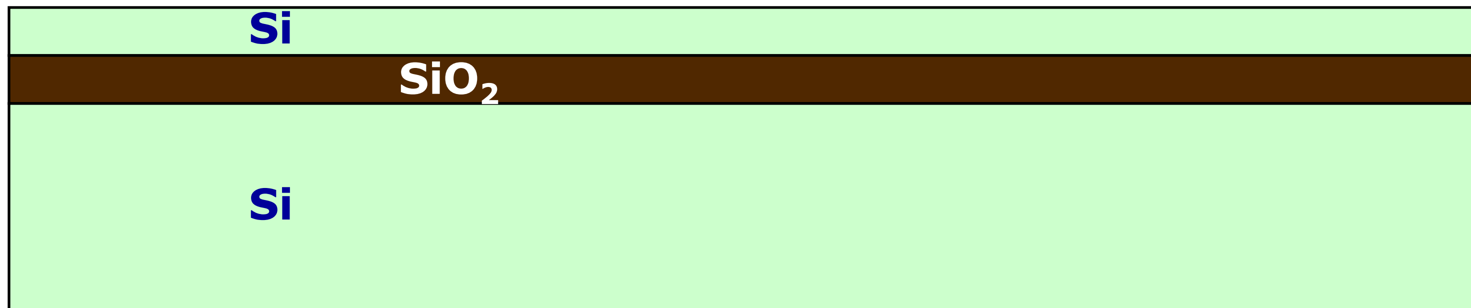


Oxygen content profile obtained by SIMS

(half wafer, the other half is equal)

SOI substrates

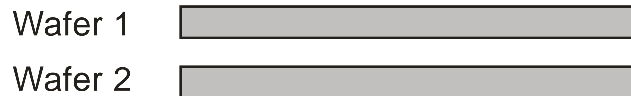
- SOI (silicon on insulator): Silicon active layer is over an insulating layer.
- Usually used the sandwich Si-SiO_2-Si

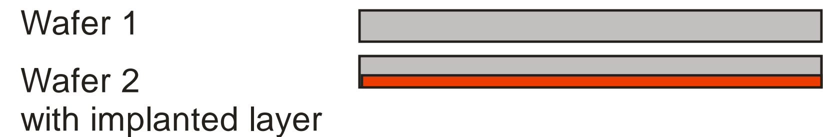


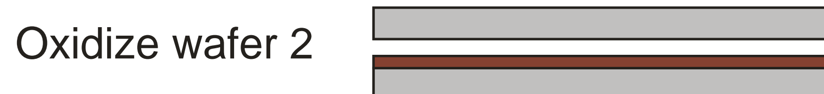
- Fabrication techniques
  - SIMOX: deep O_2 implant and anneal
  - BESOI: oxidation, bonding, polishing
  - Soitech: H_2 implant, bonding, anneal, separation

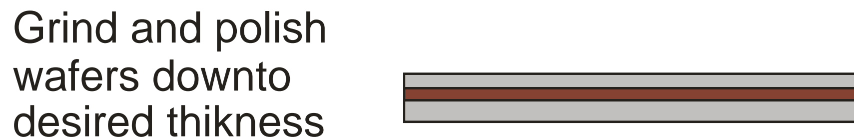
SOI wafers

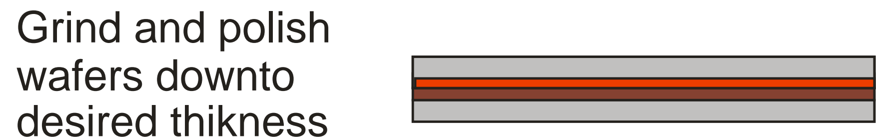
- Can be tailored to the needs:
  - Thickness of each wafer
  - Thickness of intermediate layer
- Implanted wafers can be used
  - Even with more complex processing
- It is also possible to de-bond wafers





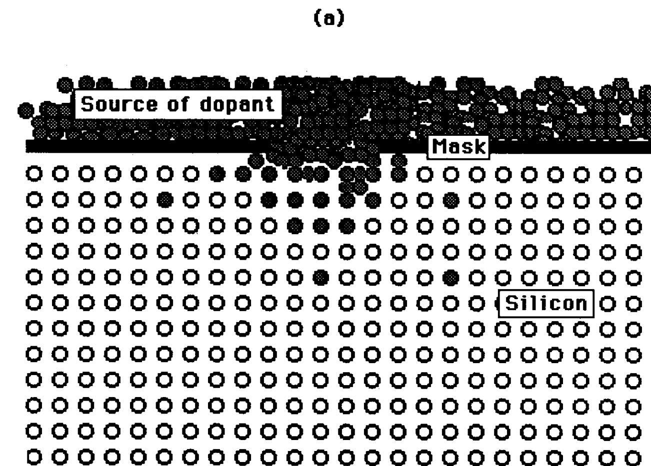


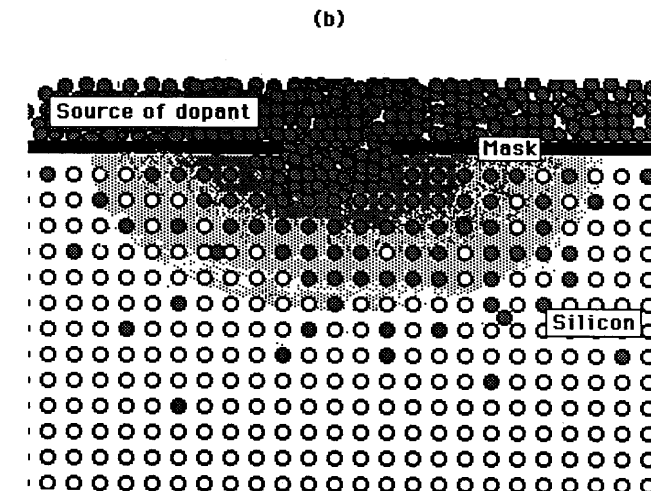




Dopant thermal diffusion

- Atom movement within a solid at high temperatures.
- Used to introduce dopants into semiconductor substrates (n+ and p+ regions)
- Parameters:
  - Diffusion coefficient of each dopant into silicon
  - Dopant Concentration, Temperature and Time
- Dopant types
  - Acceptor (N-type): Boron
  - Donor (N-type): Phosphorus, Arsenic
- Dopant sources: gas, liquid, solid





Dopant thermal diffusion

- **A SiO_2 mask can be used to limit dopant area**
- **Reproduce the mask on the wafer surface (SiO_2 resistant to high T and dopants diffusion)**
- **Apply the right concentration, temperature and time**

- **Two possibilities:**
  - **Dopants in ambient in constant concentration: Predeposition + diffusion**
  - **Dopant introduced in silicon: Implant + Drive-in**

Dopant thermal diffusion model

- **Analytical solution for the two cases presented**

Predeposition

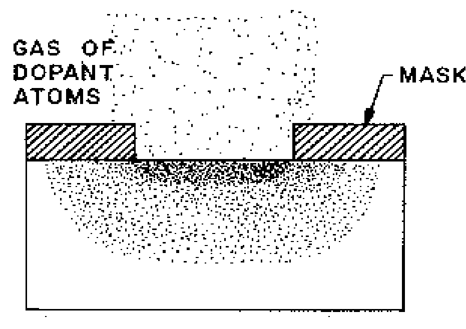
Constant surface concentration

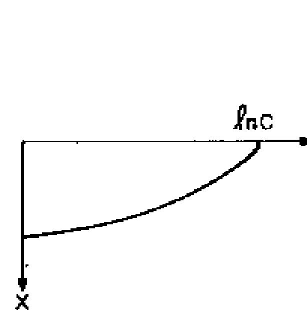
Ion implant

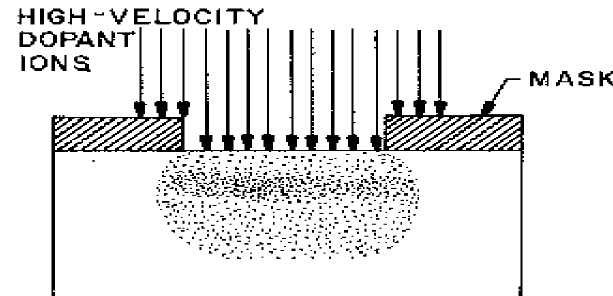
Constant total charge

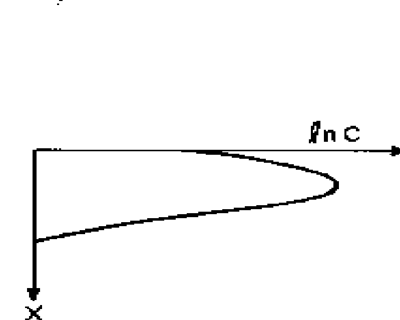
$$C(0,t) = C_S \quad \Rightarrow \quad C(x,t) = C_S \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right)$$

$$\int C(x,t)\,dx = Q \quad \Rightarrow \quad C(x,t) = \frac{Q}{\sqrt{\pi Dt}} \exp\left(\frac{-x^2}{4Dt}\right)$$





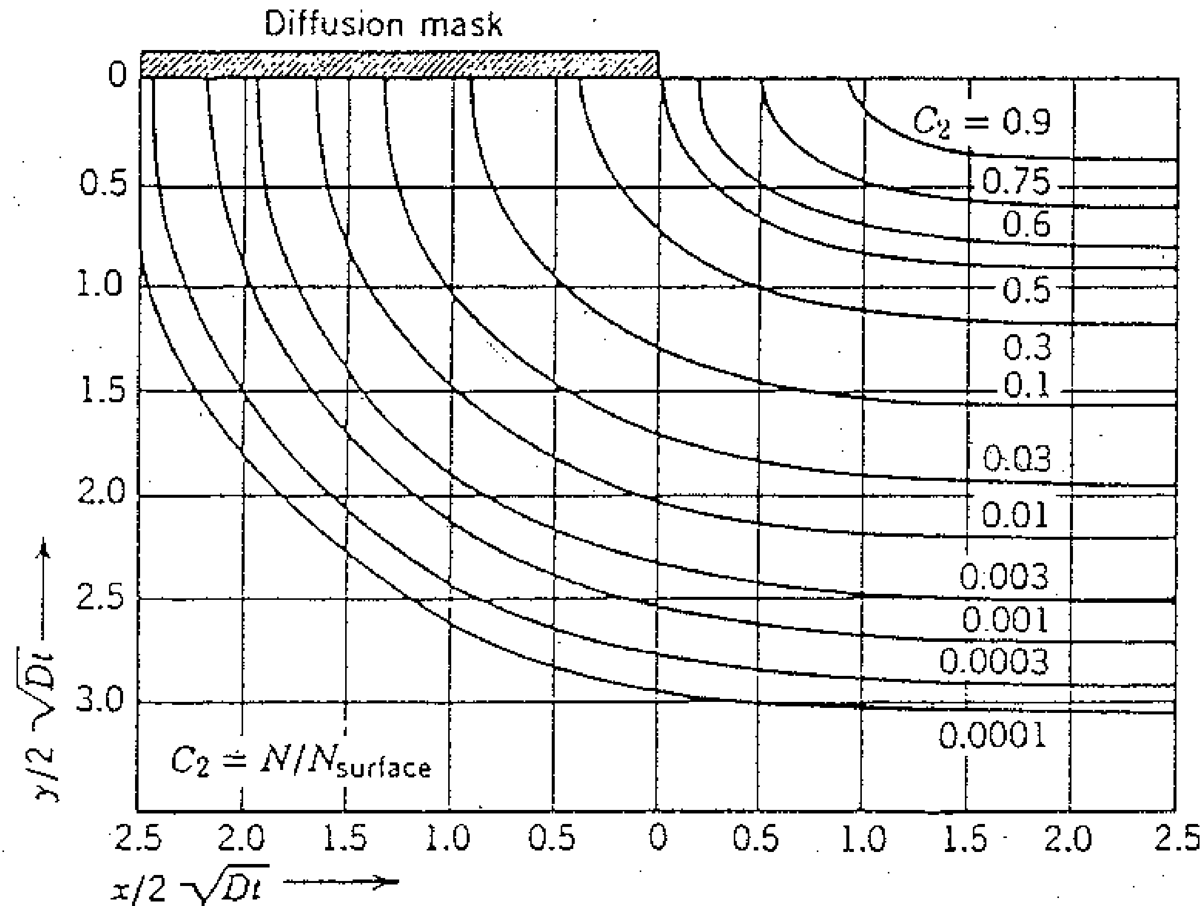




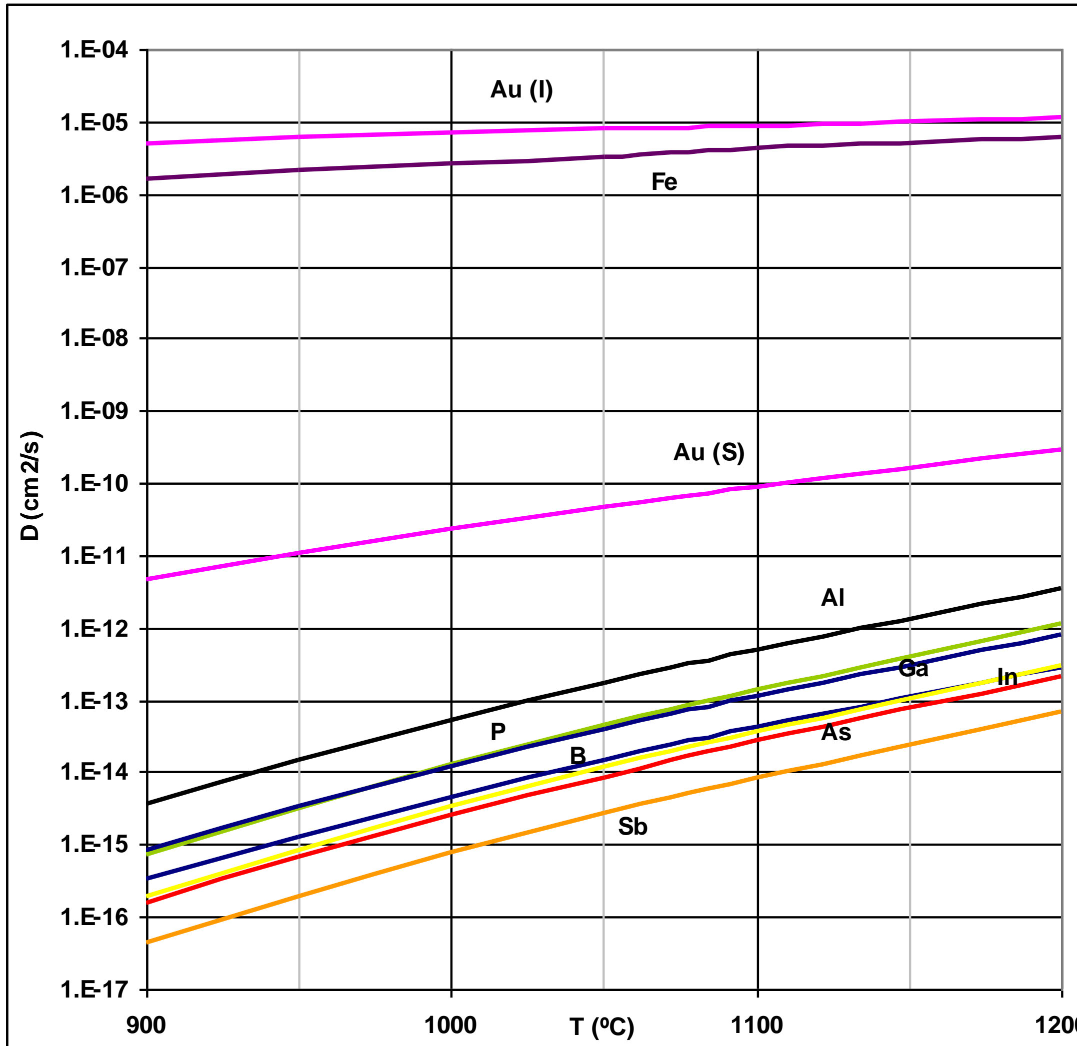
Lateral diffusion

- **Dopants diffuse below masks**

lateral diffusion = 0.8 vertical diffusion



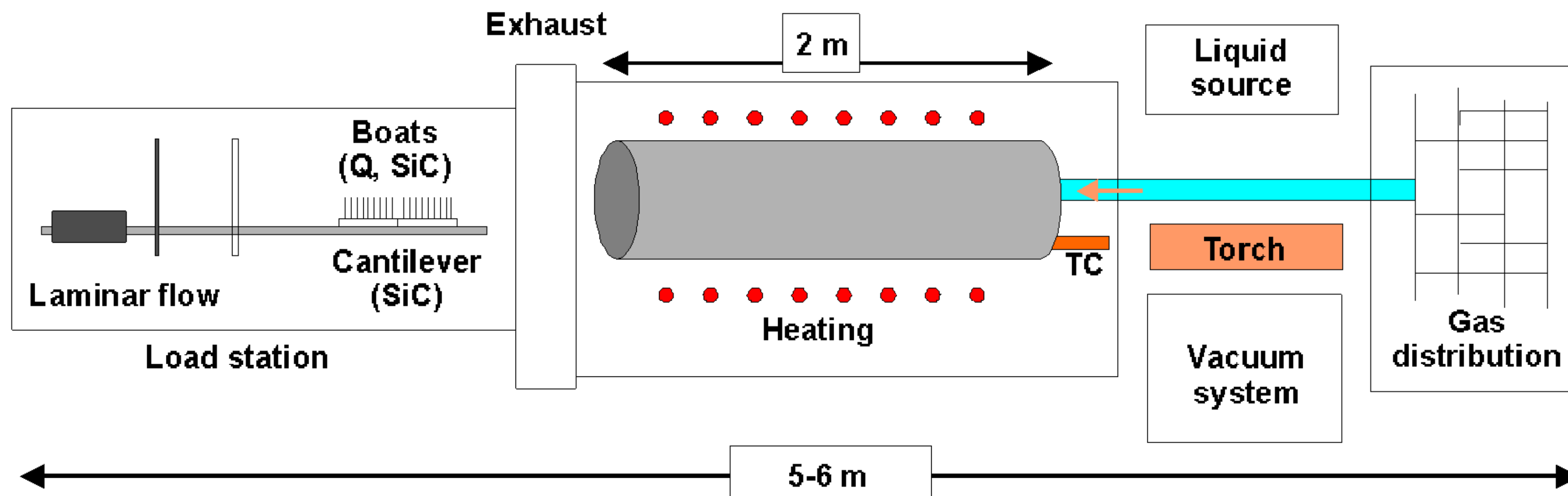
Diffusion coefficients



- **Contamination concern:**
  - **Na, Au.**
- **Example: length diffused during 1 hour at 1000 ºC:**

B	0.039 µm
P	0.065 µm
As	0.029 µm
O	2.4 µm
Au	300 µm
Na	> 1,000 µm

Furnace layout



- **Tube material:**
  - **Quartz**
  - **Polysilicon**
  - **SiC**
- **Wall**
  - **Single**
  - **Double**

Furnace wall material comparison

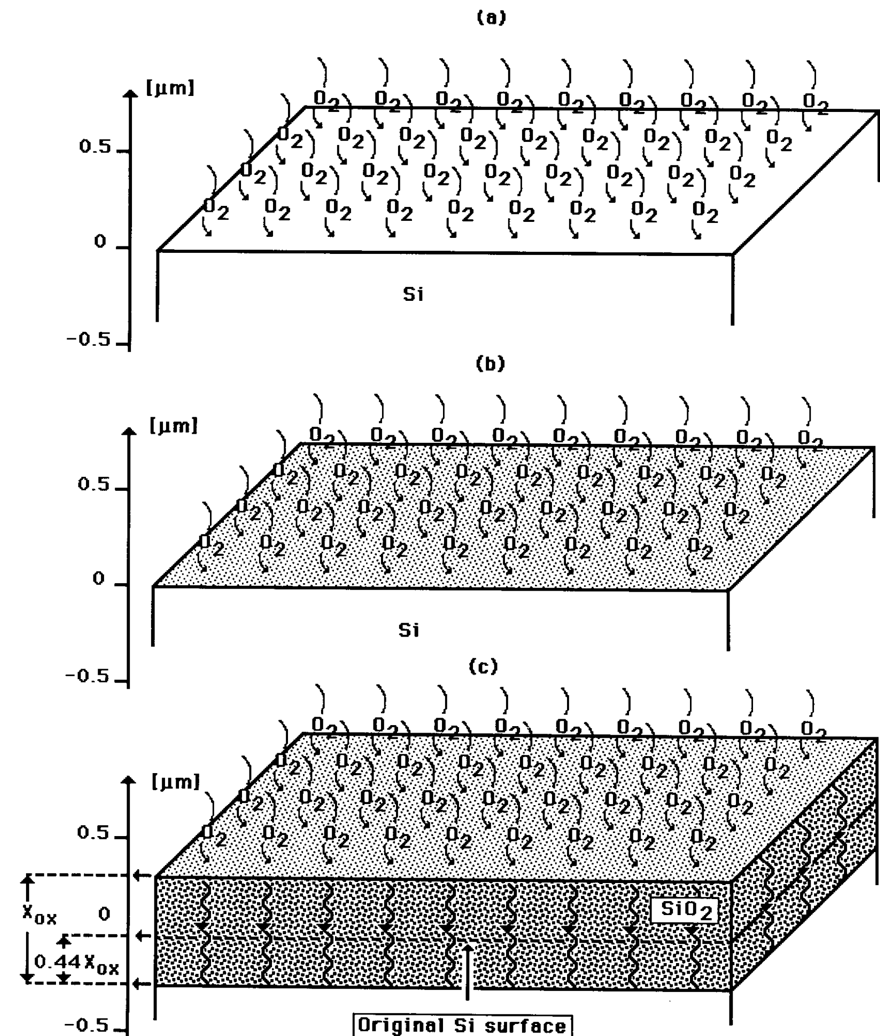
Tube type	Advantages	Disadvantages
Quartz SW	Cheap (4,000 €)	Quartz transparent for most contaminants Sag, creep Devitrification (brittleness) at HT < 1100ºC Thick wall < 1200ºC unusable
Quartz DW	Low pollution	Expensive Large gas consumption
Poly	Contaminant barrier Process up to 1400ºC	Expensive High Cu diffusivity
SiC	High durability (infinite lifetime) Process up to 1350ºC	Very expensive (25,000 €)

- Summary:
  - Up to 1100ºC → Quartz
  - Higher → SiC

Furnace images

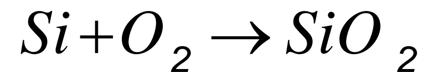
Thermal oxidation

- SiO_2 growing from silicon on the silicon
- SiO_2 is an amorphous material and very good insulator
- High temperature process
  - 950 - 1150 ºC
- Used for:
  - Mask for further thermal steps
  - Insulating layer
  - Gate dielectric oxide in MOS devices
- SiO_2 characterization
  - Density, porosity
  - Pinholes
  - Dielectric breakdown
  - Trapped charge
  - SiO_2-Si interface states

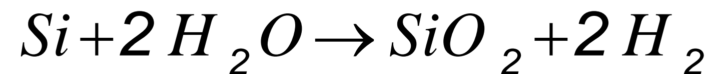


Thermal oxidation process

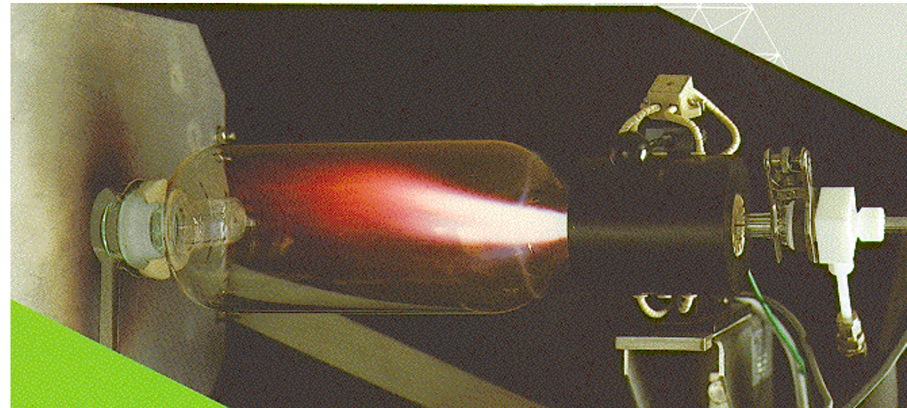
- **Same furnaces as for thermal diffusion**
- **Dry thermal oxidation**
  - **O_2 atmosphere**
  - **Slow growth**
  - **High oxide quality**
- **Wet thermal oxidation**
  - **H_2O atmosphere**
    - **H_2O bubbler**
    - **H_2+O_2 combustion**
  - **Fast growing**
  - **Worse quality**



$$Si+O_2 \rightarrow SiO_2$$



$$Si+2H_2O \rightarrow SiO_2+2H_2$$



Thermal oxidation model

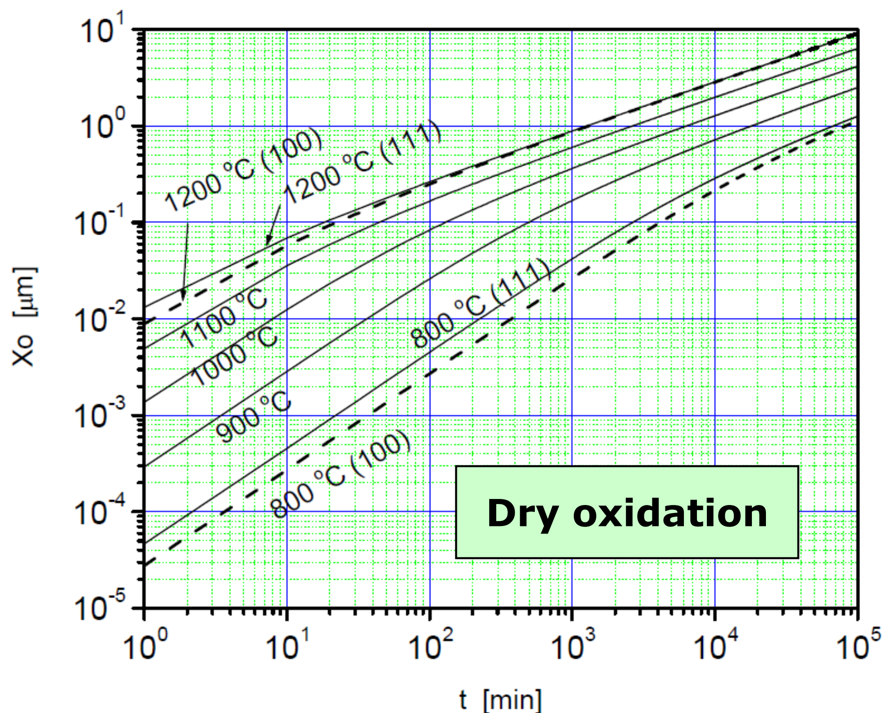
- **Deal & Grove model**

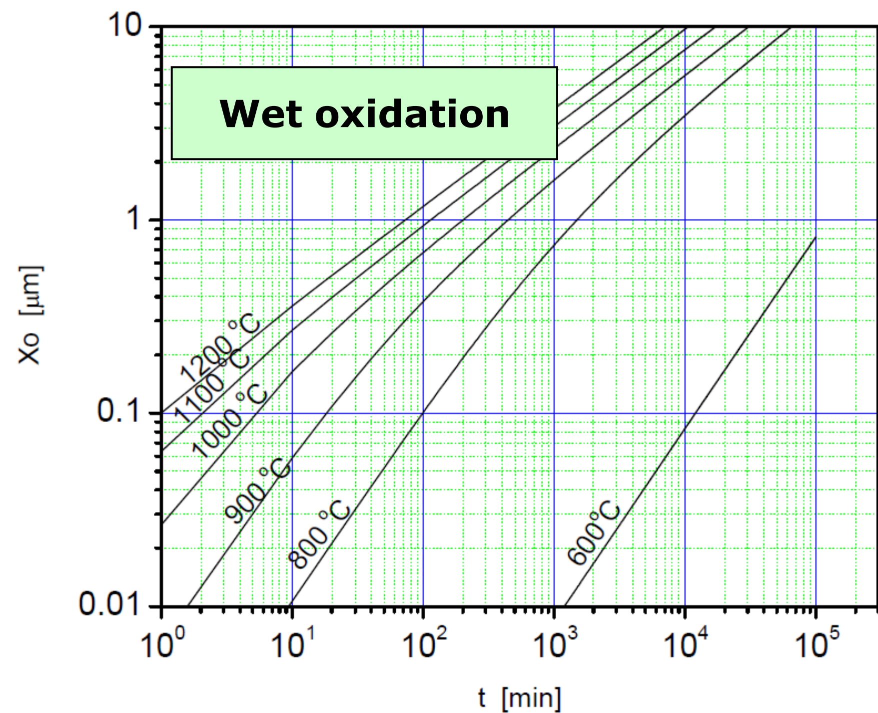
$$\frac{1}{B} d_{ox}^2 + \frac{A}{B} d_{ox} = t + \tau$$

$$B = B_0 \exp(-E_B / kT)$$

$$B / A = (B / A)_0 \exp(-E_{B/A} / kT)$$

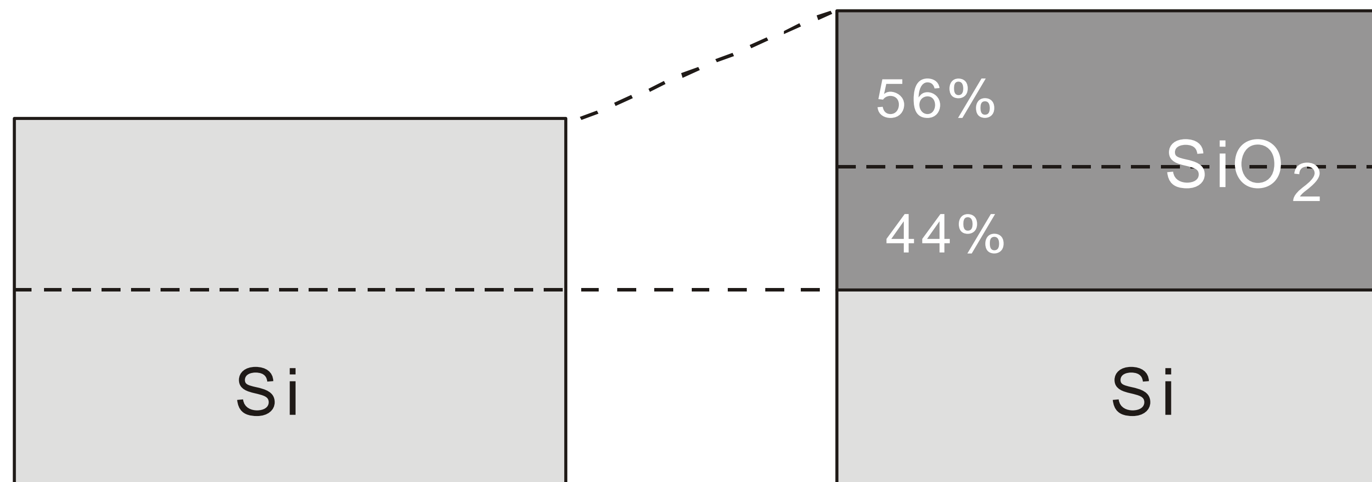
$$\tau = \frac{d_i^2 + A d_i}{B}$$





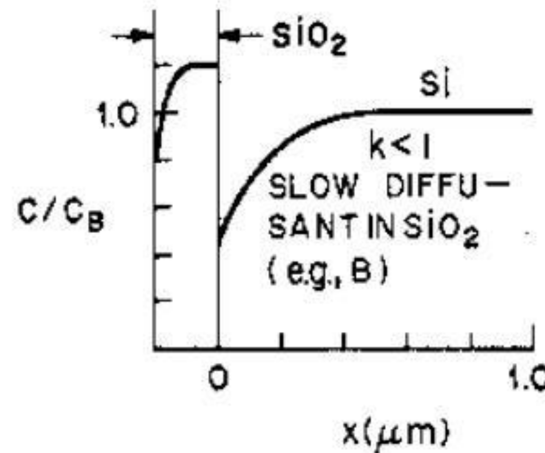
Silicon thermal oxidation

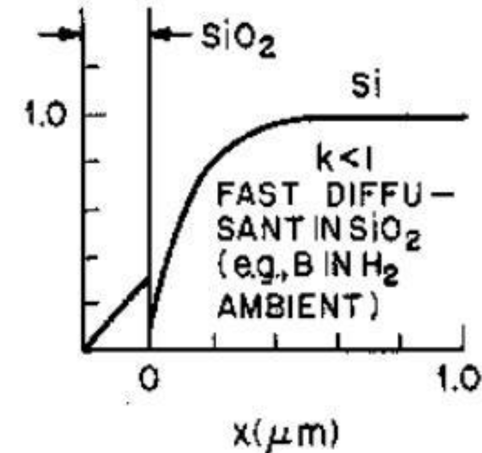
- **SiO2 grows consuming silicon substrate**
  - **As opposite to deposition**

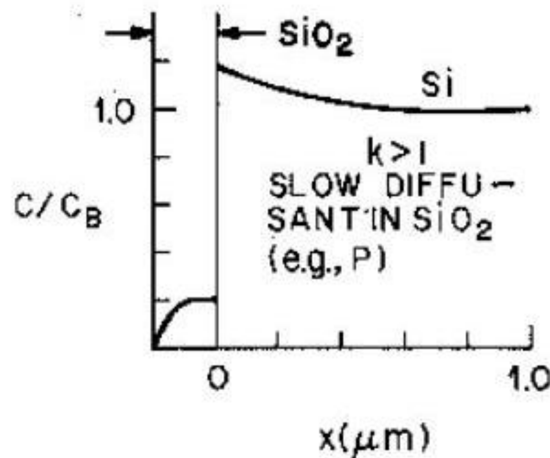


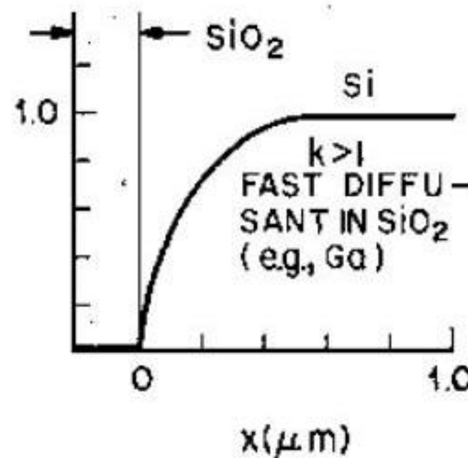
Relationship between diffusion and oxidation

- **Segregation coefficient k**
- **k<1 Oxide takes impurities from substrate**







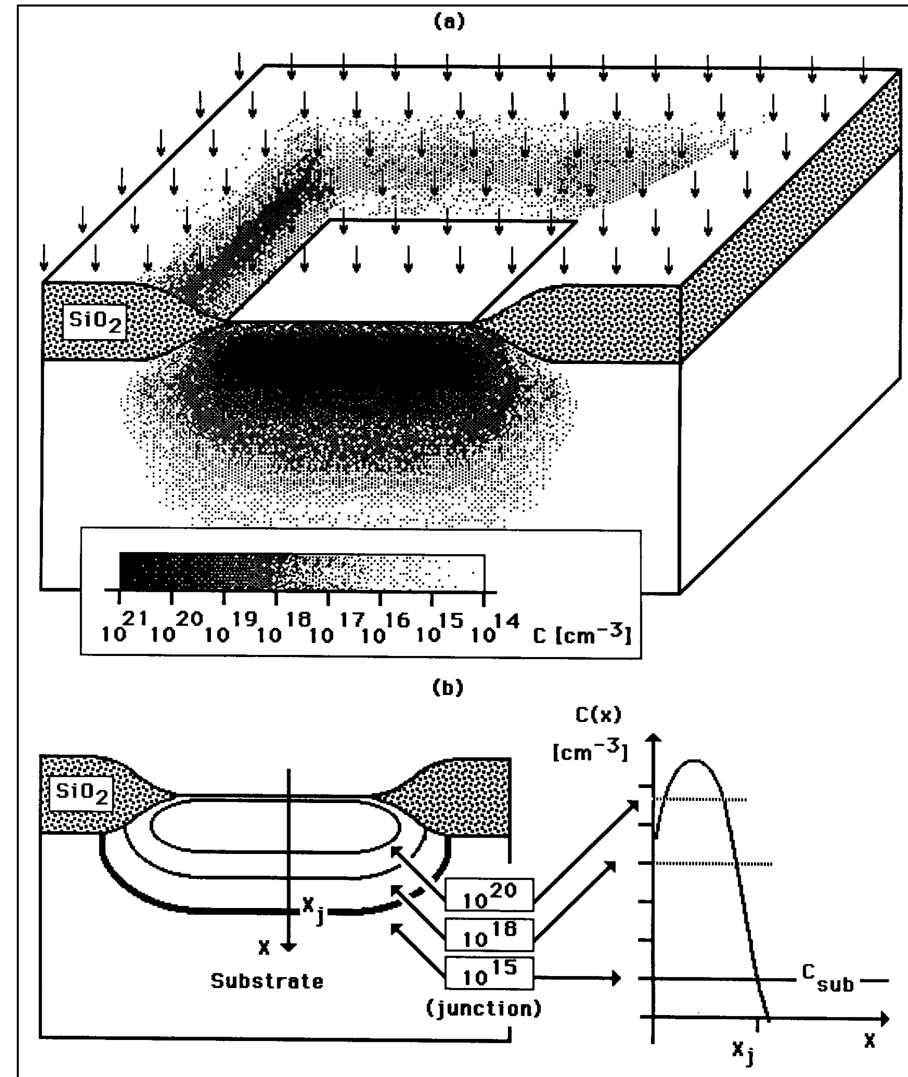


- **k<1 Oxide rejects impurities to substrate**

Ion implant

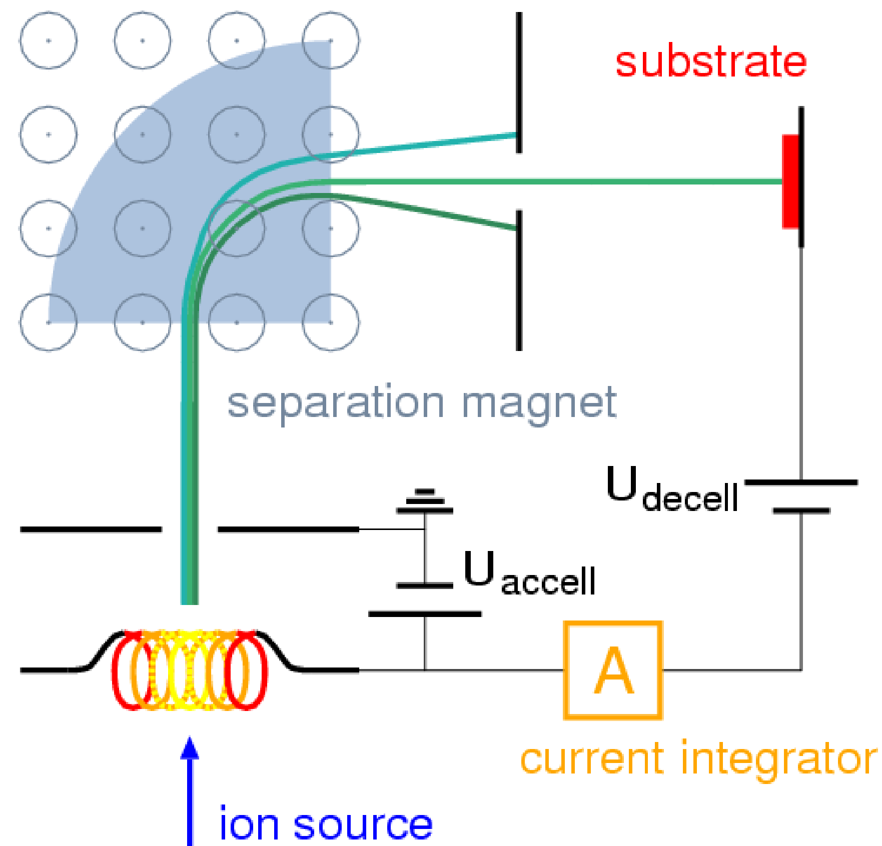
- Impurity introduction in substrates
- Very well dose control
  - Masking (SiO_2 for instance) can be used to delimit doping regions
- Method:
  - Ion (isotope) acceleration in an electric field
- Parameters:
  - Energy: 50 -250 keV (even 1MeV)
  - Dose: $10^{11} – 10^{14}$ ions/cm^2

  (= current × time)
- Impurities
  - N-type: As, P
  - P-type: B
  - Other elements: O, F, N, Ar



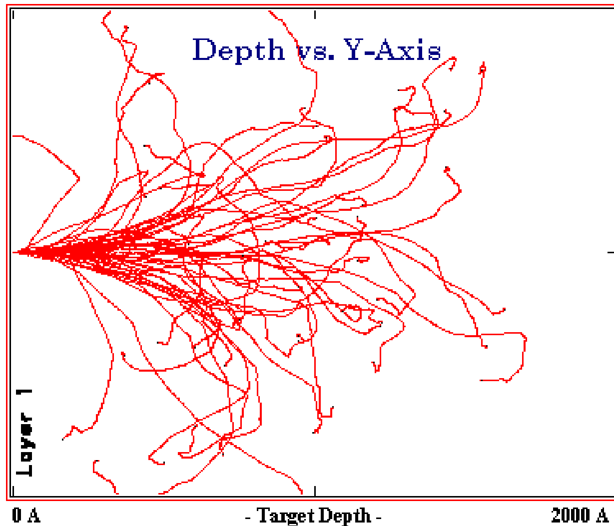
Ion implant effect to be considered

- **Amorphization: After implant, crystal structure of Si is damaged.**
- **⇨ Annealing is necessary (minimum 950ºC, 20 min)**
- **Channeling: If implanting perpendicular to crystal structure, ions enter very deep without control**
- **⇨ Wafer rotated and tilted**
- **Uses:**
  - **Junction formation**
  - **Polysilicon doping**
  - **Threshold voltage adjustment**



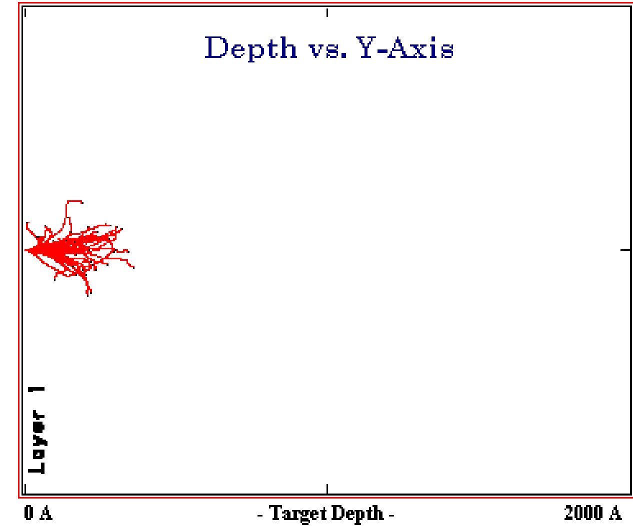
Ion implanter schematic

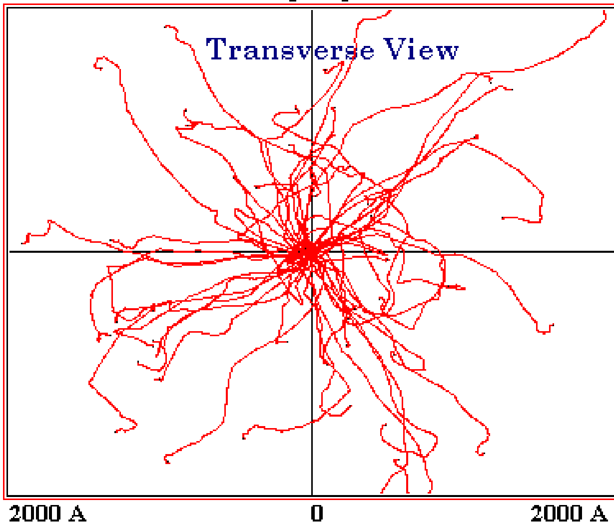
Ion implant



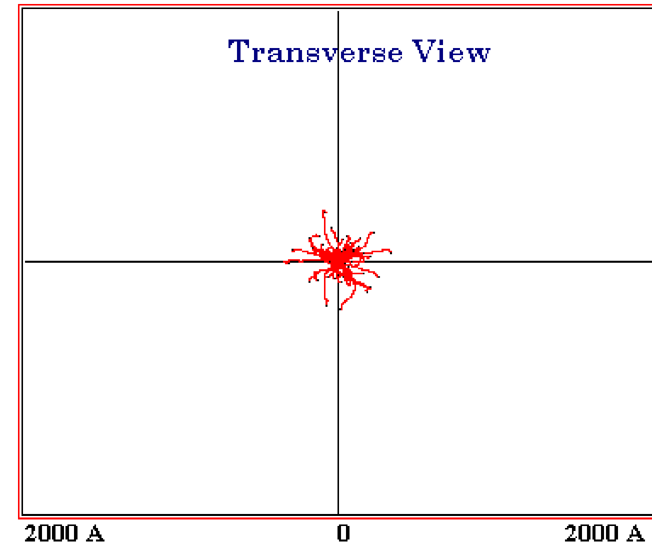
E=100 keV

Boron
(light atom)





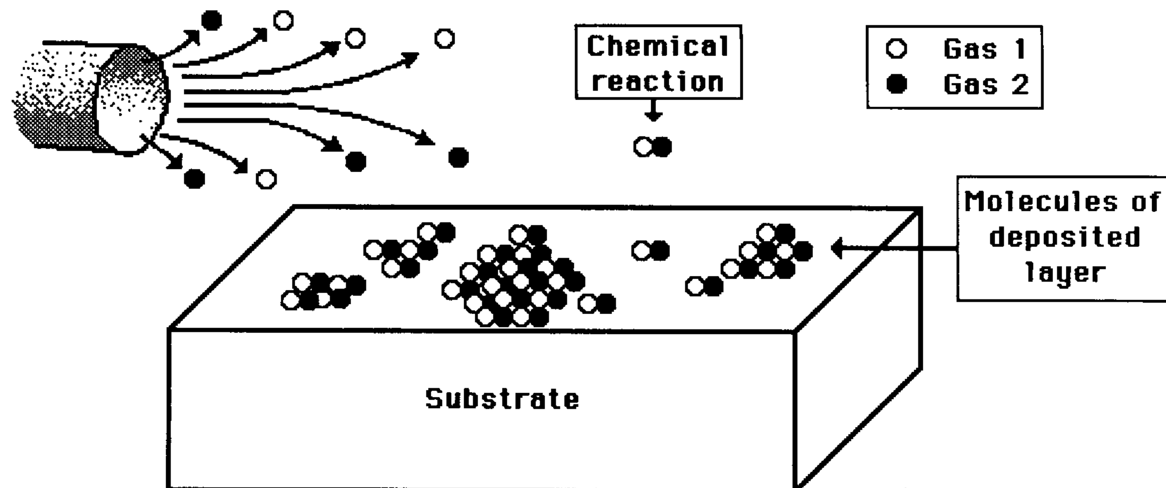
Phosphorus
(heavy atom)



CVD layer deposition

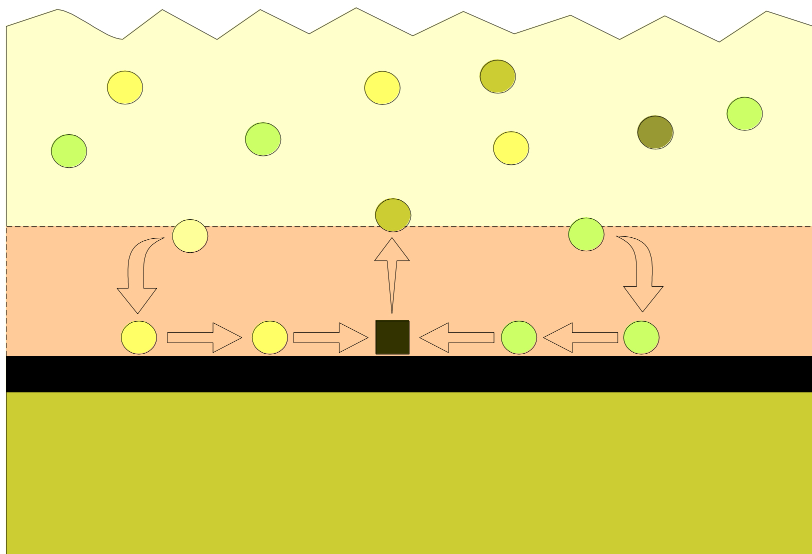
- **CVD: Chemical Vapor Deposition**
- **Layer deposition by chemical reaction in vapor phase**
- **Mainly used for dielectric,s, but also for Poly**
- **Main deposited materials: Polysilicon, SiO_2, Si_2N_3 , BSG, PSG, BPSG (SiO_2 doped with B or P)**

- **HTCVD: High Temperature**
- **LTCVD: Low Temperature**
- **PECVD: Plasma Enhanced**
- **LPCVD: Low Pressure**
- **APCVD: Atmospheric Pressure**



CVD layer deposition

- The substrate does not participate in the process
- Reaction of gas molecules on the surface
  - Reactions in the gas to be avoided
- Linear growth: there is no diffusion through a layer of increasing thickness



- Deposit velocity limited by:
  - At high T, reactant concentration (APCVD)
  - At low P, surface reaction velocity (LPCVD, PECVD)
- As it is a surface reaction, layers offer good step coverage (conformal deposition)

CVD layer deposition

	APCVD	LPCVD	PECVD
Simplicity	+	-	--
Temperature	low	medium	low
Coverage	-	++	+
Speed	+	-	+

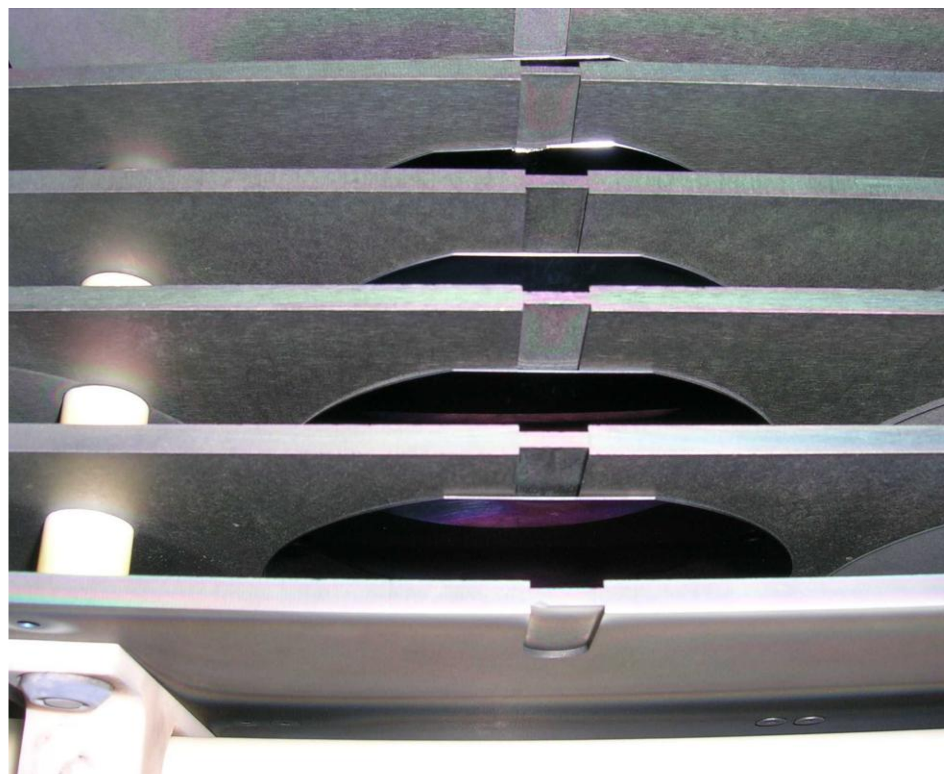
Gas	Type	Pressure	Temp	Layer
$SiH_2Cl_2 + NH_3$	LPCVD	~160mTorr	800°C	Nitride
SiH_4	LPCVD	~130mTorr	580 - 630°C	Polysilicon
N_2O, SiH_4, NH_3	PECVD	~1Torr	380°C	Oxide, nitride passivation
SiH_4, PH_3/SiH_4, B_2H_6, O_2	APCVD		400°C	Interlevel oxide, PSG, BPSG

CVD layer deposition

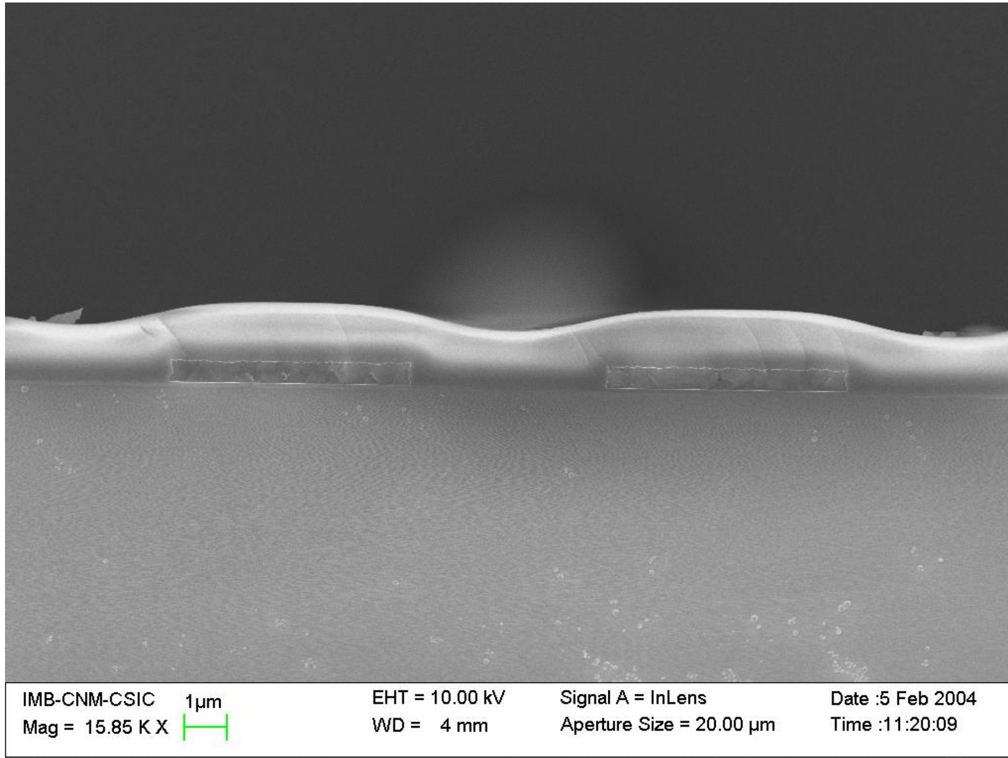
LPCVD poly deposition furnace

CVD layer deposition

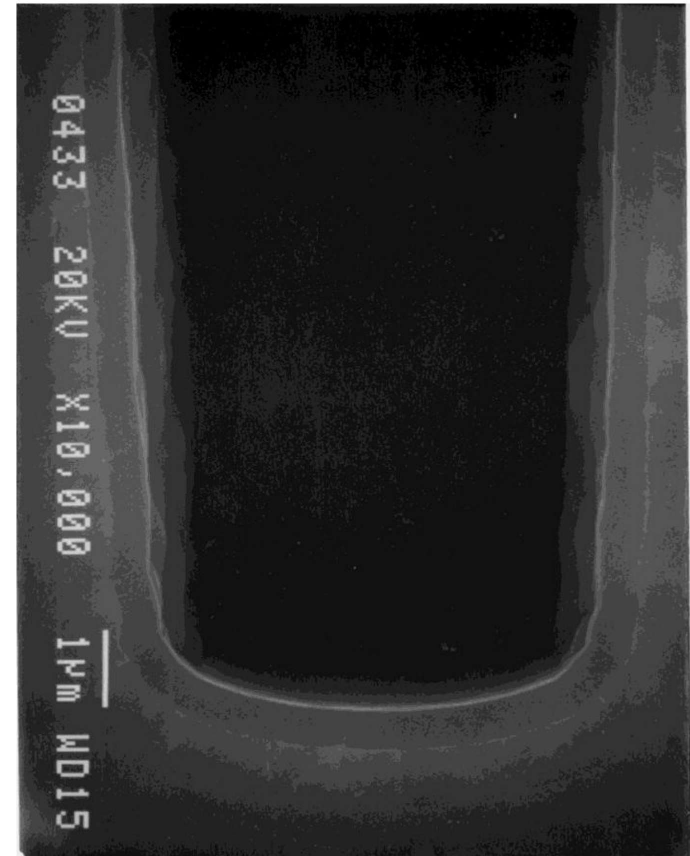
PECVD poly deposition furnace



CVD layer deposition



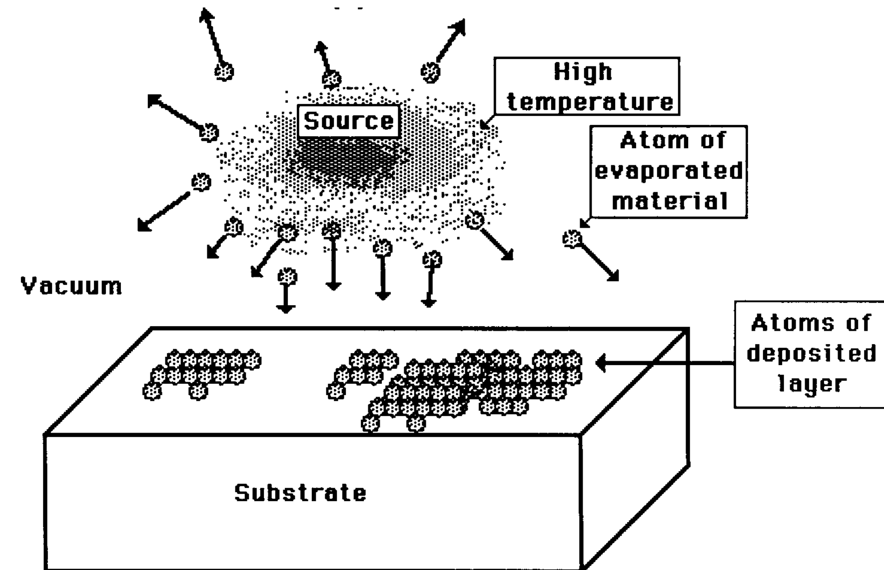
1.5 µm BPSG deposited
Planarization effect



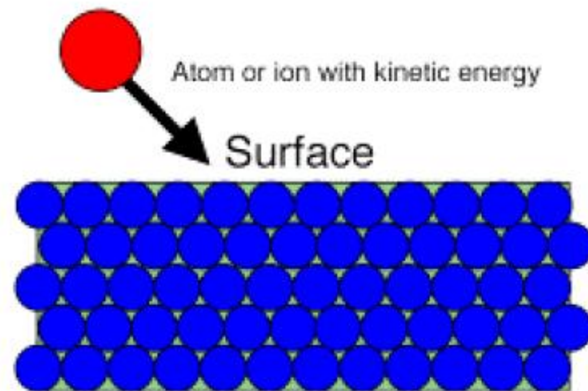
1 µm Poly deposited in holes
See the good wall coverage

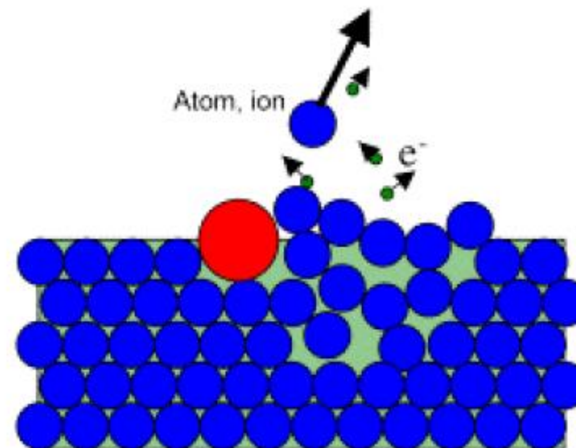
PVD metal layer deposition

- Metal deposition
- Techniques
  - Evaporation
  - Sputtering
- Multicomponent
  - Co-sputtering
  - Co-evaporation
- Problems with metals:
  - Spiking
  - Electromigration
- Metal used:
  - Al, Al/Si, Al/Cu, Al/Si/Cu, Au, Pt, W, Pd, Ti, Ta, Ni
- Multilayer metallization possible



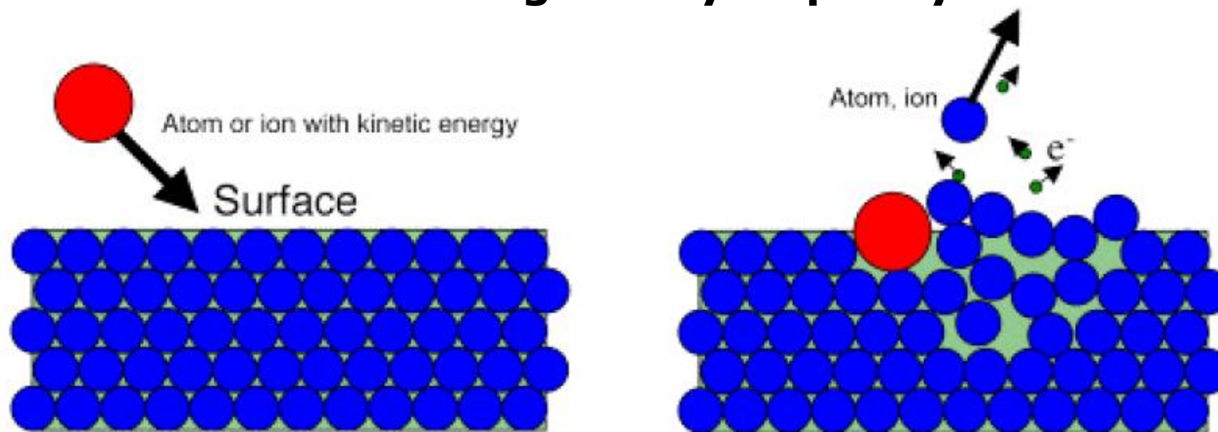
- **Sputtering: Ion or electron bombardment of target to extract atoms**





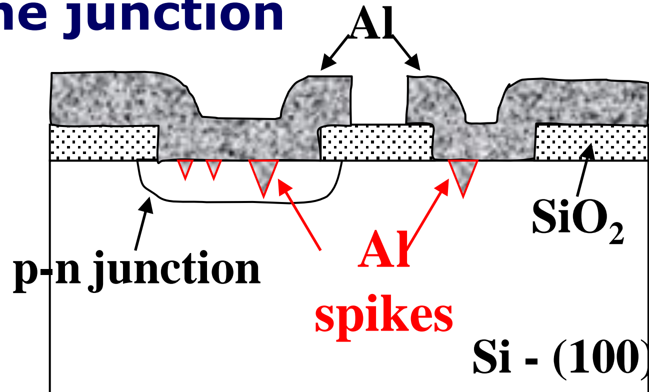
- **Evaporation: target heating to evaporate (actually sublimate) the metal and re-deposition on wafer surface (colder than target)**
  - **Difficult thickness control, contamination by crucible and coil metals, hard to deposit alloys**

- **Sputtering: Ion or electron bombardment of target to extract atoms**
  - **Good thickness control and good layer quality**



Metal problems

- **Spiking: Al penetration in substrate and eventually shorting the junction**



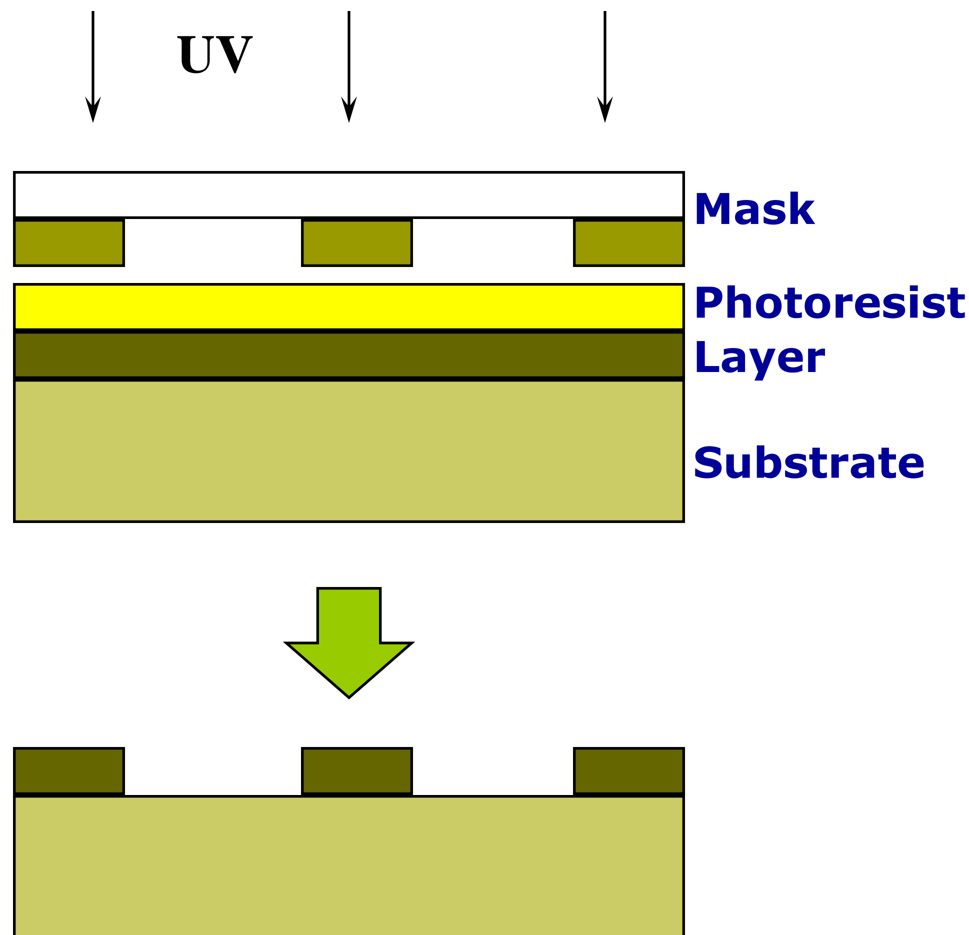
Spiking is due to dissolution of Si into Al and Al into Si and is related to the phase diagram.

Minimized by using Al/Si alloy and adjusting sintering temperature

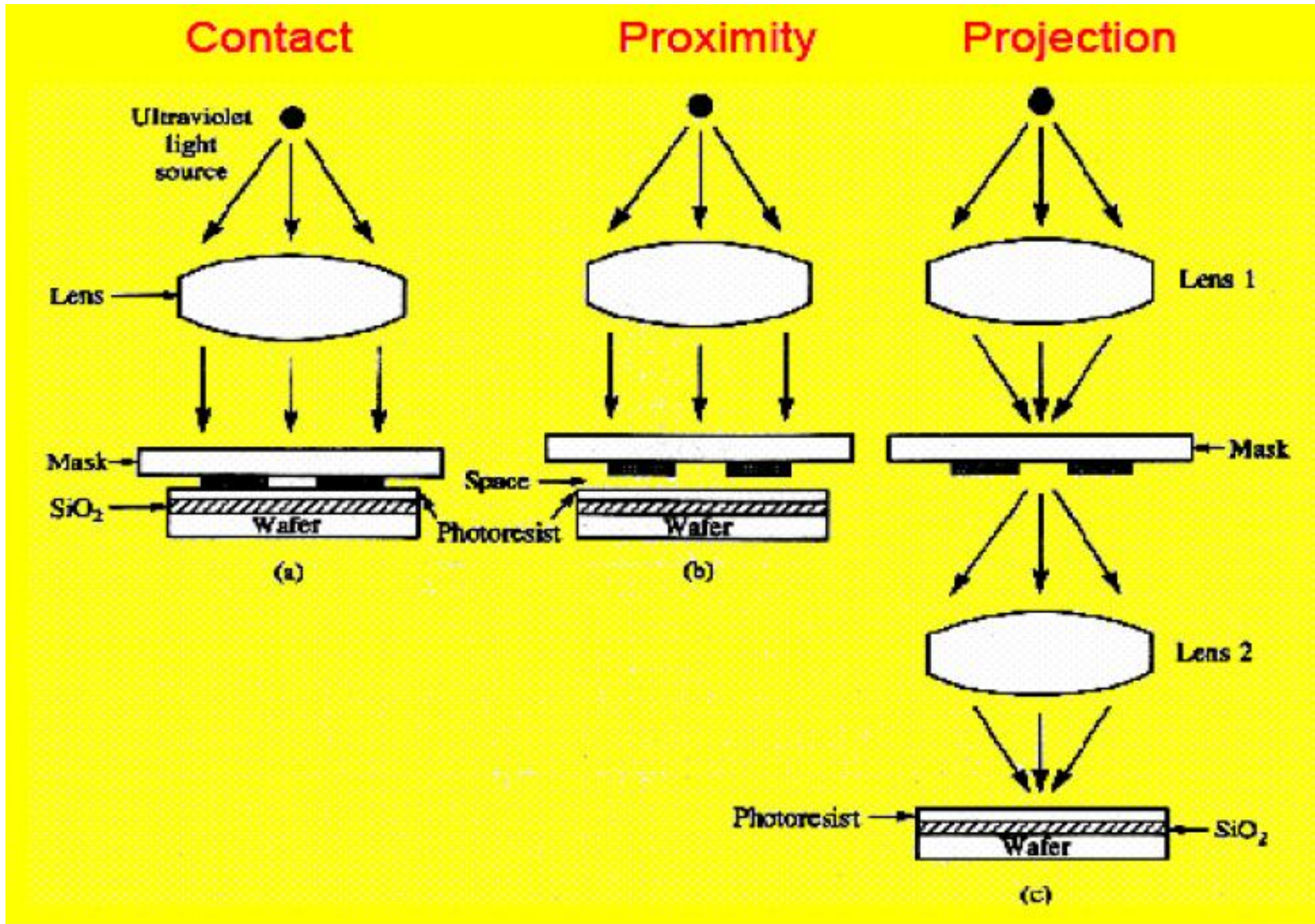
- **Electromigration: material movement due to kinetic energy of charge carriers. Eventually can open circuit a metallic track**
  - **Probability is proportional to current density, temperature and time**
  - **Minimized by using Al/Cu alloy**

Photolithography

- Image transfer from a glass mask to the wafer
- Employs
  - UV light
  - Masks or reticles
  - Photoresist
- Types
  - Contact/proximity
    - Resolution: 2um
  - Projection
    - Resolution: 1 um
- Better resolution
  - Deep UV
  - X rays
  - Electron beam

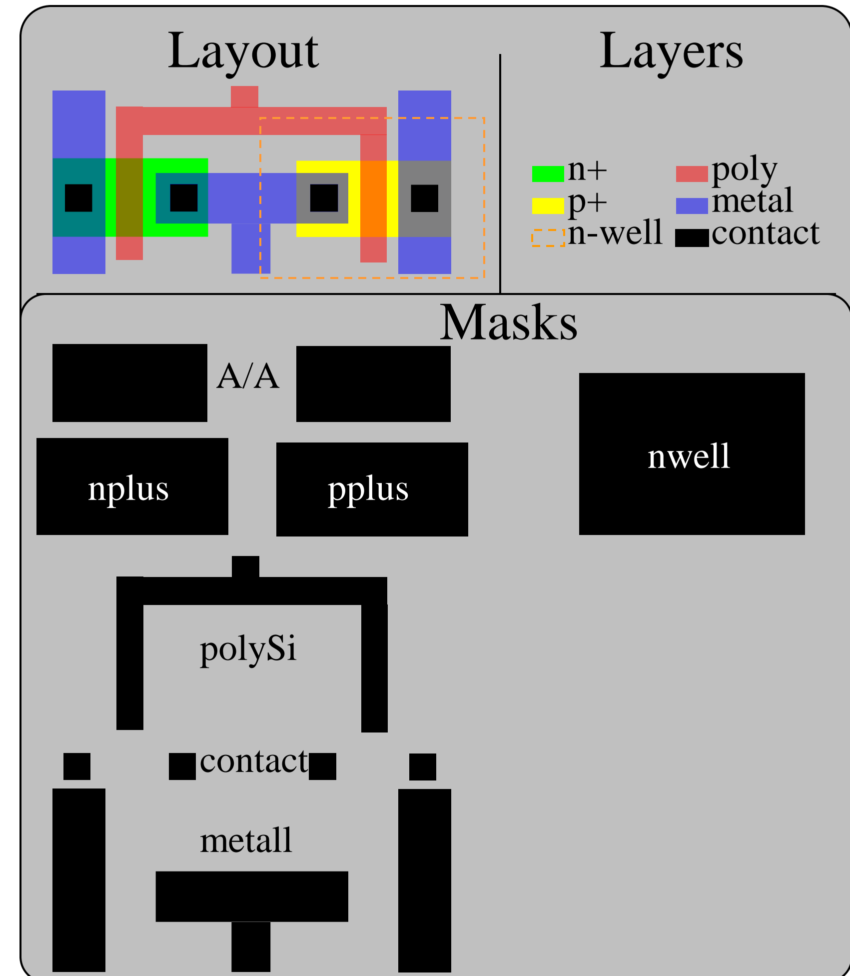


Photolithography types



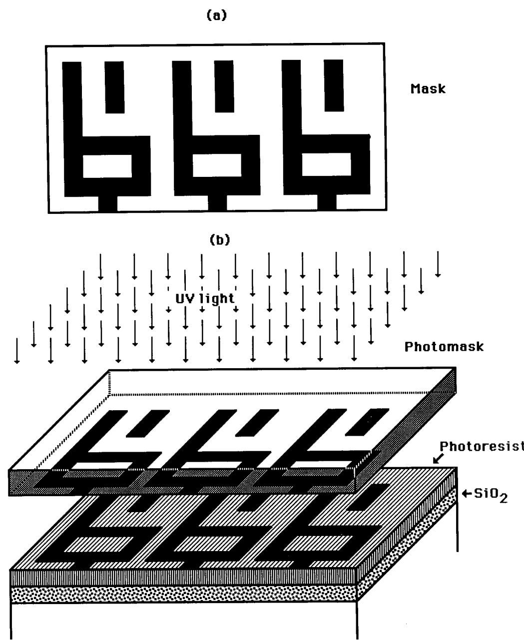
Photolithography masks

- **Layout: final geometrical drawings resulting from a design process for a target technology**
- **Layers: all the different basic drawing levels to design ICs for a target technology**
- **Masks: clear and opaque areas over a glass obtained from layers to transfer over and process the wafers.**
- **Mask material**
  - **Quartz and Chromium (with ARC)**

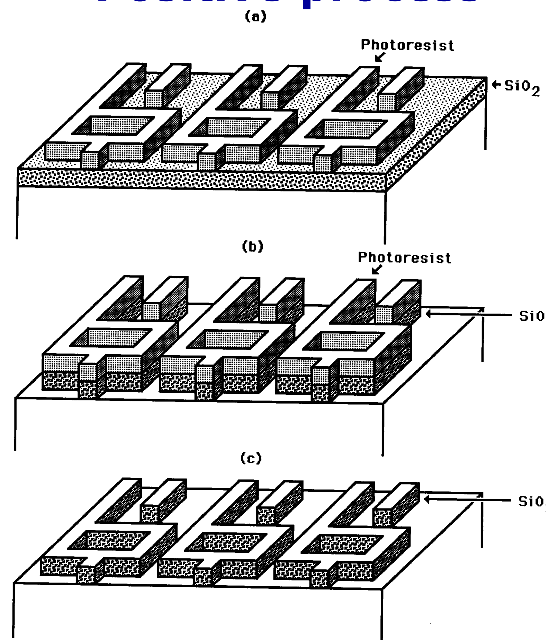


Photolithography process

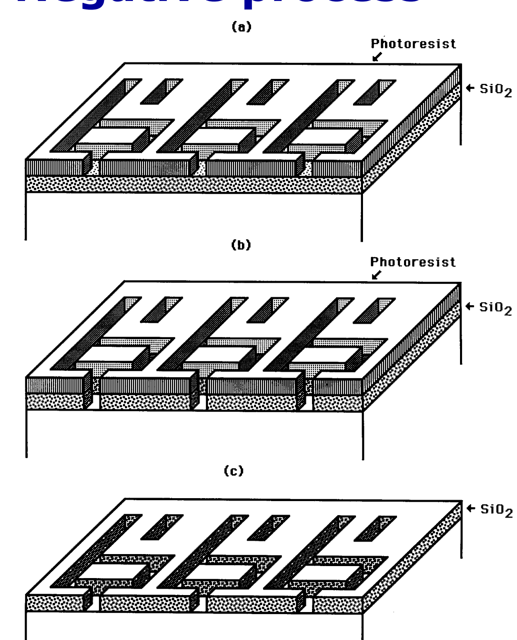
- Coating wafer with thin film photoresist
- Mask-Wafer Alignment
- UV Exposure
- Photoresist Development
- Etching/implant/etc.
- Photoresist removal



Positive process

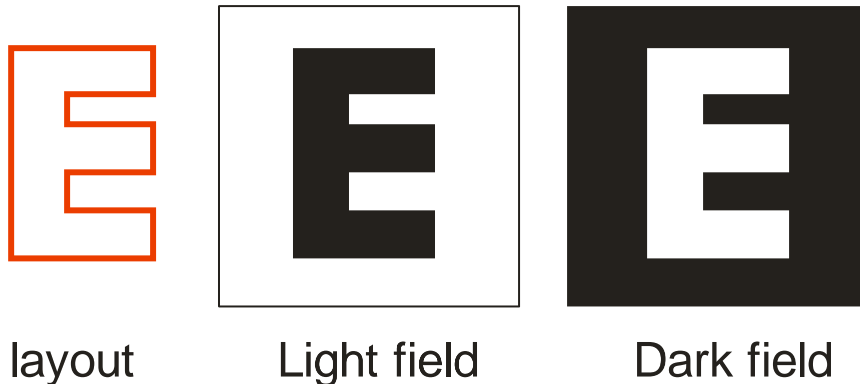


Negative process



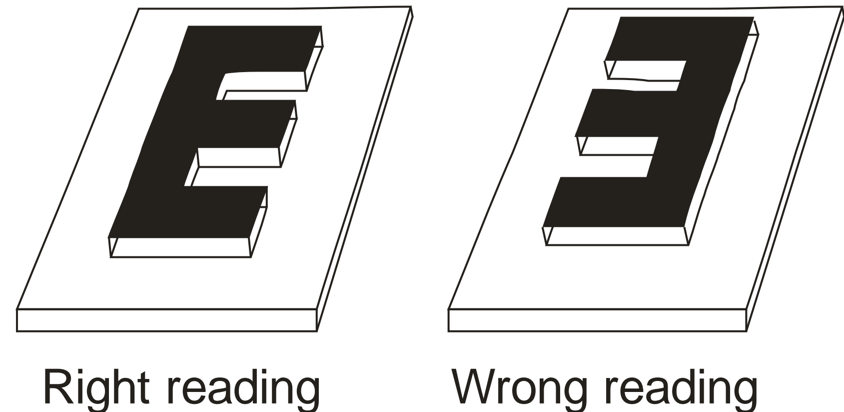
Photolithography process: Other key points

- Negative vs. positive photoresists
- Relationship between virtual layout and phisical mask
  - Dark field, light field
  - Right reading, wrong reading



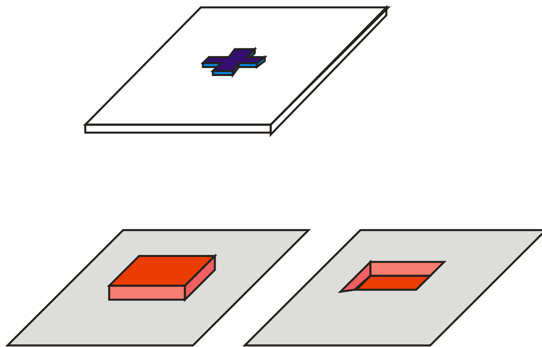
For masks to be used in the back side of the wafer.

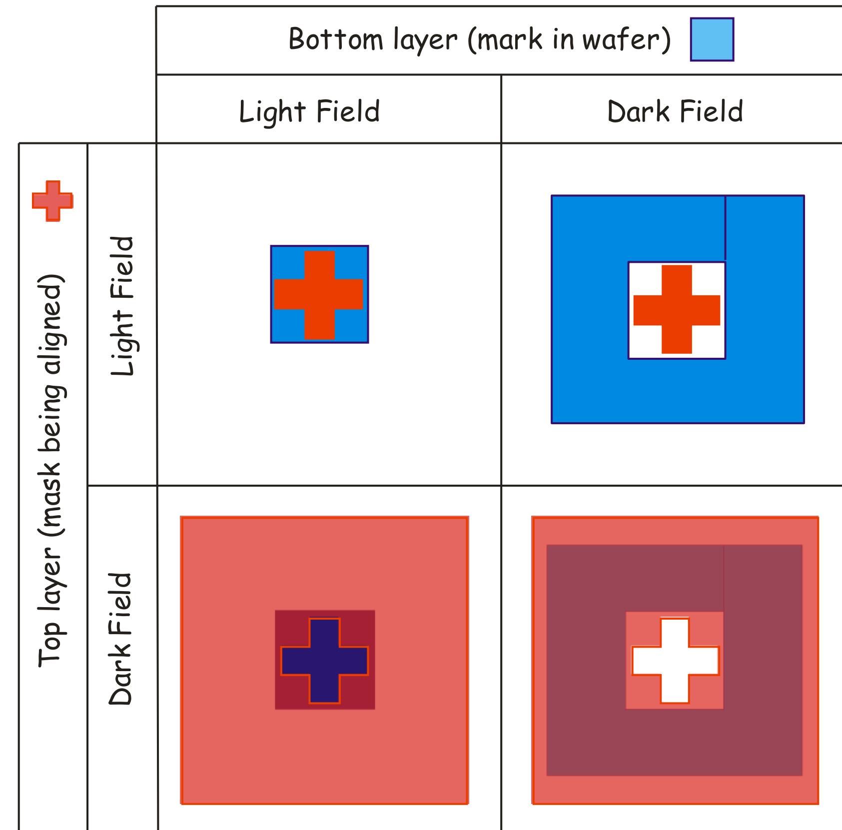
Two side processing



Photolithography process: Other key points

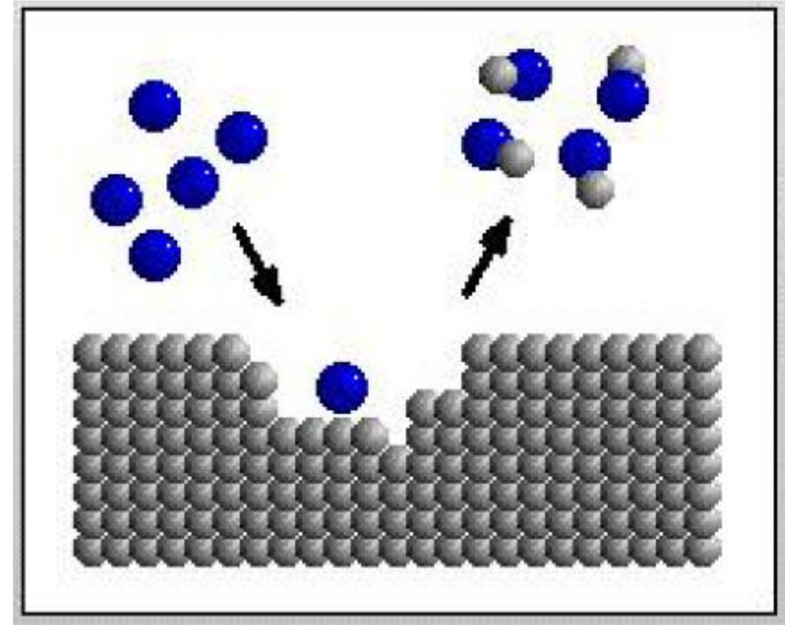
- **Projection lithography (Step and repeat)**
  - **Better resolution**
  - **Limited chip surface (25×25 mm maximum)**
- **Alignment marks**
  - **Very important**
  - **Clear chips: Critical in layers "all dark" as contact opening**





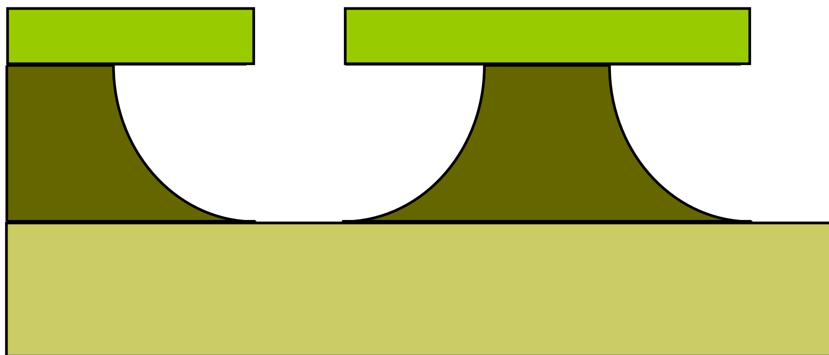
Etching

- Selectively remove of previously deposited material from top of wafers.
- Parameters:
  - Selectivity(For example: SiO_2 should be attacked but not photoresist and silicon)
  - Degree of Anisotropy (attack direction)
- Process:
  - Purely chemical vs. P. Physical (Selectivity vs. Anisotropy)
  - Wet Etching: wafers are exposed to liquid chemicals
  - Dry Etching: wafers are chemically etched in a gas at reduced pressure



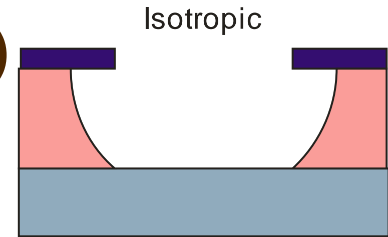
Wet etching

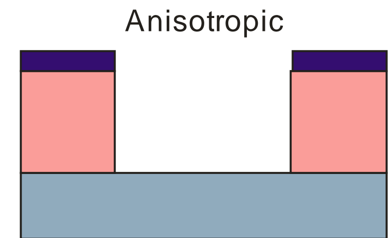
- Etching with wet chemical agents
- Used: to:
  - Surface cleaning
  - Complete removal of layers
  - Selective etching of layers

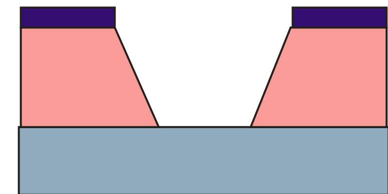


- Examples:
  - Cleaning: H2SO4, H2O, HCl
  - SiO2: HF + NH4F
  - Polysilicon: HF + HNO3
  - Al: H3PO4
- Needed:
  - High selectivity
  - High etching rate
- Characteristics:
  - Isotrope profile
  - Easy control
  - Dimension losses
  - No end point detection

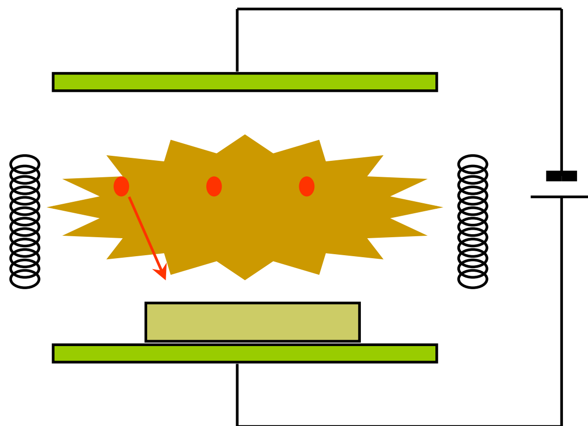
Dry etching: Reactive Ion Etching (RIE)

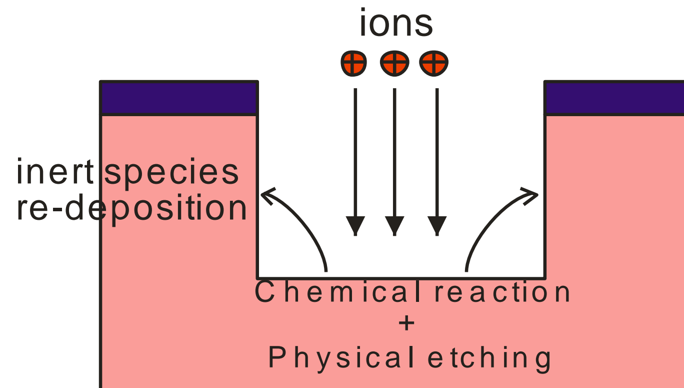






- RIE (also known as plasma etching) is a technique developed in the 80’s which combines simultaneous chemical and physical etching.
- Chemical reactants are excited to become a plasma by RF capacitively coupled and also accelerated in an electric field.

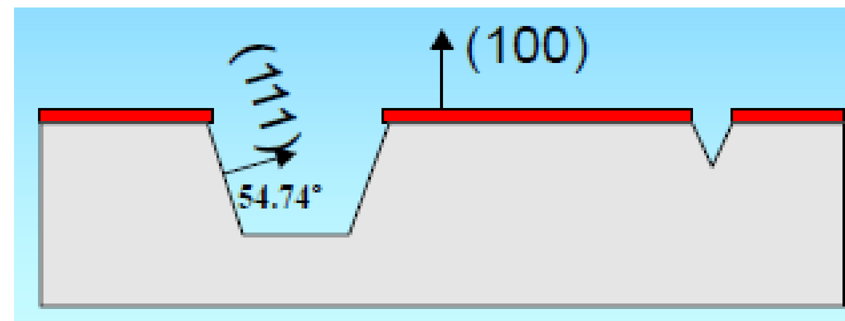


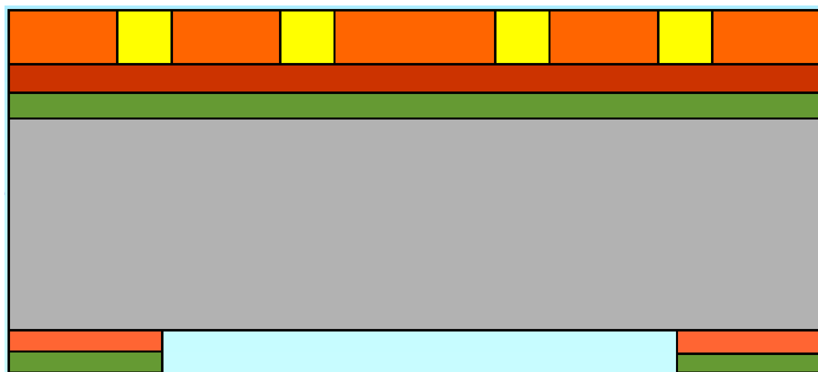


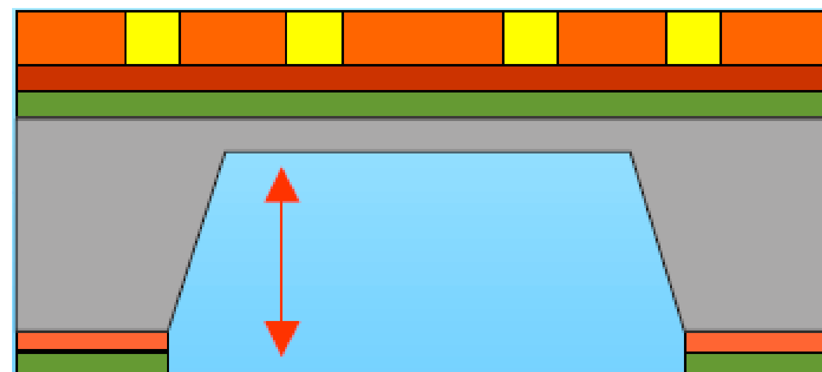
- Different degrees of anisotropy can be obtained modifying gas concentrations, pressure, RF power
- Some degree of re-deposition in the sidewalls which act as passivation allow finer control of etching profiles
- End point control possible by monitoring gas reactions

Anisotropic Si etching

- Etching through preferential crystalline planes
  - V(110)>V(100)>V(111)
- Wet etching with alcalis
  - KOH
  - TMAH (Tetra Metil Hydroxi Ammonia)



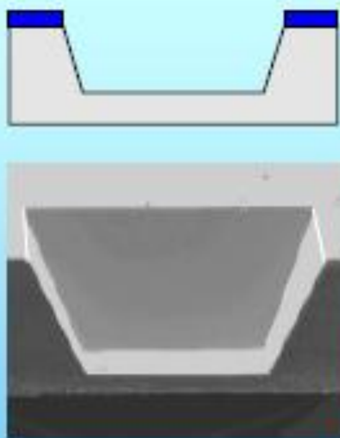




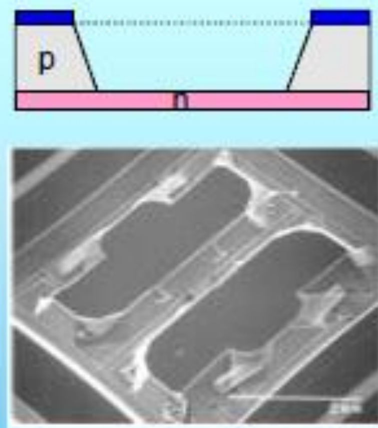
Anisotropic Si etching

- Difficulty: Etch stop at the required depth
- Stopping techniques:
  - Time
  - Inner layer
  - Highly doped P+ layer
  - Electrochemical: requires complex setup

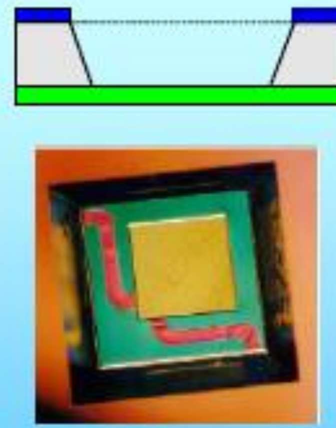
Time



Electrochemical



Inner layer (SOI for example)



Highly doped P+ layer