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ALICE Central Trigger System for LHC Run 3

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A major upgrade of the ALICE experiment is ongoing aiming to a high-rate data taking during LHC Run 3 (2022-2024).

The LHC interaction rate at Point 2 will be increased to 50 kHz kHz in Pb-Pb collisions and 1 MHz in pp collisions. ALICE experiment will be able to readout full interaction rate leading to an increase of the collected luminosity up a factor of about 100 with respect to the LHC Run 1 and 2. To satisfy these requirements a new readout system has been developed for most of the ALICE detectors allowing the full readout of the data at the required interaction rates without the need for a hardware trigger selection. A novel trigger and timing distribution system will be implemented based on Passive Optical Network (PON) and GigaBit Transceiver (GBT) technology. To assure backward compatibility a triggered mode based on RD12 TTC technology as the one used in the previous LHC runs will be maintained and re-implemented under the new Central Trigger System (CTS). A new universal ALICE Trigger Board (ATB) based on the Xilinx Kintex Ultrascale FPGA has been designed to function as a Central Trigger Processor (CTP), Local Trigger Unit (LTU), and monitoring interfaces.

In this paper, this hybrid multilevel system with continuous readout will be described, together with the triggering mechanism and algorithms. An overview of the CTS, the design of the ATB and the different communication protocols will be presented.

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