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Silicon pixel-detector R&D for future lepton colliders

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The physics aims at future lepton colliders such as CLIC or FCC-ee pose challenging demands on the performance of the proposed all-silicon vertex and tracking-detector systems. A single-plane spatial resolution of a few micrometers is needed, combined with a low mass of $\sim 0.2\%$ X_0 per layer for the vertex detectors and $\sim 1\%$ X_0 per layer for the main trackers. Moreover, hit-time tagging with a few nanosecond resolution is required for CLIC, to reduce the impact of beam-induced background on the measurement accuracy to an acceptable level. An even better timing precision below 100 ps on pixel level would improve the background rejection further, and opens up the possibility of particle-identification by time of flight measurements within the tracking layers.

To address these detector requirements, a broad R&D program on new silicon detector technologies is being pursued within various collaborative frameworks, such as the CERN EP R&D programme, AIDAInnova and the CLICdp collaboration. Different small pitch (25 micron) hybrid technologies with innovative sensor concepts are explored as candidates for the inner vertex-detector layers. A dedicated 65 nm readout chip (CLICpix2) has been developed and interconnected via fine pitch bump-bonding to 50-150 micron thin planar active-edge sensors. Furthermore, alternative interconnects such as bonding using anisotropic conductive films (ACF) are explored. Fully monolithic CMOS technologies are considered both for the vertex and the tracking detectors. Based on 3D TCAD simulations and previous test results, innovative concepts for CMOS sensors with a small collection electrode have been developed, targeting various future projects. Several prototype chips have been produced using variants of a modified 180 nm CMOS process with different substrate materials. The CLICTD tracker demonstrator design includes an innovative sub-pixel segmentation scheme for a readout pitch of 300 micron x 30 micron. An extensive test-beam measurement campaign has been performed to compare the various CLICTD design and processing variants. Recent measurements with the ATTRACT FASTPIX timing demonstrator produced in the same 180 nm CMOS process have demonstrated the feasibility of performing time tagging on single-hit level with a precision of approximately 100 ps for a pixel pitch of 20 micron and below. Similar concepts are currently being explored in a 65 nm CMOS process offering further performance improvements. To predict and optimise the performance of the various prototype technologies, a fast and versatile Monte Carlo Simulation Tool (Allpix-Squared) has been developed.

This contribution introduces the requirements and gives an overview of the R&D program for silicon-based vertex and tracking detectors at future lepton colliders, highlighting new results from measurements and simulations of recent prototypes.

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