High performance data acquisition and processing based on programmable SoC for multichannel particle detectors

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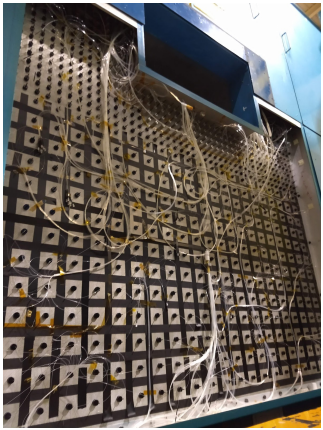
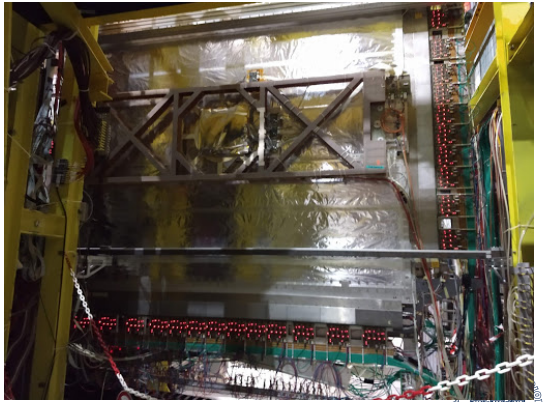
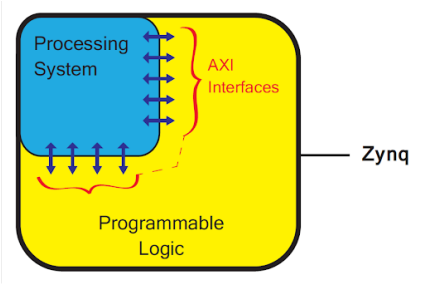
Modern high energy physics experiments are characterized by a large number of detectors with huge amount of channels ($> 10^4$) which produce extremely large amount of data per unit of time (e.g. TB/s). All these data must be acquired and processed online in order to apply complex algorithms for data reduction and filtering before storage for subsequent offline data analysis.



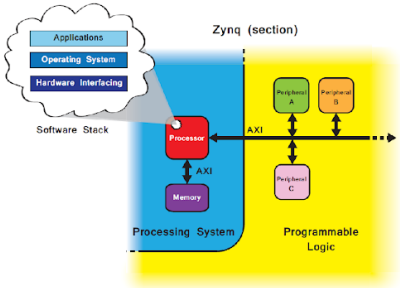
An important contribution for solving these challenges can in principle be provided by fully programmable systems on chips tightly integrating FPGA fabrics with multi-core processors (e.g. Xilinx Kintex Ultrascale or Intel Cyclon V SoC FPGA).



All-Programmable System-on-Chip (SOC)

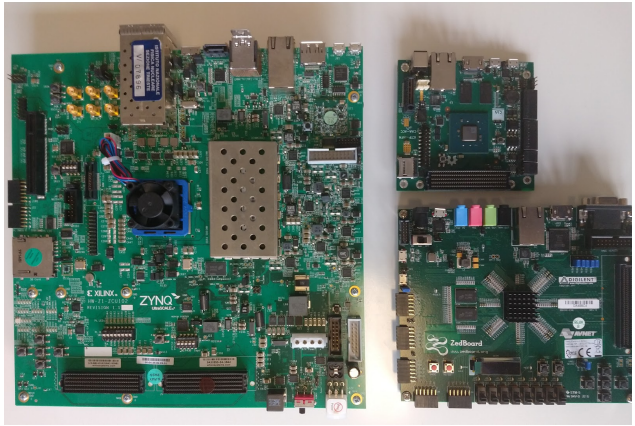


A simplified model of the Zynq architecture

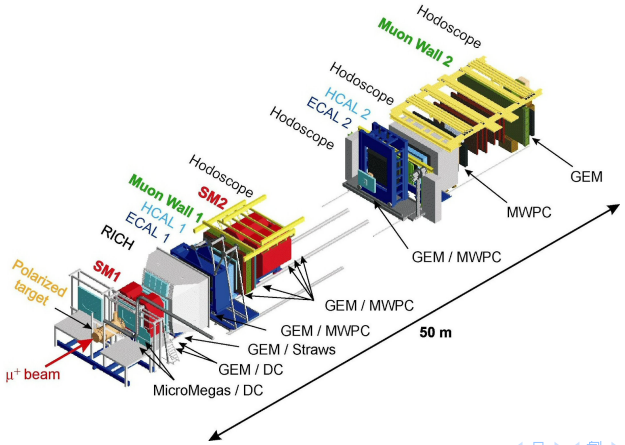


Relationship of the software system, hardware system and Zynq architecture

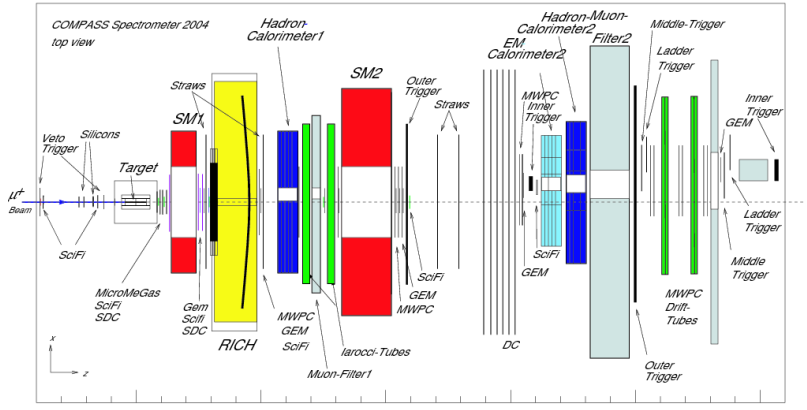
Development Boards



COMPASS Experiment



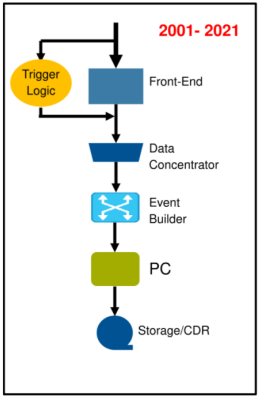
COMPASS Experiment

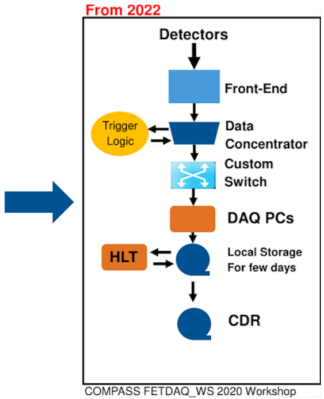


Traditional vs Free Running DAQ

Current COMPASS DAQ

- 20 years old electronics
- Maximum trigger rate capability 40 kHz
- Depends on analog Trigger Logic Electronics



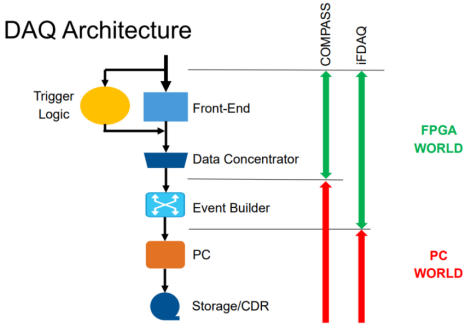


DAQ beyond 2020 requirements :

- 100kHz trigger rate
- Complex trigger algorithms
- Free running DAQ requires a continuous data stream from the r-o channel.

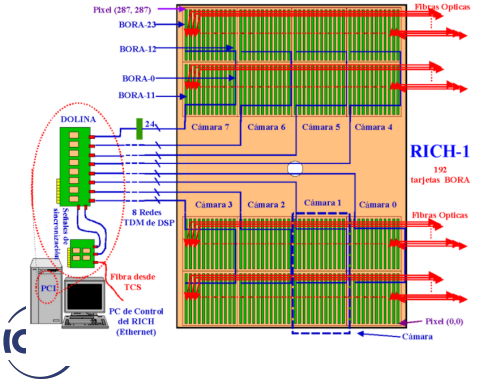
Traditional vs Free Running DAQ

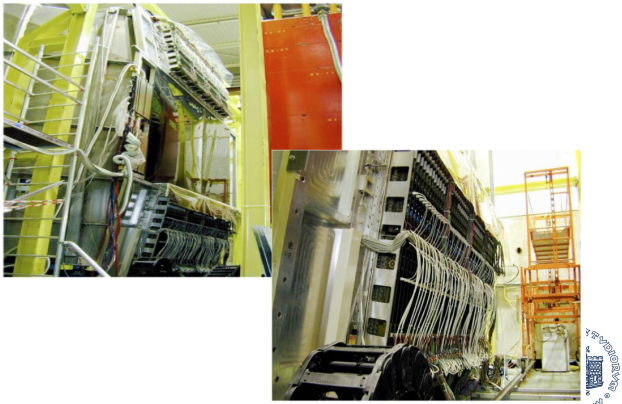
- **Triggered DAQ**
- Event data acq
- Takes a “picture” of all channels at the same time
- Big amount of data per event



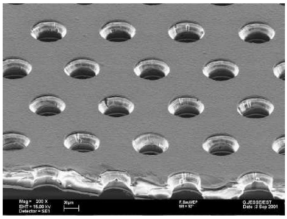
- **Free Running DAQ**
- Features extraction
- Triggerless DAQ
- Reduce data congestion
- Continuous data acq.
- Detection per Channel

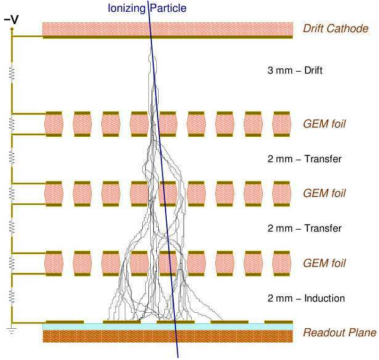
RICH Detector



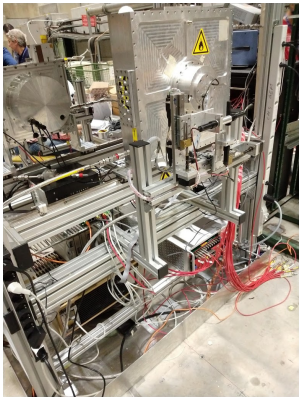


Gas Electron Multipliers





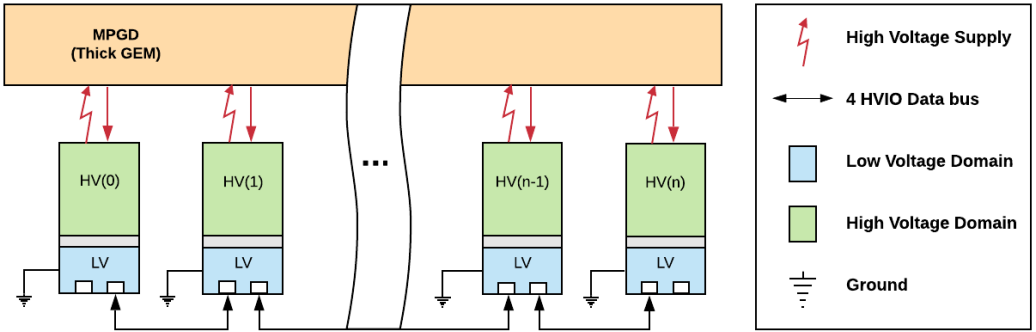
Micro Pattern Gasseous Detectors



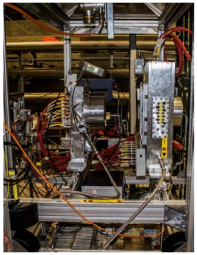
Thick GEM Detector setup
CERN 2018

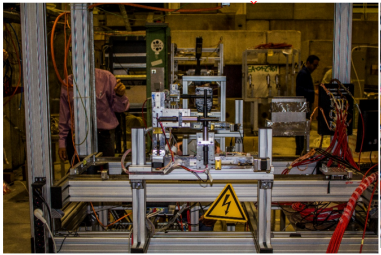
Micro-Pattern Gaseous Detectors (MPGDs), namely Gaseous Electron Multipliers (GEMs) need different voltages up to several kV for biasing the device electrodes. The absolute voltage among channels may be up to 2 kV making a direct galvanic connection among them impossible.
Wireless communication is not recommended to prevent electromagnetic noise interference in the detector.

To avoid electronic noise propagation in the detector, each channel is required to be connected in the HV power domain with independent floating power supplies.



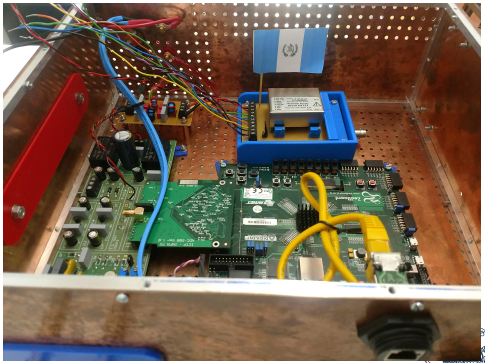
HVPSS V 0.1





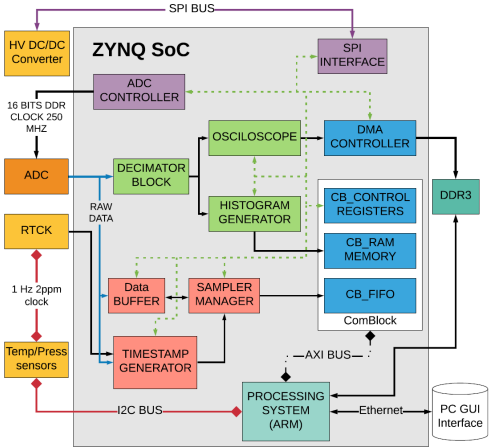
High Voltage Power Supply System (HVPSS) based on SoC-FPGA

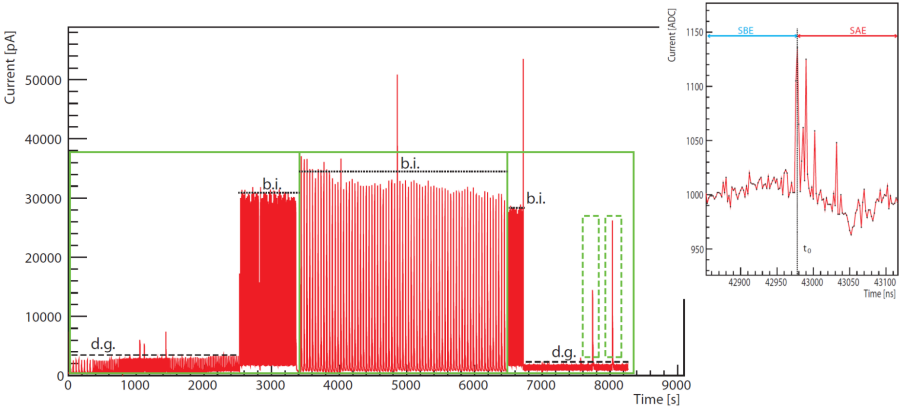
- Provide high voltage to each segment of the MPGD (up to 2kV).
- Monitoring the low current variations (10 pA) in the MPGD.
- Detect and timestamp high speed voltage transients (2 ns).
- Communicate with other HVPSS channels and adjust the HV accordingly.



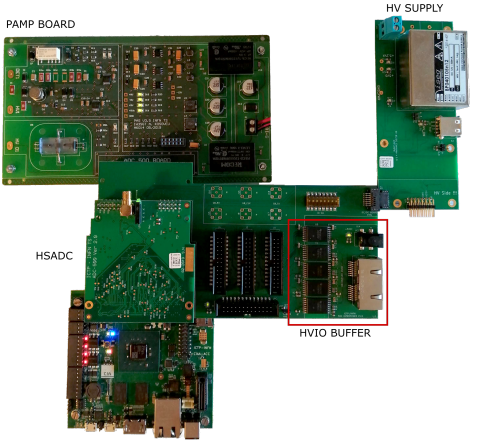
HVPSS v0.1

FPGA System


SPI BUS
HV DC/DC Converter
ZYNQ SoC
SPI INTERFACE
ADC CONTROLLER
16 BITS DDR CLOCK 250 MHZ
OSCILOSCOPE
DMA CONTROLLER
ADC
DECIMATOR BLOCK
DDR3
RAW DATA
HISTOGRAM GENERATOR
CB_CONTROL REGISTERS
RTCK
CB_RAM MEMORY
1 Hz 2ppm clock
Data BUFFER
SAMPLER MANAGER
CB_FIFO
ComBlock
Temp/Press sensors
TIMESTAMP GENERATOR
AXI BUS
PROCESSING SYSTEM (ARM)
Ethernet
PC GUI Interface
I2C BUS

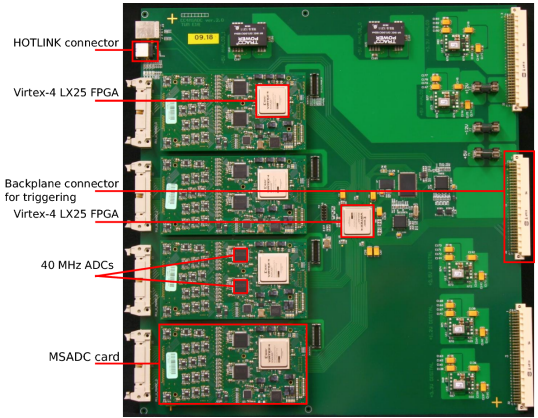

Current [pA]
50000
40000
30000
20000
10000
0
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
Time [s]
d.g.
b.i.
b.i.
b.i.
d.g.
Current [ADC]
1150
1100
1050
1000
950
SBE
SAE
t_0
42900
42950
43000
43050
43100
Time [ns]

HVPSS v1.0


PAMP BOARD
HV SUPPLY
HSADC
HVIO BUFFER
ZYNQ 7030 CIAA-ACC BOARD

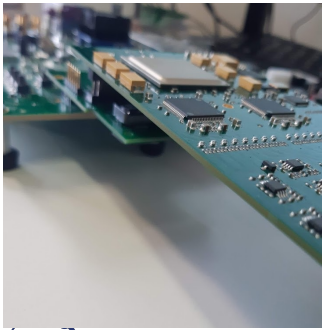
ECAL2 Readout System

ECAL2 Readout System, Original Triggered DAQ



- MSADC
  - 16 Channels @ 80MHz
  - 12 bits Digitalization
  - Interleaving
  - Multiplexing
  - Zero suppression
  - Formatting
- Carrier Design
  - Combines 4 MSADC
  - Power supply
  - Multiplexing
  - Transmit Data
  - Interface

ECAL2 Readout System, Proposed Trigger-less DAQ



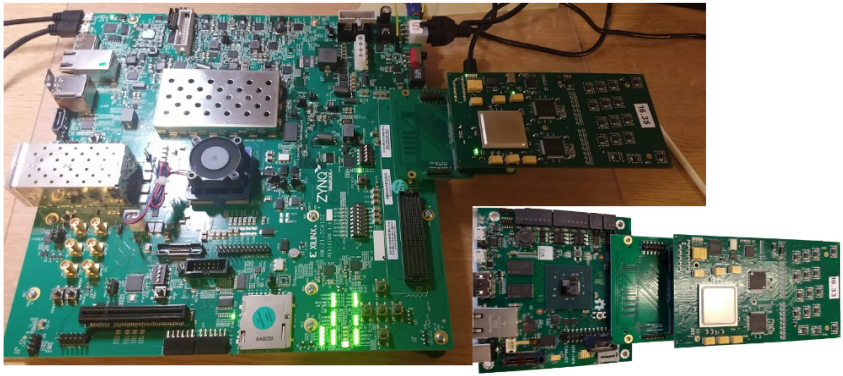
ECAL2 requirements (arrival time and amplitude)

- Feature extraction
- Pedestal calculation
- Signal detection
- Noise characterization

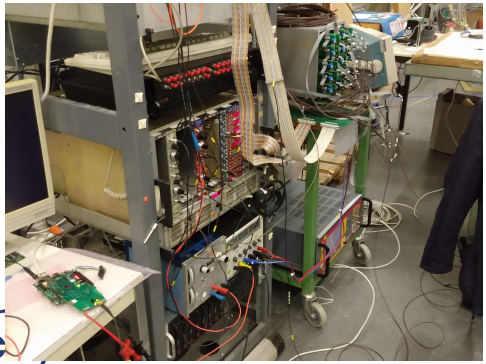
First steps on Trigger-less DAQ FPGA-SoC based system

- Long data traces retrieval required for noise analysis
- Study of each of the analog channels individually
- Portable MSADC readout system for testing
- Continuous data stream from the MSADC
- SFP+ Gigabit communication to transmit the data stream

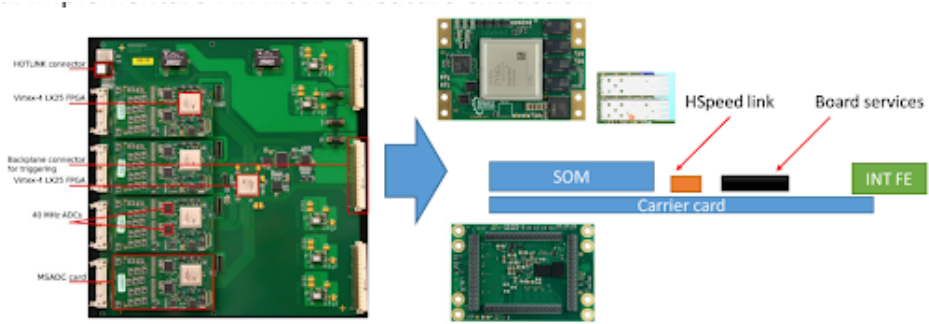
MSADC SoC Tests



ECAL2 DAQ Using SoC



FPGA SOC System On Module Exploration

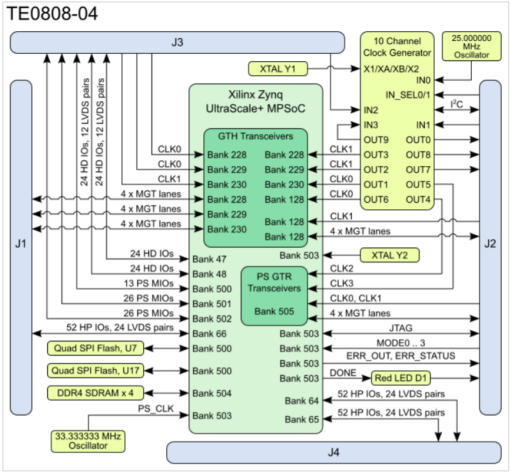


Positive aspects of SOMs

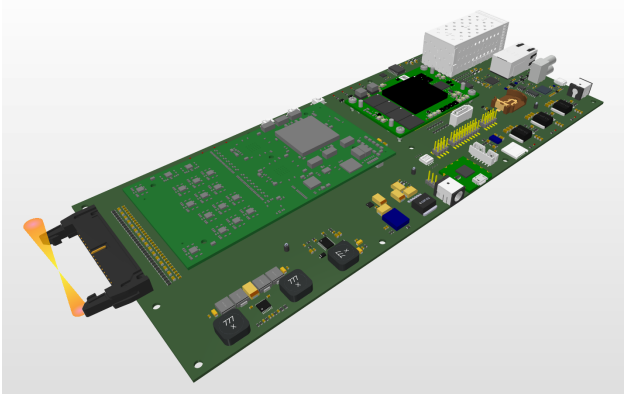
- To encapsulate a complex SoC FPGA along with essential common components in order to facilitate the design of large hardware systems avoiding risk of errors related to critical interconnections such as between SoC FPGA and DDR memories.
- To standardize a board to board connection to facilitate hardware upgradeability, partial replacement and interchangeability.
- To allow the HW designer to concentrate the efforts on the application specific aspects, relaying on an error-free partial system module.
- Availability of several affordable commercial solutions and design support.

Potential issues due to the quality of the board-to-board connectors

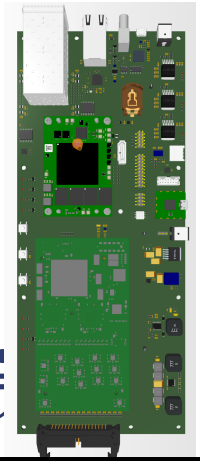
- Some signals may experience speed degradation if choose unfit connectors.
- Initial extra cost increase
- Electrical connection reliability
- Precise and reliable mechanical mounting may need securing screws.


TE0808-04
J3
J1
J2
J4
10 Channel Clock Generator
25.000000 MHz Oscillator
XTAL Y1
X1/XA/XB/X2
IN0
IN_SEL0/1
I²C
IN2
IN3
IN1
OUT9
OUT0
OUT3
OUT8
OUT2
OUT7
OUT1
OUT5
OUT6
OUT4
Xilinx Zynq UltraScale+ MPSoC
GTH Transceivers
24 HD IOs, 12 LVDS pairs
24 HD IOs, 12 LVDS pairs
CLK0
CLK0
CLK1
4 x MGT lanes
4 x MGT lanes
4 x MGT lanes
Bank 228
Bank 229
Bank 230
Bank 228
Bank 229
Bank 230
Bank 228
Bank 128
Bank 128
Bank 128
CLK1
CLK1
CLK0
CLK0
CLK1
4 x MGT lanes
24 HD IOs
24 HD IOs
13 PS MIOs
26 PS MIOs
26 PS MIOs
52 HP IOs, 24 LVDS pairs
Bank 47
Bank 48
Bank 500
Bank 501
Bank 502
Bank 66
Bank 503
XTAL Y2
PS GTR Transceivers
Bank 505
CLK2
CLK3
CLK0, CLK1
4 x MGT lanes
JTAG
MODE0 .. 3
ERR_OUT, ERR_STATUS
Quad SPI Flash, U7
Quad SPI Flash, U17
Bank 500
Bank 500
Bank 503
Bank 503
Bank 503
DONE
Red LED D1
DDR4 SDRAM x 4
Bank 504
PS_CLK
Bank 503
Bank 64
Bank 65
52 HP IOs, 24 LVDS pairs
52 HP IOs, 24 LVDS pairs
33.333333 MHz Oscillator

MSADC SOM Card



MSADC SOM Card

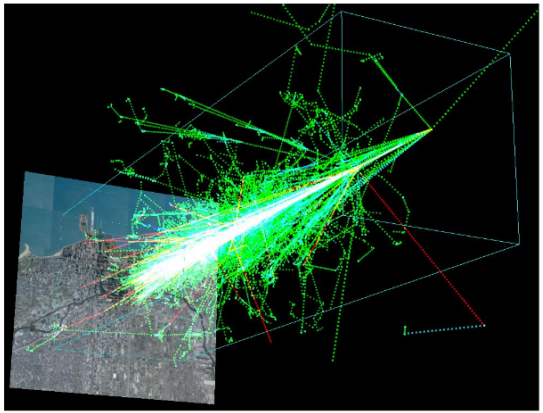


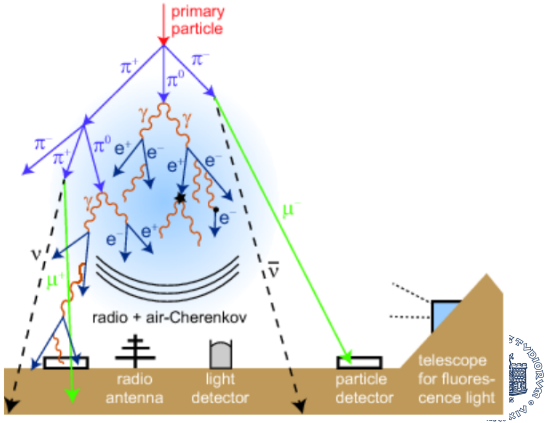
- Characteristics
- Fully populated MSADC pin support.
- Baseboard for Xilinx Zynq Ultrascale+ MpSoC.
  - Compatible with Trenz UltraSoM+ modules TE0808 and TE0803.
  - Zynq Ultrascale+ ZCU4EV to ZCU15EG.
- 4 SFP+ Connectors for data transmission up to 16.3Gb/s* each.
- Ethernet connection to embedded microprocessor.
- USB-UART interface.
- 3 different boot mode.
  - JTAG (Daisy chained with MSADC and SoM, or independent)
  - QSPI32 Flash Memory
  - SD Card.
- 2 LEMO Connectors (In and Out)
- SATA interface.

*According Xilinx GTH specifications, to be tested on board.

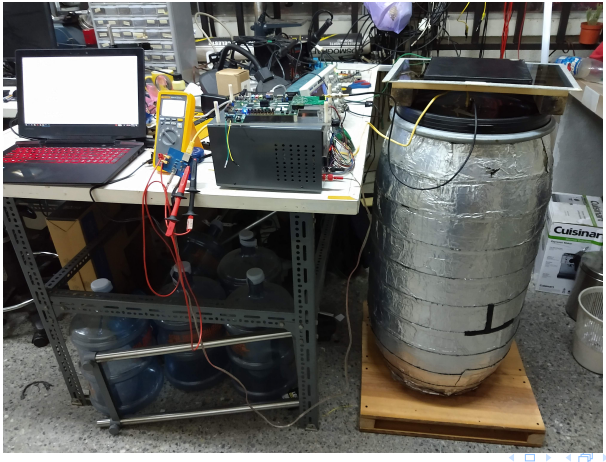
Other applications

Cosmic Rays Studies





ADC500 + Zedboard Setup USAC



Thanks for your attention.