# The Mu3e Tile Detector: From prototype to pre-production

**HighRR Seminar** 

December 09, 2020

Hannah Klingenmeyer

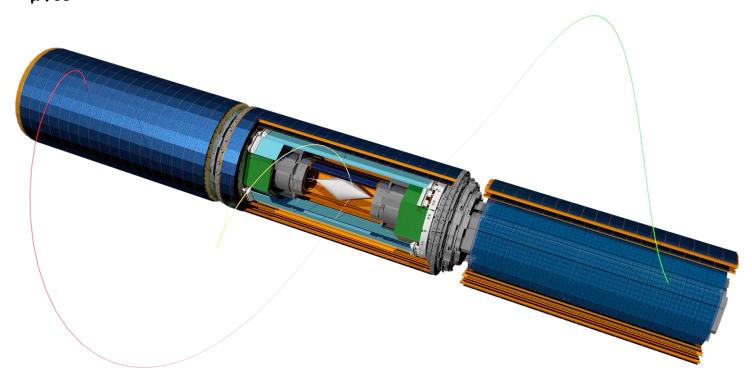
**Kirchhoff-Institute for Physics** 

- Introduction to the Mu3e experiment
- The tile detector: technical prototype and new design
- Production steps and methods
- Validation of new design
- Pre-production setup and plans

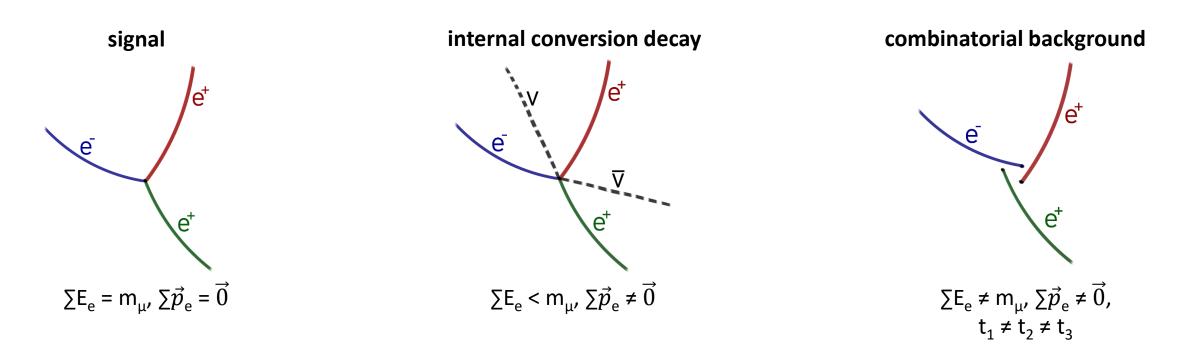
### Introduction to the Mu3e experiment

### The Mu3e experiment

- search for cLFV decay  $\mu^{\scriptscriptstyle +} \rightarrow e^{\scriptscriptstyle +} e^{\scriptscriptstyle +} e^{\scriptscriptstyle -}$ 
  - SM (including v mixing):  $B_{\mu \rightarrow 3e} \approx 10^{-54}$
- current upper limit:  $B_{\mu \rightarrow 3e} < 10^{-12}$  (SINDRUM, 1988)  $\rightarrow$  aim of Mu3e:  $B_{\mu \rightarrow 3e} < 10^{-16}$
- stopping target experiment at PSI in Switzerland  $\rightarrow$  muon beam rate: 10<sup>8</sup> µ/s
- first commissioning run in 2021

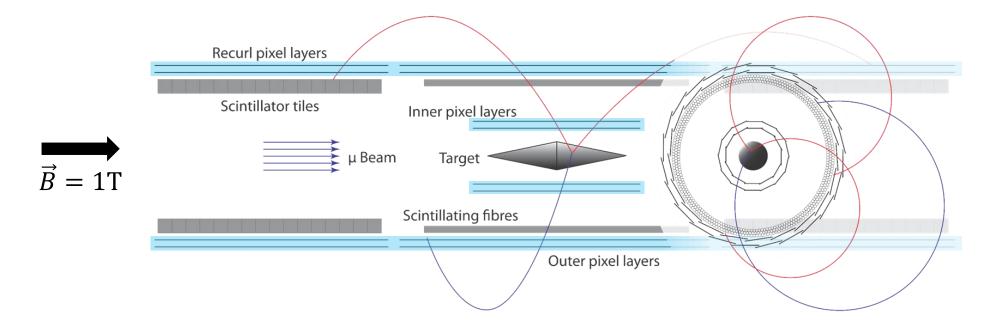


- background sources for  $\mu \rightarrow eee$ :
  - internal conversion  $\mu \rightarrow eeevv \implies$  reject via precise momentum measurements



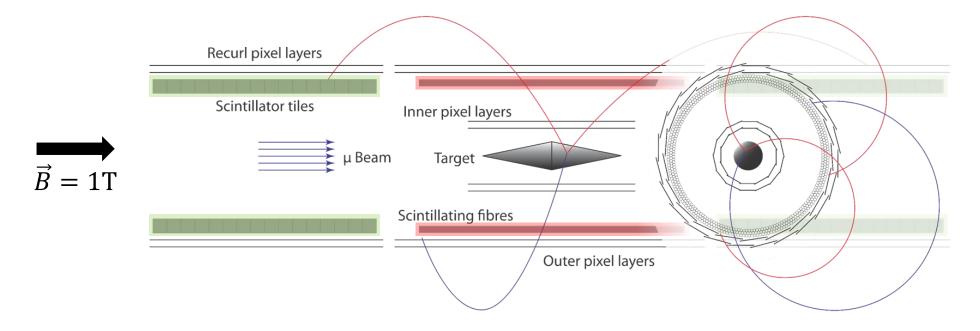
- background sources for  $\mu \rightarrow eee$ :
  - internal conversion  $\mu \rightarrow eeevv \implies$  reject via precise momentum measurements
  - combinatorial background reject via precise time and vertex determination

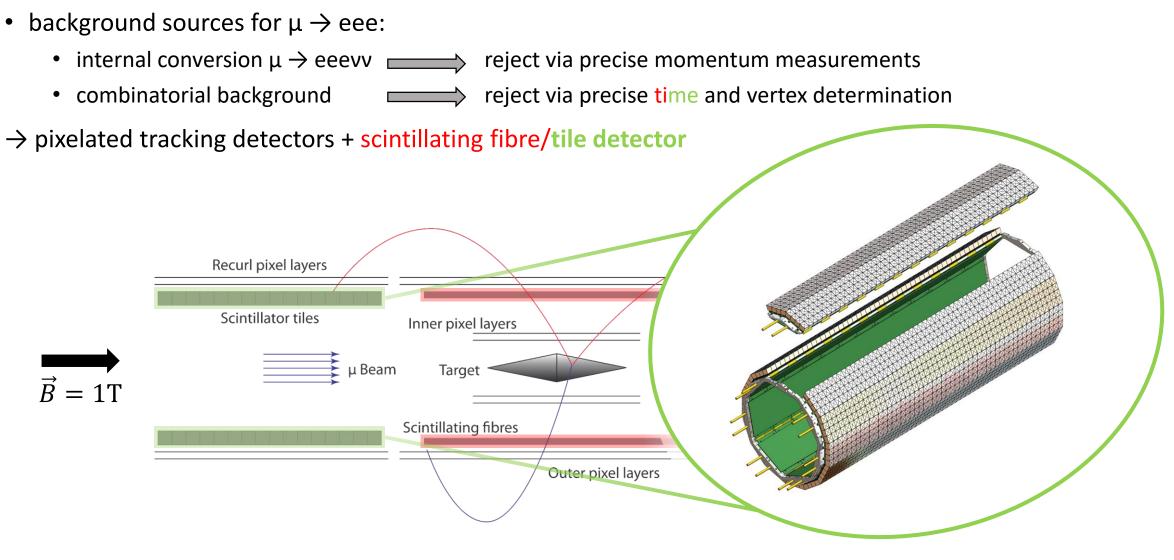
→ pixelated tracking detectors + scintillating fibre/tile detector



- background sources for  $\mu \rightarrow eee$ :
  - internal conversion  $\mu \rightarrow eeevv \implies$  reject via precise momentum measurements
  - combinatorial background reject via precise time and vertex determination

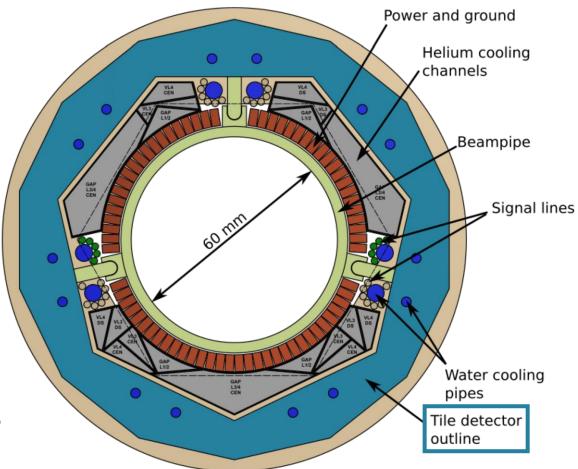
→ pixelated tracking detectors + scintillating fibre/tile detector





### Tile detector overview

- main challenges for detector design:
  - continuous read-out at high rates ( $10^8 \mu/s$ )
  - compact experiment layout → limited space
- tile detector requirements and implications:
  - timing resolution  $\leq 100 \text{ ps}$
  - high granularity
  - up to 80 kHz per channel
  - limited space for electronics, services, ...
  - operate in high magnetic field and helium atmosphere



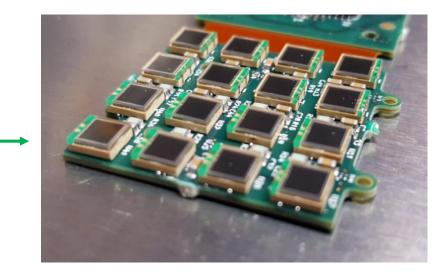
### Detector structure I

- basic detector components:
  - plastic scintillator tiles
  - silicon photomultipliers (SiPMs)
  - MuTRiG: custom-designed ASIC developed in Heidelberg

### → resulting base-unit: **submodule**

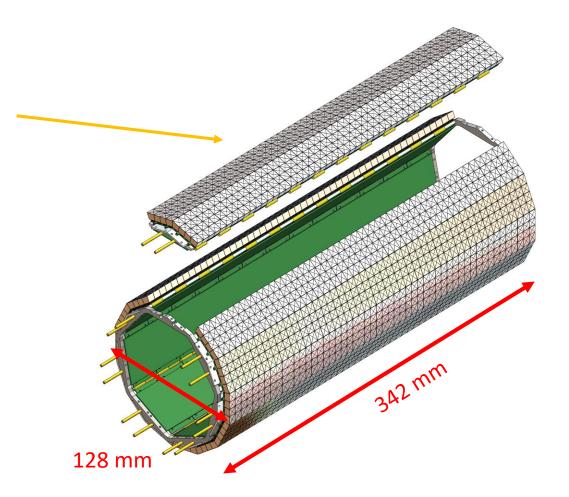
- 32 channels (tiles + SiPMs)
- one MuTRiG
- custom-designed PCB with flex-print





### Detector structure II

- module:
  - 13 submodules  $\rightarrow$  416 channels
  - aluminium support and cooling structure
  - aluminium pipes (water cooling)
  - one read-out board
- recurl station:
  - 7 modules
  - one pair of endrings (PEI or similar material)
- $\rightarrow$  two recurls stations = full tile detector



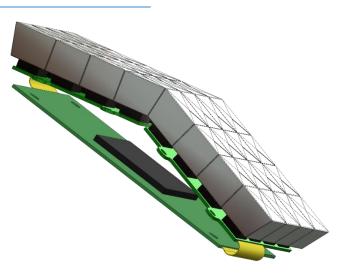
### The tile detector

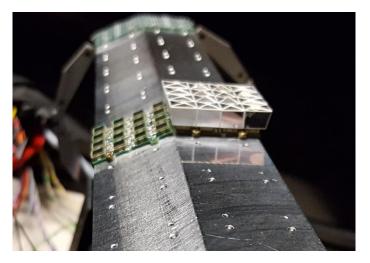
Technical prototype and new design

### First technical prototype

- first technical prototype: 3 submodules
  - development of production and assembly procedures
  - cooling system test
- succesful testbeam campaigns @ DESY in February and June 2018
  - prototype fully functional
  - time resolution clearly below 100 ps

see HighRR talk by Tiancheng Zhong from January 2019

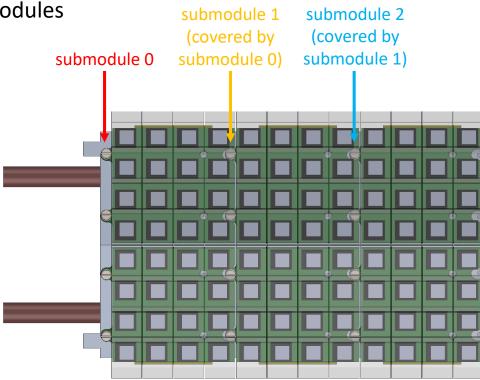




### Design modification

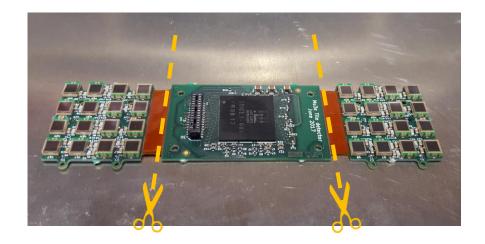
- challenges during prototype production:
  - assembly screws are covered by next submodule
    - $\rightarrow$  submodule failure could require removing large number of submodules
  - assembly to cooling plate difficult because of flex-print
    → risk of damaging tiles
- change in size required for experiment integration
  - length reduction  $\rightarrow$  integration with pixel detector endrings
  - "slimming" in radial direction -

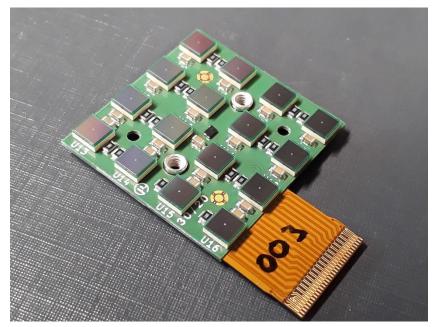




### New design

- "cut up" submodule:
  - two separate 4x4 tile matrices
  - MuTRiG moved to read-out board
    - $\rightarrow$  replace board in case of ASIC failure without affecting detector parts

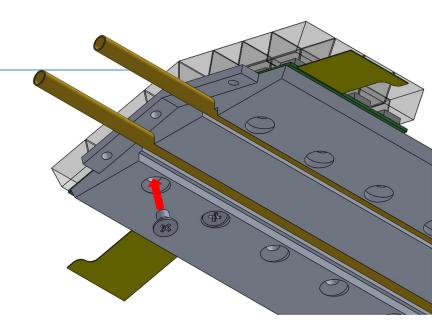


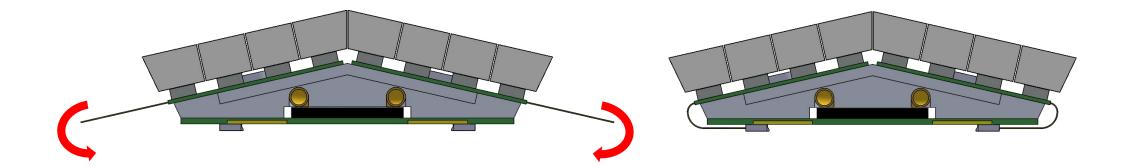


board design by Yonathan Munwes

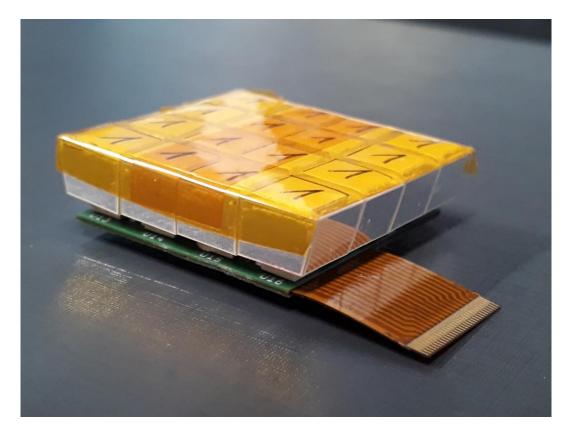
### New assembly method

- assembly of tile matrix:
  - threaded spacers assembled to matrix PCB
  - assembly from bottom-side through cooling plate
  - ightarrow cooling plate re-design
- new low-profile connector
  - soldered to read-out board
  - directly connect flex-print

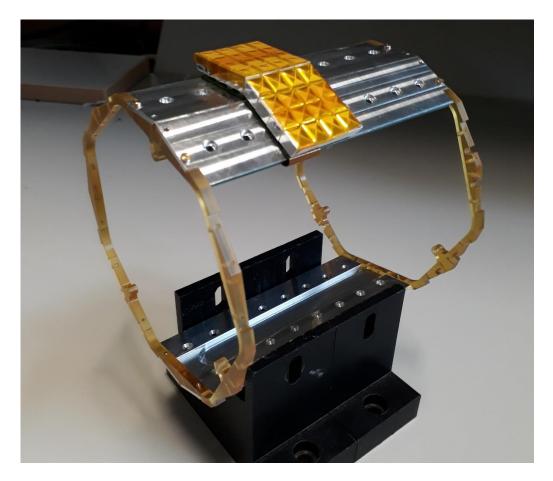




### New prototype

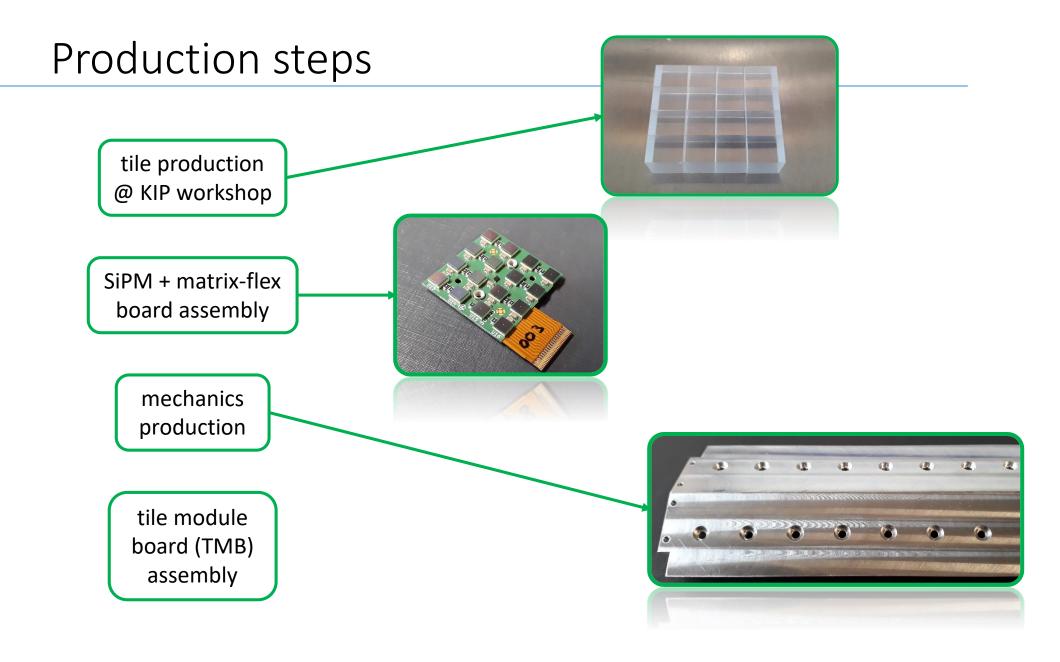


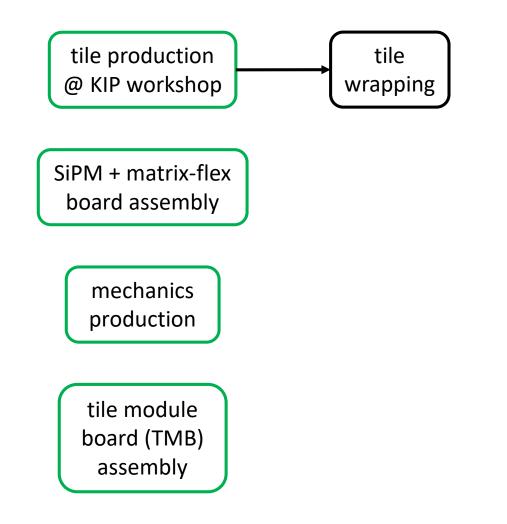
4x4 matrix with wrapped tiles and SiPMs, using new matrix design

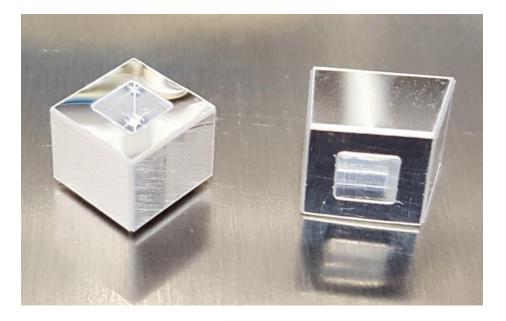


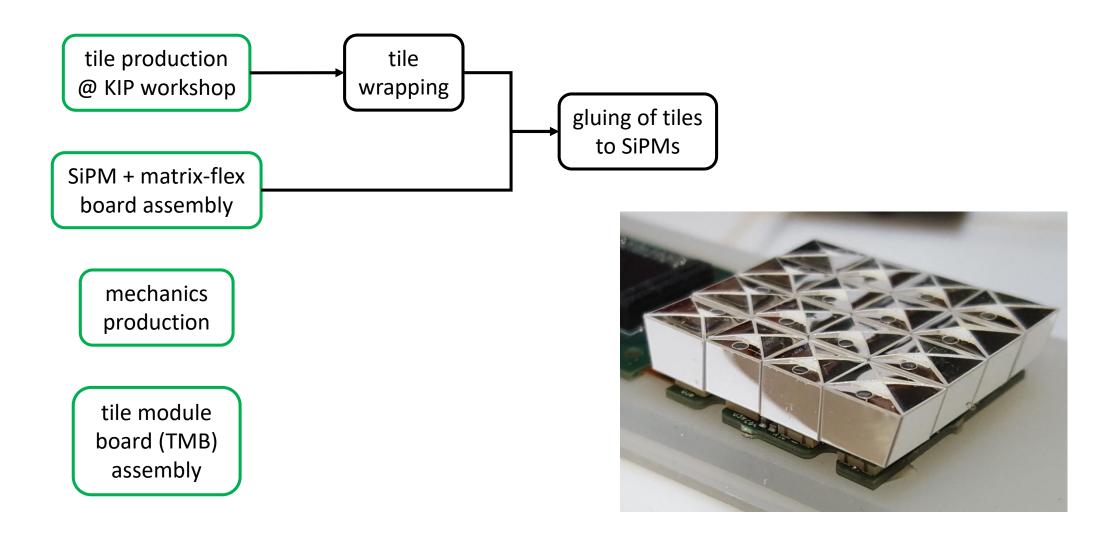
assembly test with PEI endrings and shortened cooling plate

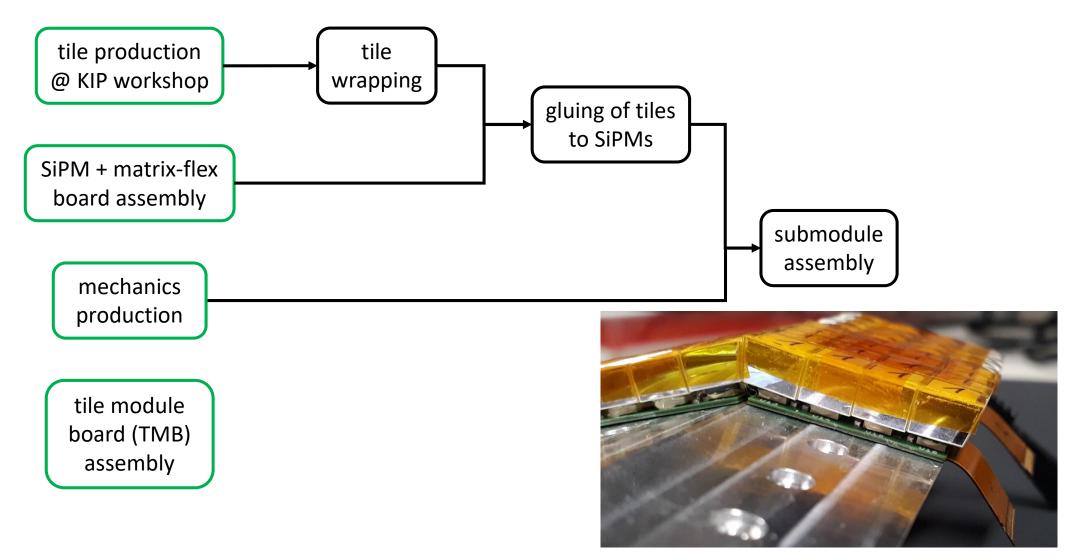
## Production steps and methods

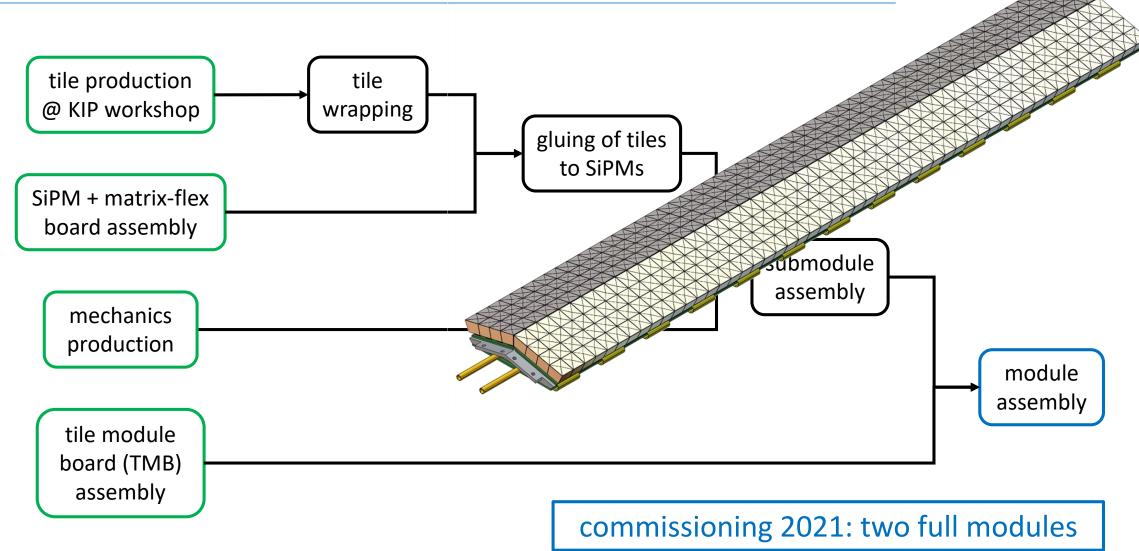








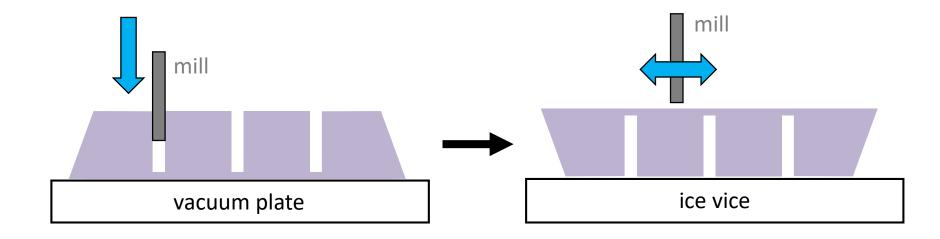




- number of tiles for two recurl stations: 5 824 tiles  $\rightarrow$  6.5k tiles
- first technical prototype: 100 tiles produced in **70 working hours** @ KIP workshop
  - all faces diamond-milled from the top
  - can only work on two tiles at the same time
- $\rightarrow$  effort to improve production time @ KIP workshop
- idea: use "ice vice" ("Gefrierspanner") system
  - $\rightarrow$  mill many tiles at once

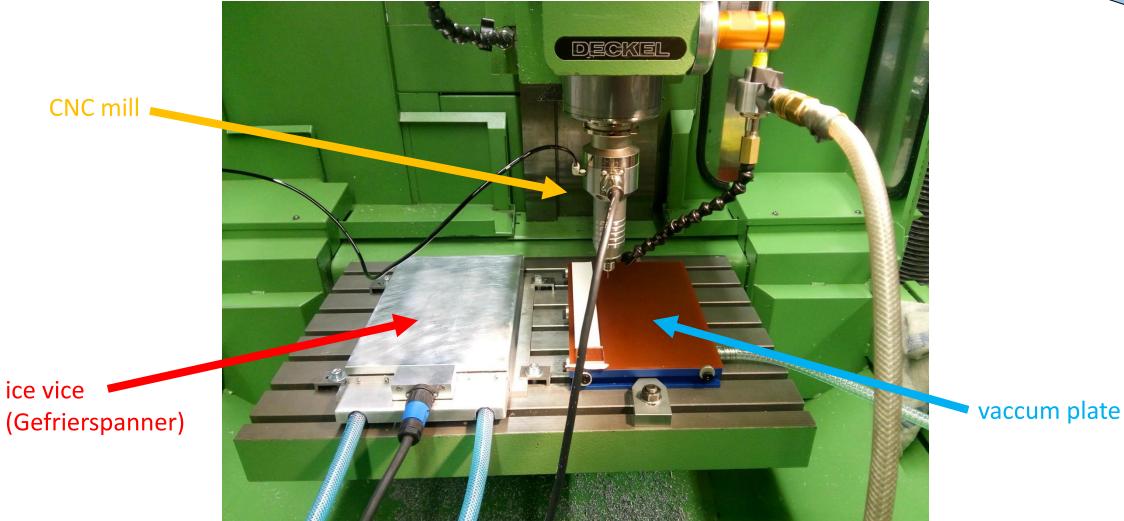
### The ice vice

- basic idea: freeze small parts to a plate to hold them in place during machining (-10°C)
- plate size: 200 mm x 300 mm
  - $\rightarrow$  could clamp down ~ 100 tiles at once
- one step further: cut out a full matrix from scintillator plate



### Tile production setup @ KIP workshop





(Gefrierspanner)

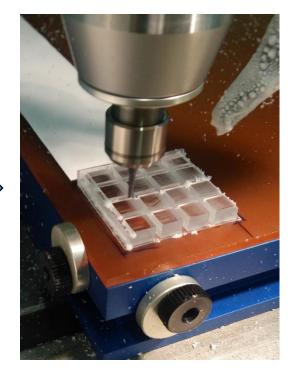
HighRR Bi-weekly Seminar

### 09.12.2020

# vertical milling

# Vacuum plate milling

- milling of edge tiles:
  - step-wise milling with regular mill head
  - final milling with custom-made conical mill head

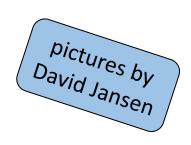


H. Klingenmeyer

### horizontal milling

### milled matrix with 0.5 mm leftover material

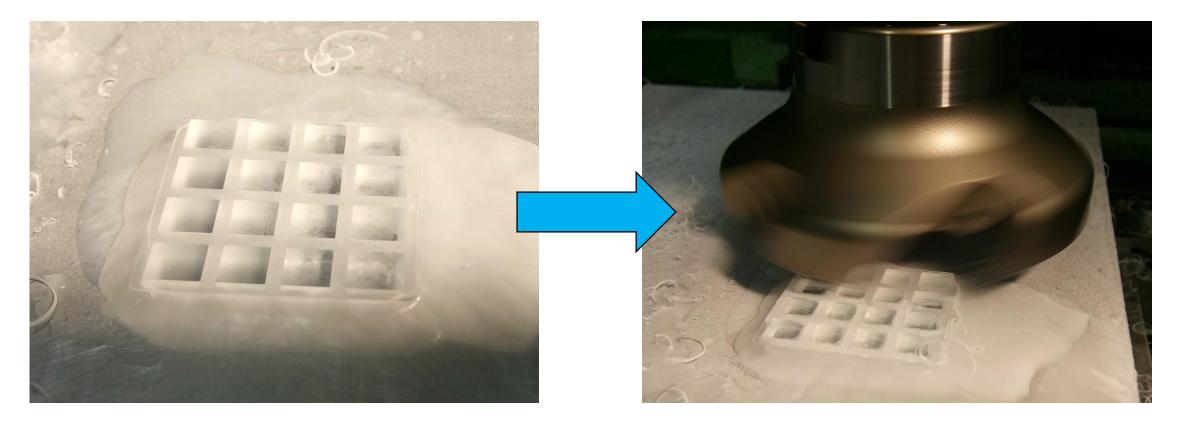




### Ice vice milling



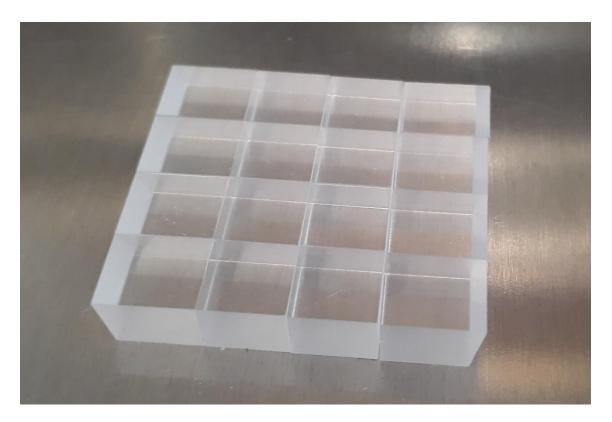
mill away leftover material from the top



pictures by David Jansen

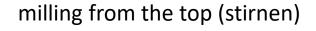
### Final matrix

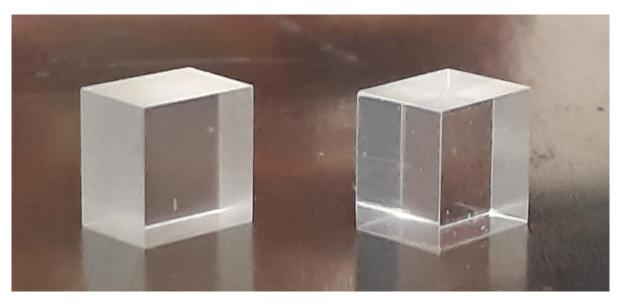
- production time per matrix < **30 minutes**
- reminder: we need 26\*7\*2 = 364 matrices for Mu3e Phase I
  - $\rightarrow$  2-3 months production time  $\checkmark$

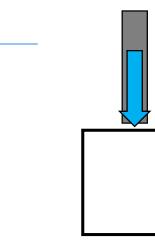


- price to pay for fast milling: "dull" side faces
  → effect on light yield and timing?
- idea: compare clear-surface matrix with dull-surface matrix
  - $\rightarrow$  testbeam at DESY
- alternative: mill all faces from the top
  → slower, but still realistic time frame (6 months)

milling from the side (walzen)





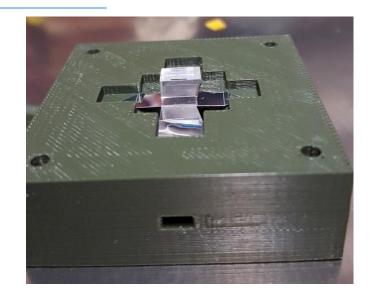


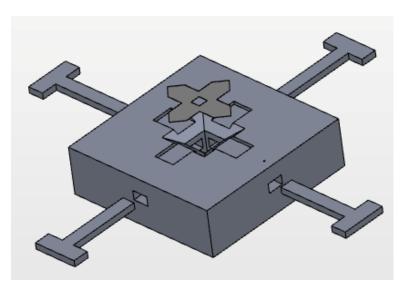
H. Klingenmeyer

# Tile wrapping

- wrapping of tiles with reflective foil to reduce optical cross-talk
- origignal wrapping tool design using CAD software
  - $\rightarrow$  3D-printed prototype
  - → "upgrade" to (semi-)automatic solution for easier handling and faster production

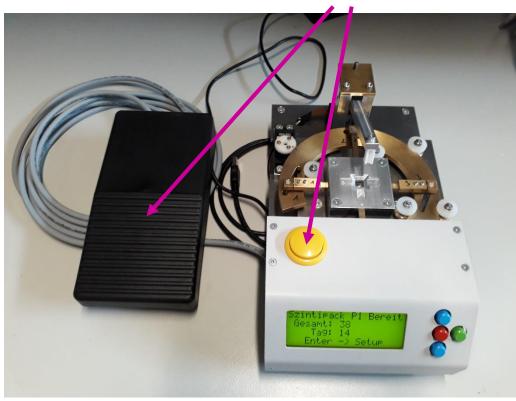


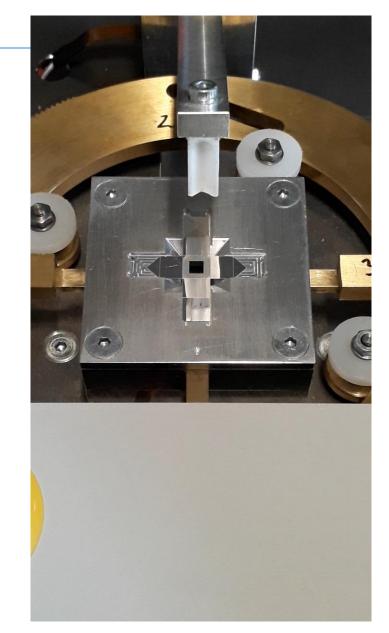




### Semi-automatic wrapping tool

- constructed by Knut Azeroth (electronics workshop) and Christian Herdt (mechanical workshop)
- wrapping sequence controlled by Arduino
  - move through sequence by pressing "Enter"

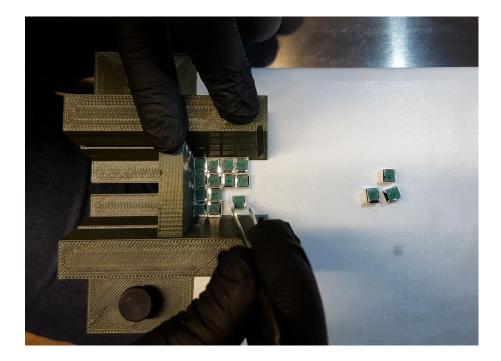


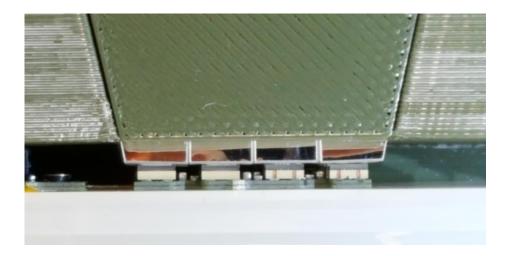


# Tile gluing

- attach tiles to SiPMs using light-transmitting glue
- glue full tile matrix (4 x 4 tiles) all at once
- 3D-printed prototype

 $\rightarrow$  production of final tools @ KIP workshop

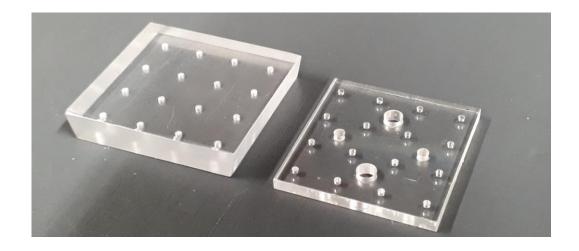


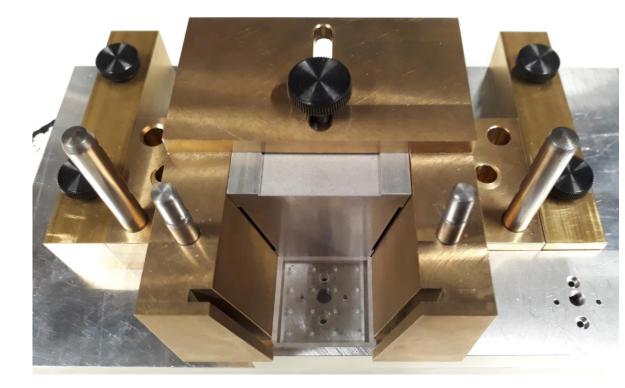




# Final gluing tool

- four gluing tool stations produced @ KIP workshop
  → used for new matrix prototype
- alignment of tool to pedestal using tile matrix and SiPM mock-ups (plexiglass)
  - circles mark centres of tiles and SiPMs, respectively
  - align under microscope
  - to ensure alignment of foil window to SiPM





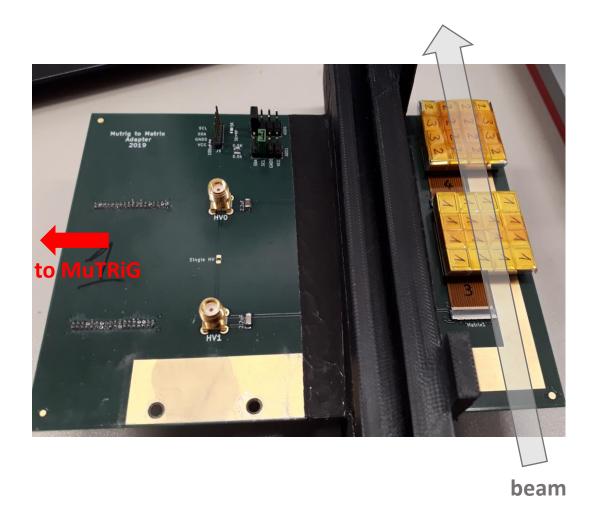
### Validation of new design

### Timing measurements at DESY testbeam

- produced four matrices using new design
  - different tile surface qualities
  - different tile heights (5.0 mm and 4.5 mm)

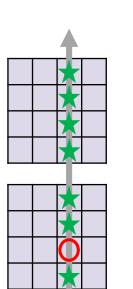
 $\rightarrow$  investigate effect on timing

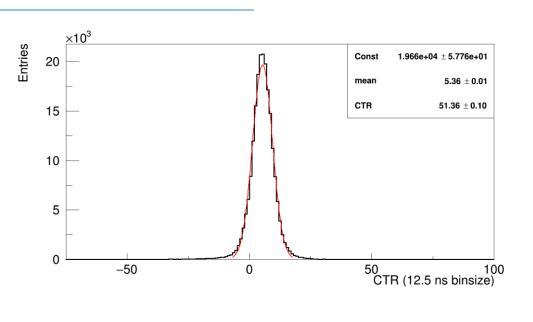
- SiPM read-out using standalone MuTRiG setup
  - only 2 matrices (32 channels) at once
  - $\rightarrow$  matrices switched during testbeam



### Timing calculation

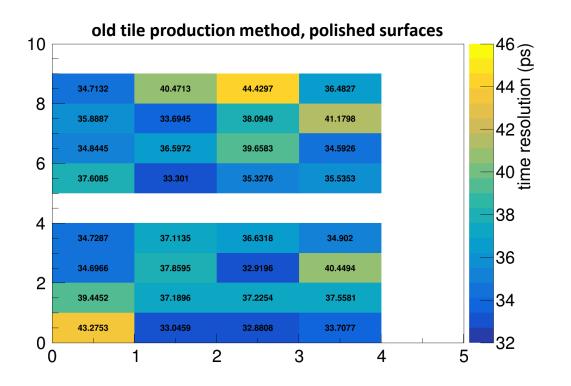
- coincidence time resolution (CTR):  $\sigma_{ii}^2 = \sigma_i^2 + \sigma_i^2$
- single channel resolution using three channels 1, 2, 3:  $\sigma_1 = \frac{1}{\sqrt{2}} \sqrt{\sigma_{12}^2 + \sigma_{13}^2 - \sigma_{23}^2}$
- single channel resolution using both matrices
  - 8 channels in one column
  - no cuts on energy spectra
  - using timewalk correction
  - ightarrow extract individual channel resolution

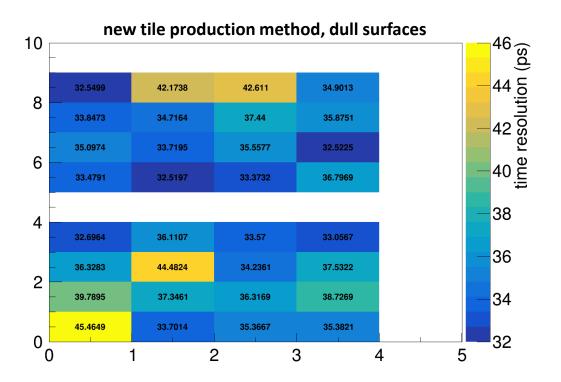




### Timing results

- single channel resolution of all four matrices
  - excellent uniformity of time resolution
  - some "outliers" due to MuTRiG channel variations
    - remember: same MuTRiG used for left and right plot

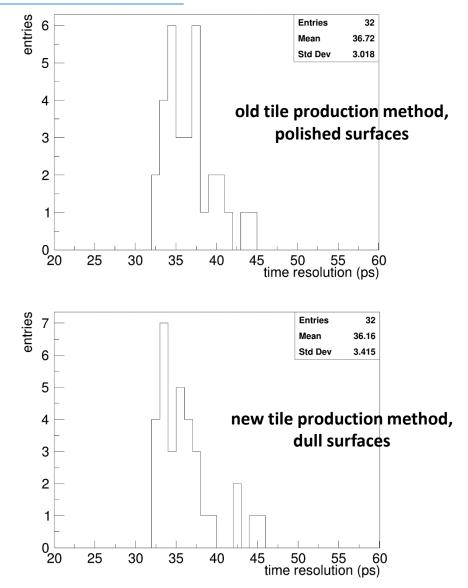




### Conclusions

- excellent uniformity of single channel resolution
  - within and between matrices
- excellent timing performance
  - average resolution (old method): (36.7 ± 3.0) ps
  - average resolution (new method): (36.2 ± 3.4) ps
- no difference in time resolution between old and new tile production methods

### $\rightarrow$ functionality and timing performance of new design validated



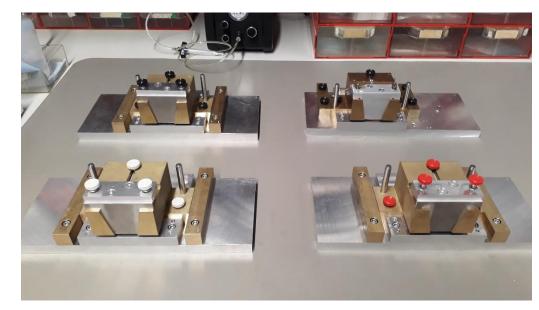
### Pre-production setup and plans

### Pre-production status

### **Pre-production has started!**

- reminder: goal are two modules for commissioning in spring 2021
  - we have all the material needed (> 1000 tiles, 1000 SiPMs, two cooling plates, ...)
- production & assembly:
  - first round of matrix PCBs assembled with SiPMs
  - wrapping tools: centre tiles ready, edge tiles needs some fine-tuning
  - gluing tools are ready
- Quality Assurance tests:
  - QA for matrix PCB is ready
    - general functionality of electronics
    - SiPM DCR
  - tile matrix QA is under development
    - SiPM gain
    - tile light yield

Tiancheng's work



### Outlook

- first round of assembly before Christmas
  - SiPM QA
  - tile wrapping & gluing
  - tile matrix QA

 $\rightarrow$  validate and optimise production & QA procedures

 $\rightarrow$  beginning for next year: start full module production

- still missing: read-out board with MuTRiGs
  - under development @ KIP electronics workshop

based on MALIBU design by Konrad Briggl

- aim at submission before Christmas
- ightarrow start board QA at end of Q1 2021
- commissioning of two modules @ DESY and PSI in spring 2021