



UNIVERSITÄT
HEIDELBERG
ZUKUNFT
SEIT 1386

ziti

Update on:
XIDer – an **X**-ray **I**ntegrating **D**etector
for the ESRF-EBS Upgrade

David Schimansky

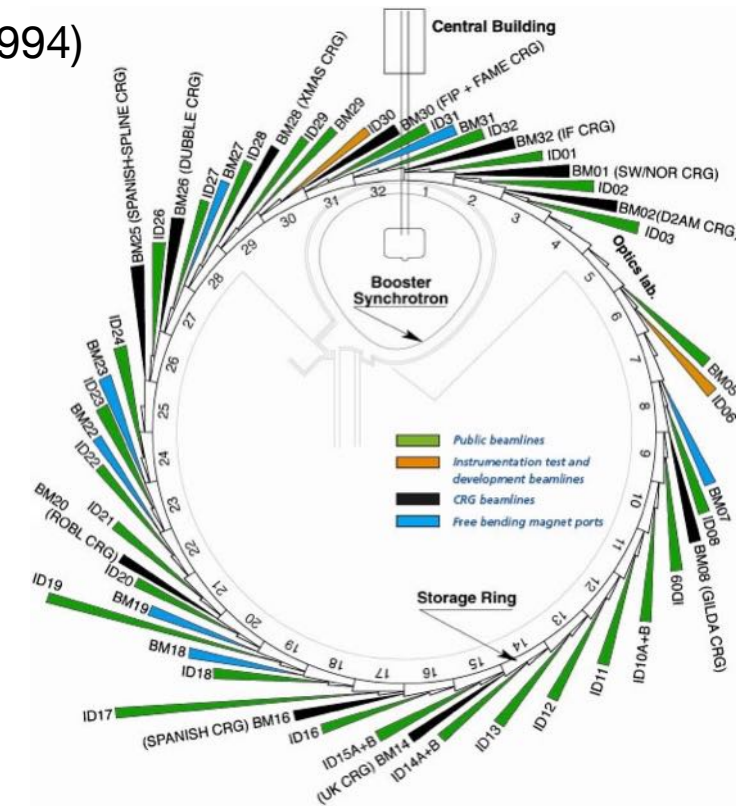
- The European Synchrotron Radiation Facility (ESRF) & its upgrade program (EBS)
- Introduction to XIDer
- Readout ASIC
 - Design
 - Characterisation Example: Frontend noise & linearity
- Sensor/ASIC assembly prototypes
- Conclusion & Outlook



European Synchrotron Radiation Facility (ESRF)



- Joint research facility in Grenoble, France (founded in 1988)
- Funded by 22 countries (France, Germany, Italy, ..)
- Electron synchrotron x-ray source (up to ~150keV)
- First 3rd generation synchrotron (opened in 1994)
- Circumference: 844m
- 2000 publications per year
- Advertises itself as „user facility“
- Available research methods
 - X-ray spectroscopy
 - X-ray tomography
 - X-ray diffraction





EBS electromagnets

Extremely-Brilliant Source (ESRF-EBS):

- Storage ring & instrumentation upgrade program over the period 2015-2022
- New storage ring has been finished and opened in 2020 as planned
- Improved energy efficiency (30% cost reduction)
- Increased brilliance of x-ray beam
- Needs new detectors tailored to the upgraded source
 - ⇒ Reach out to external laboratories



EBS electromagnets

Extremely-Brilliant Source (ESRF-EBS):

- Storage ring & instrumentation upgrade program over the period 2015-2022
- New storage ring has been finished and opened in 2020 as planned
- Improved energy efficiency (30% cost reduction)
- Increased brilliance of x-ray beam
- Needs new detectors tailored to the upgraded source

⇒ Reach out to external laboratories



XIDer: X-ray Integrating Detector



XIDer:

- R&D project until end of 2022
- 4-year funding: Shared 50/50 by ESRF and Heidelberg University
- HighRR members working on this project: Marin Collonge (ESRF), Christian Kreidl (HD), Michael Ritzert (HD), David Schimansky (HD)

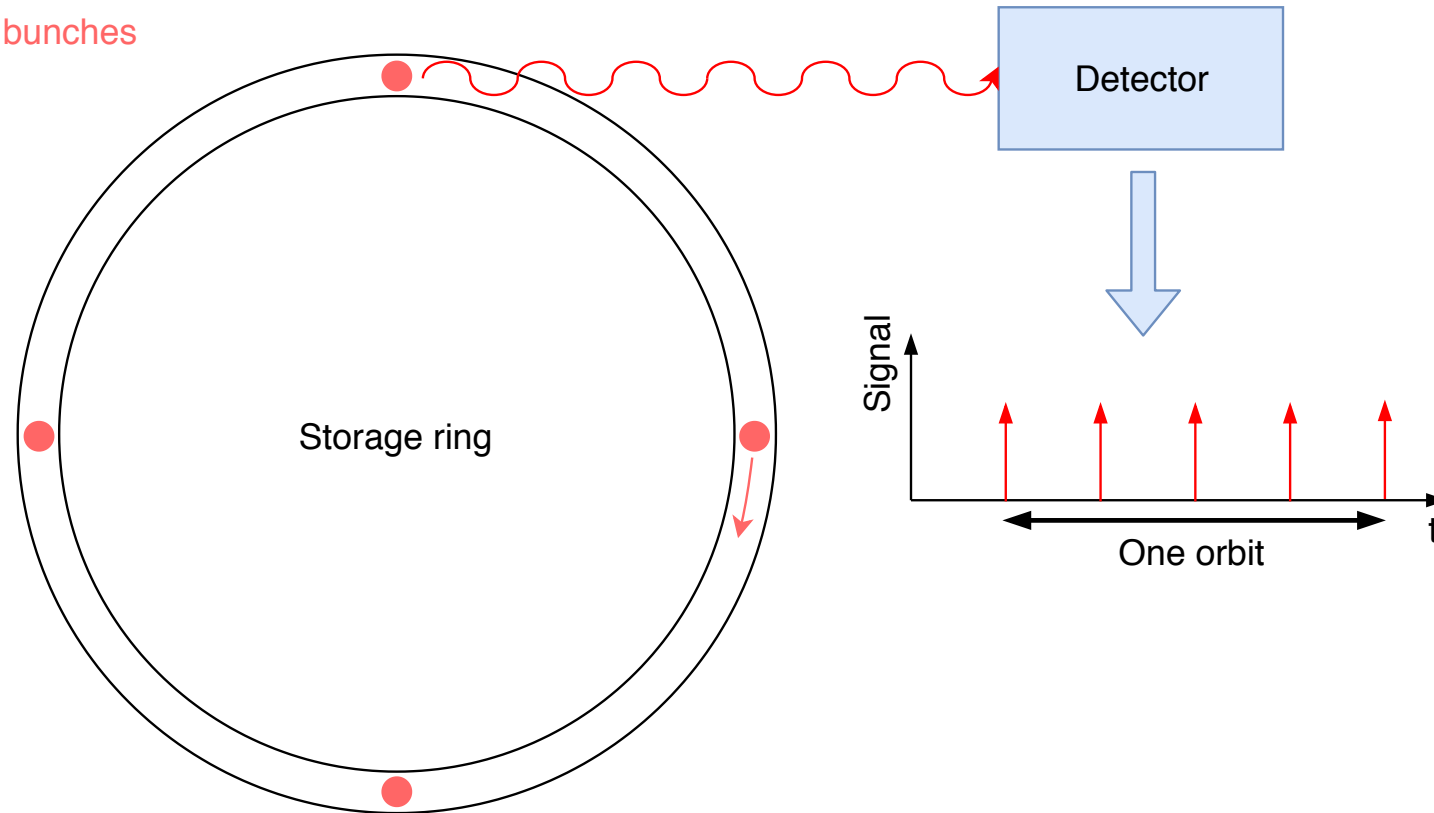
Build detector for any kind of (time-resolved) x-ray diffraction experiment at the ESRF:

- Energy range: 30-100keV
- Different spatial resolutions: 100 μ m vs. 200 μ m pixel pitch
- Dynamic range: Single Photons up to $> 10^{11} \frac{ph}{mm^2s}$
- Cope with different bunch filling modes for storage ring
- Time-resolved $>100k$ frames/s
- Flexible readout schemes single frame, accumulated frames, ..

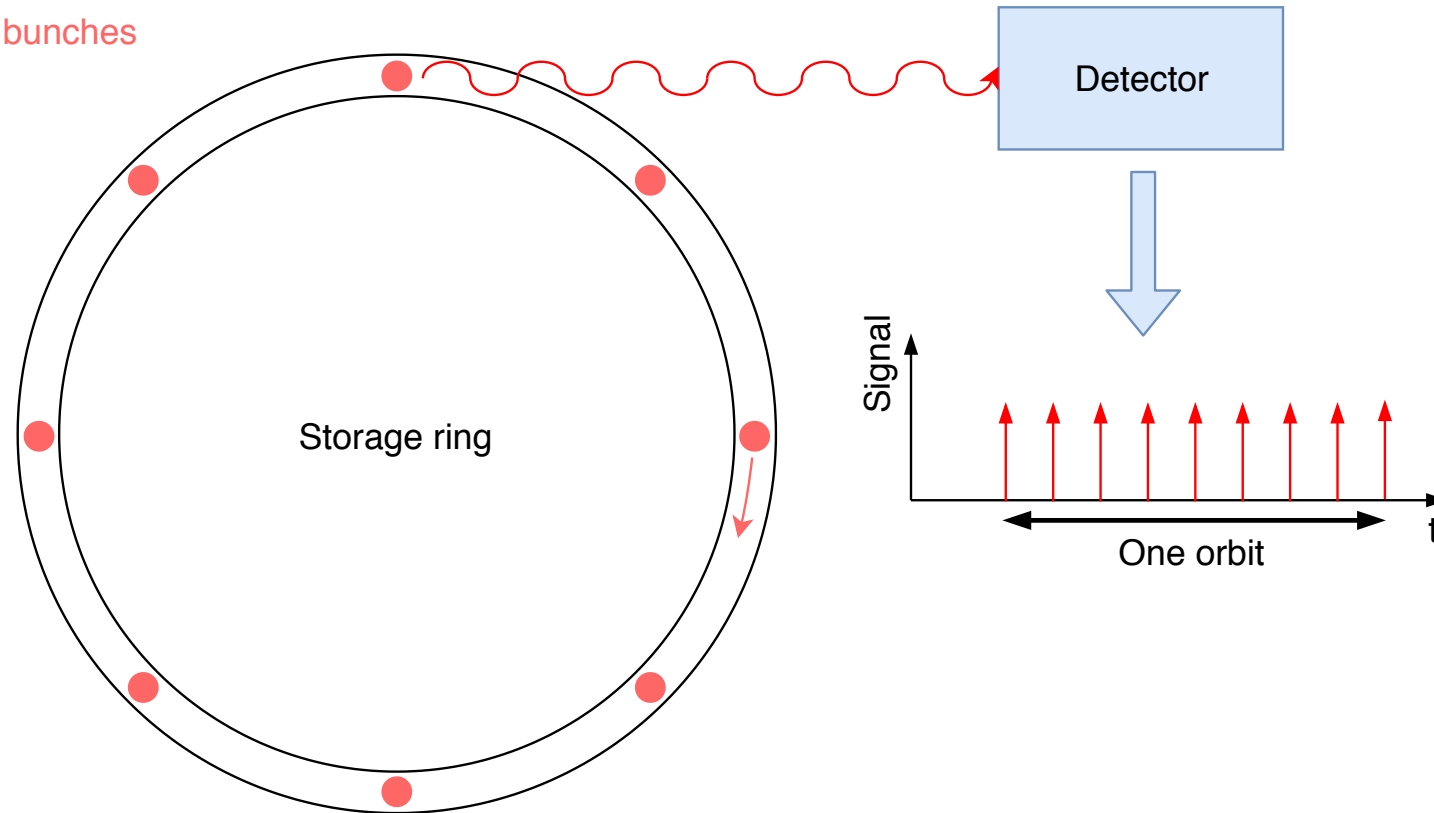
Build detector for any kind of (time-resolved) x-ray diffraction experiment at the ESRF:

- Energy range: 30-100keV
- Different spatial resolutions: 100 μ m vs. 200 μ m pixel pitch
- Dynamic range: Single Photons up to $> 10^{11} \frac{ph}{mm^2s}$
- Cope with different bunch filling modes for storage ring
- Time-resolved $>100k$ frames/s
- Flexible readout schemes single frame, accumulated frames, ..

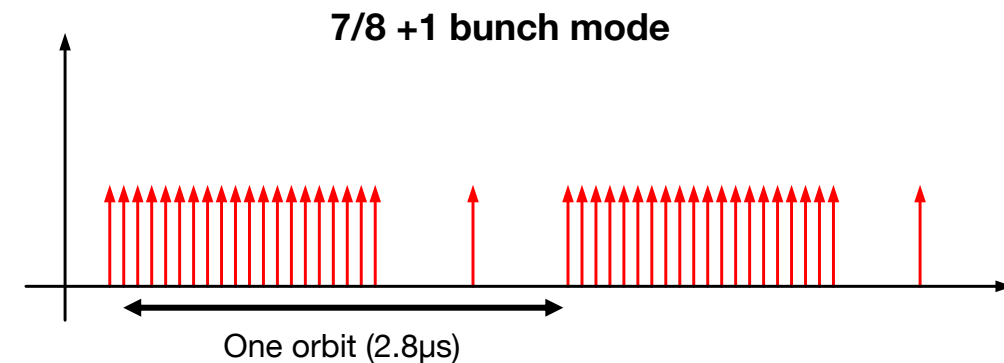
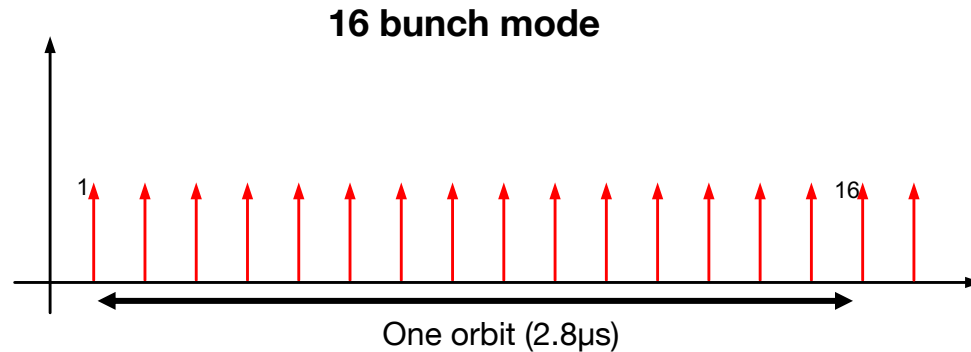
● Electron bunches



● Electron bunches



Example cases of possible bunch modes



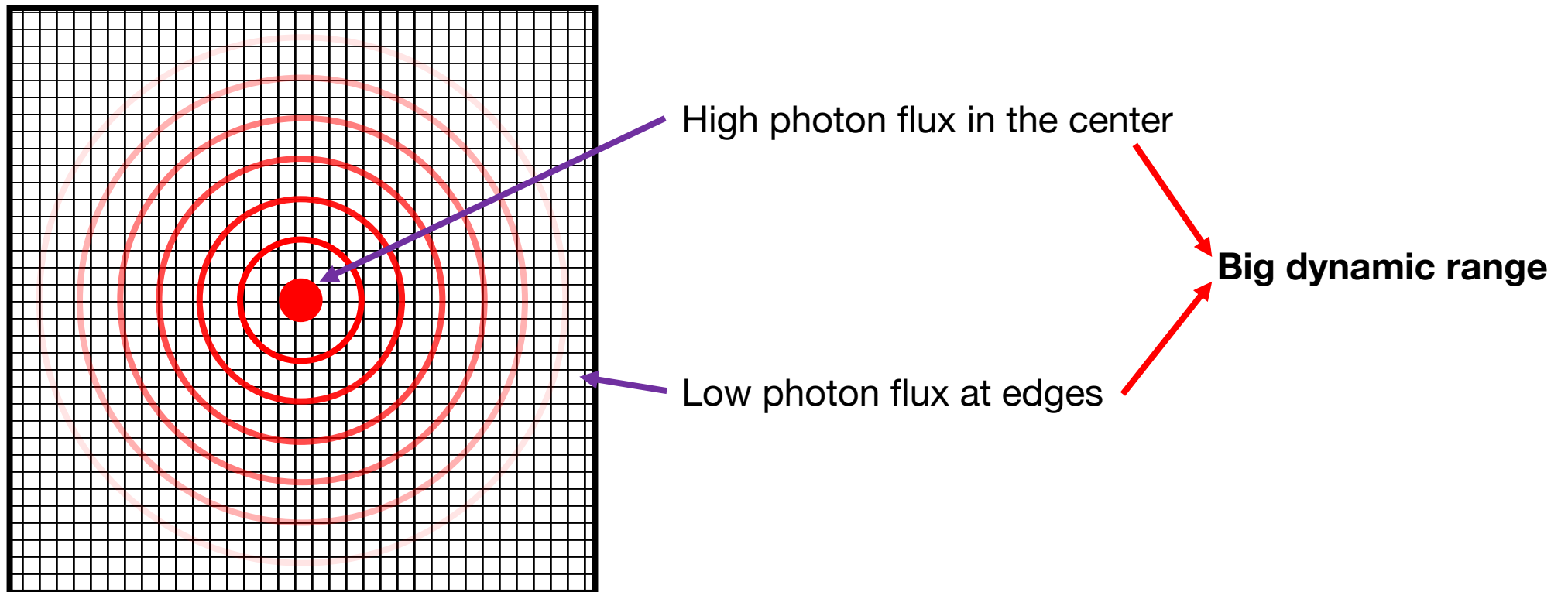
- Pulsed illumination for time-resolved experiments
- Single bunches have to be recorded and processed
- Need **single photon sensitivity**

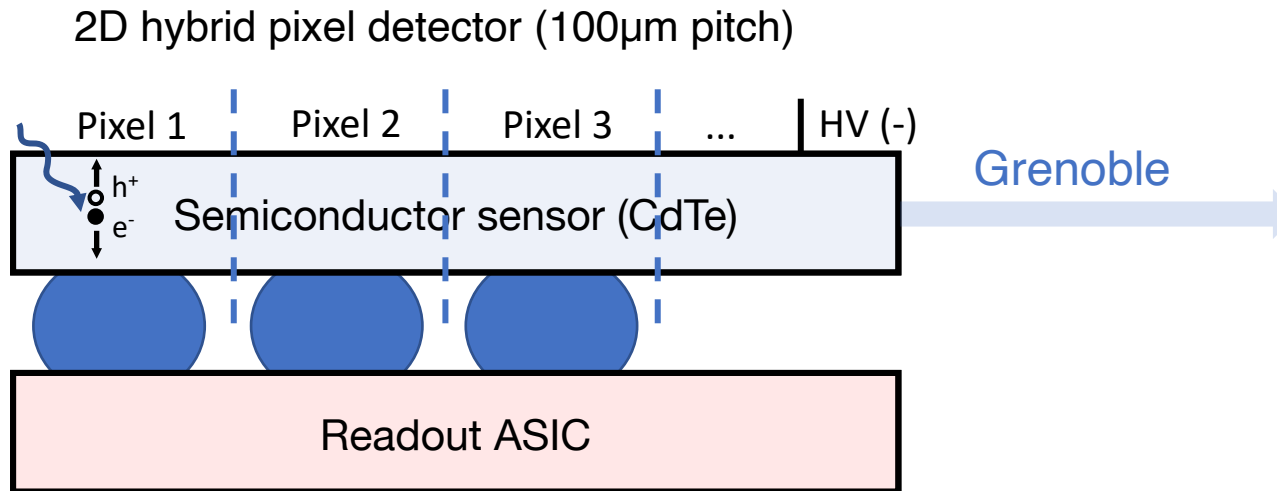
- Quasi-continuous illumination for 7/8 of the orbital period
- Integrate many bunches into one image
- Expected $> 10^{11} \frac{ph}{mm^2s}$

Big dynamic range

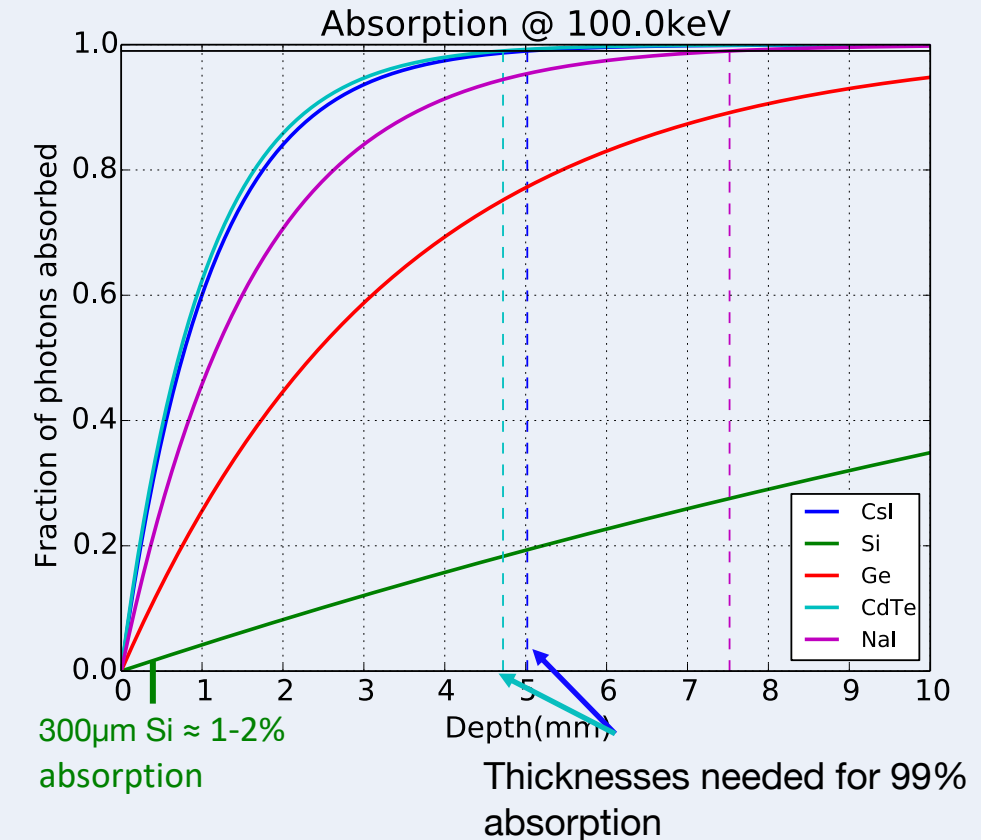
- Requirement of big dynamic range is not only given by different bunch modes
- Even in high flux experiments, single photon sensitivity is still important:

Example: Airy disk of circular aperture hits the pixelated detector





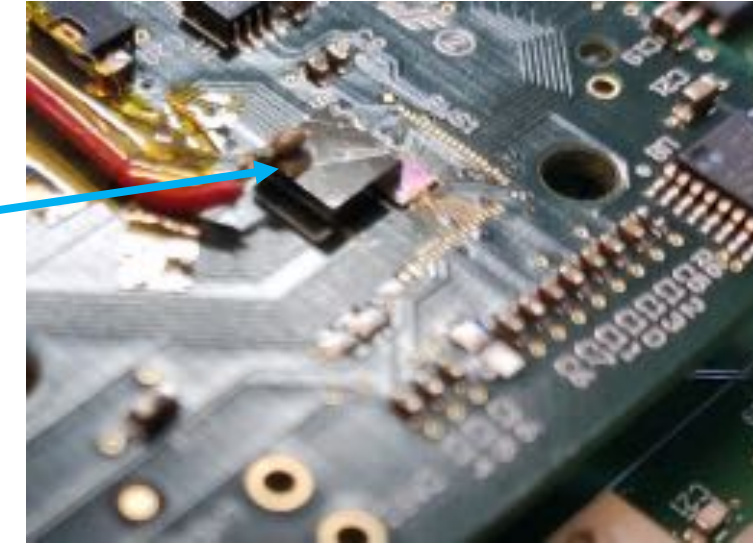
- Every pixel is connected to its own frontend in the readout ASIC
- **Charge integrating** frontend with **continuous analog-to-digital conversion** for high dynamic range

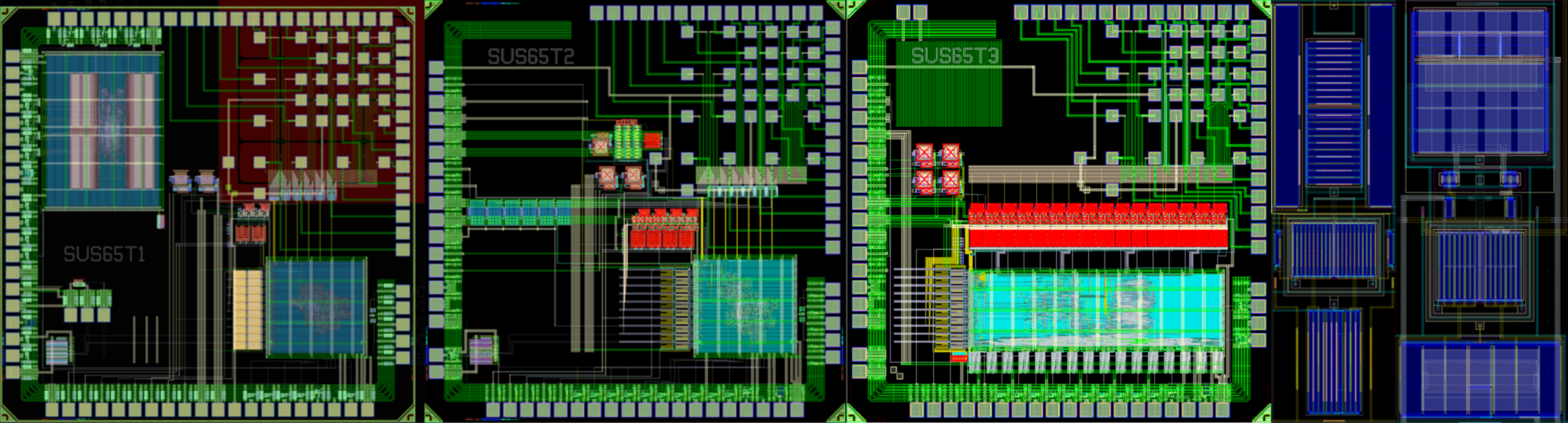


- Use **high-Z material** to get high stopping power
- Tendency: Cadmium Telluride (CdTe)

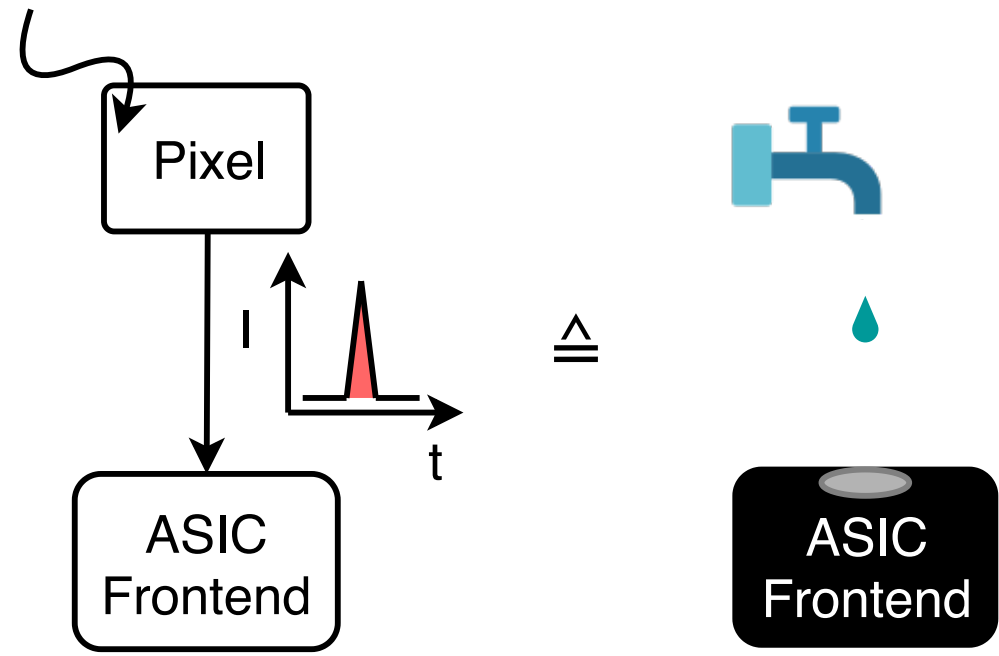
- Expensive and only a few suppliers around the world
- Heat sensitive: Introduction of defects $>80^{\circ}\text{C}$
- Brittle
- Low tensile strength
- Afterglow: Generated charge signals have very long tails (see sensor measurements)
- Polarisation:
 - High photon fluxes generate space charges due to trapping of holes (low mobility-lifetime product of holes)
 - Space charges then generate electric field that counteracts field of bias HV
 - Space charge field can get so strong that HV field is cancelled completely
 - ⇒ Detector becomes “blind” to incoming photons
 - ⇒ Addition of Zinc (Cadmium-Zinc-Telluride, CZT) in right amounts can solve this problem by increasing the hole mobility-lifetime product
 - ⇒ BUT: CZT is almost impossible to buy. We keep trying, though.

Crack in CdTe sensor
prototype after shipping
it from HD to the ESRF



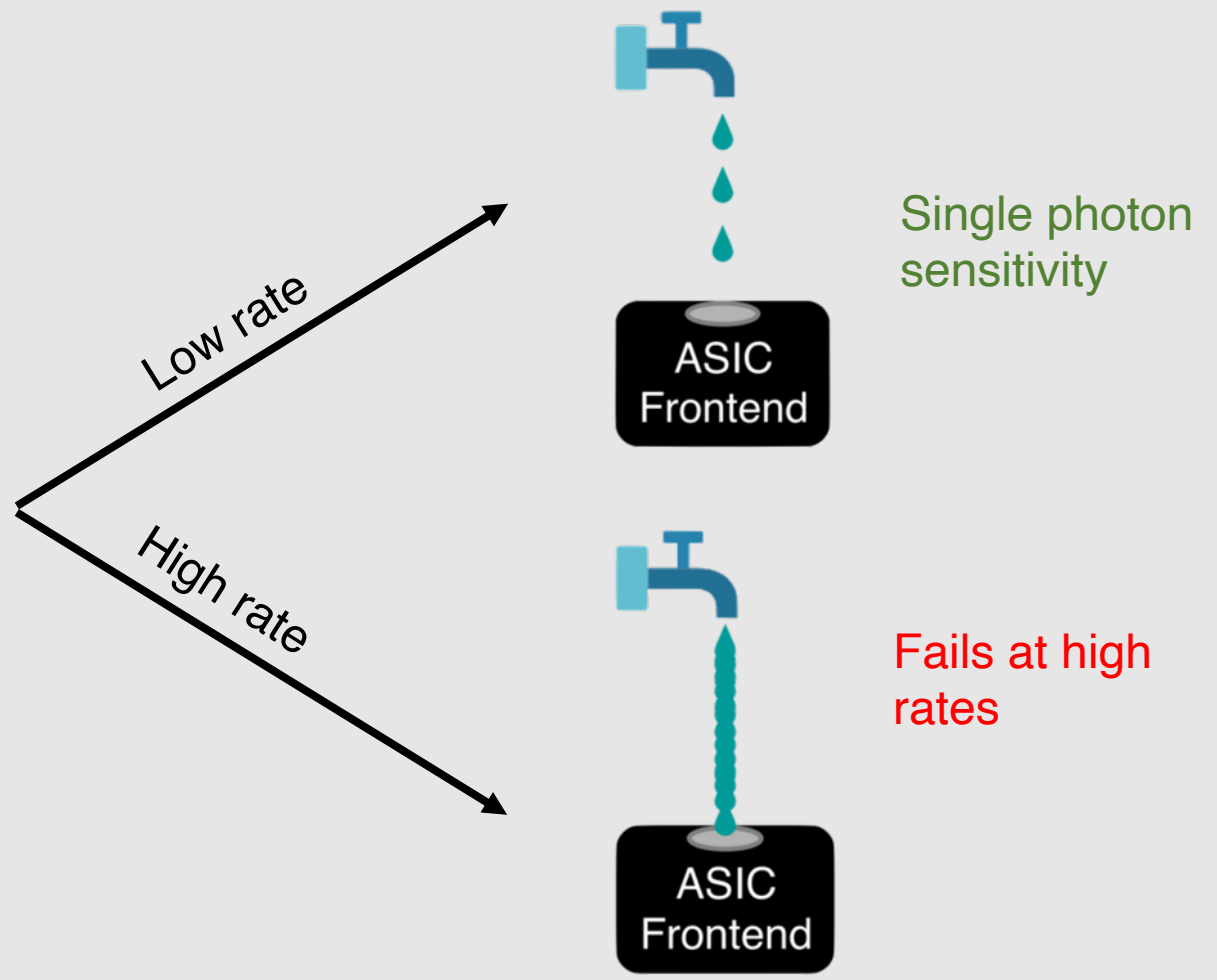


Readout ASIC

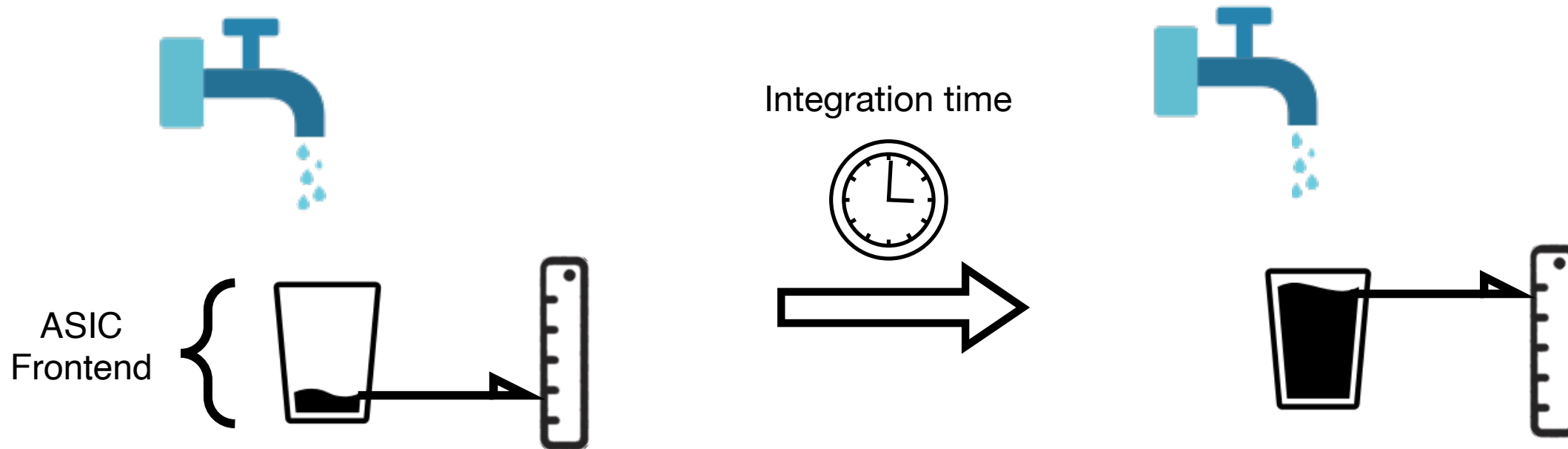


Analogy: Photons are water drops

Most basic idea: Count drops

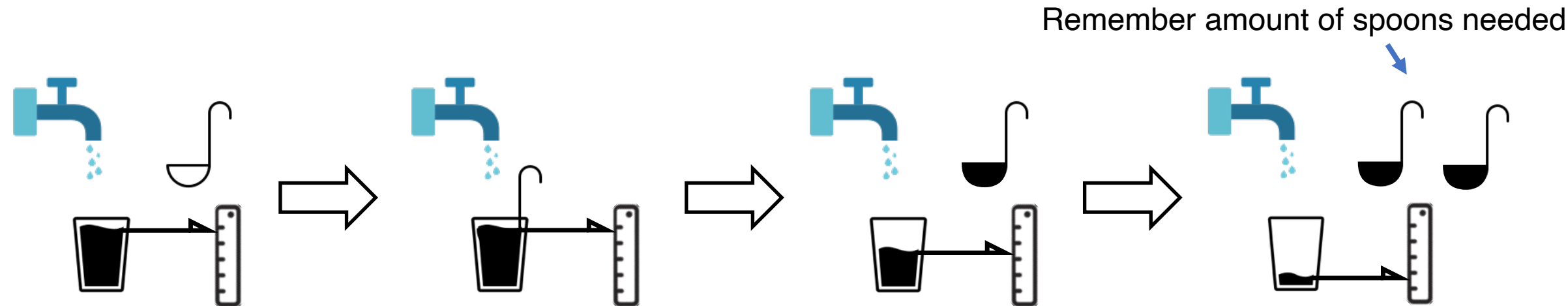


Conceptually different: Collect drops in a bucket and measure water level

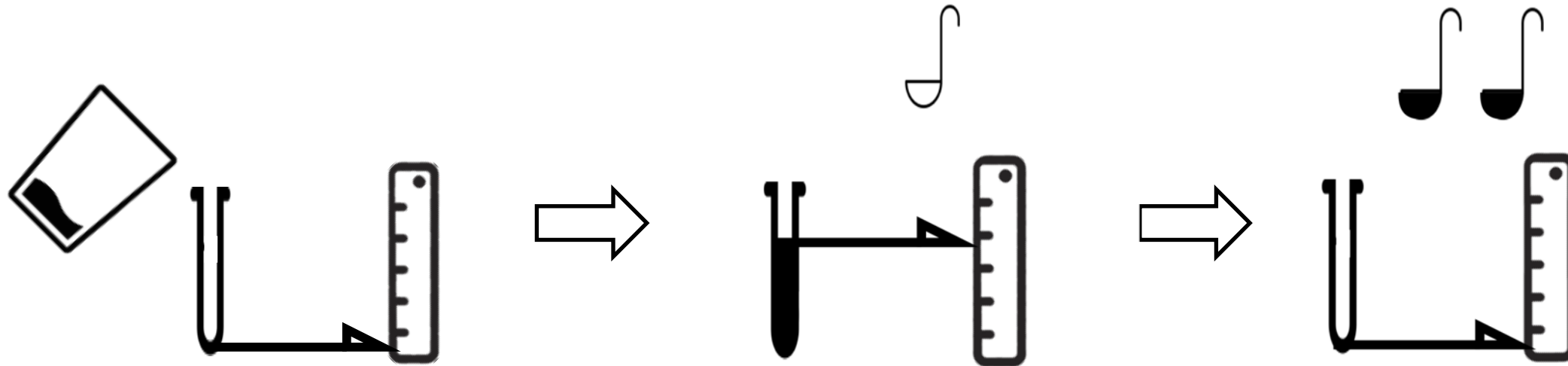


Dynamic range is limited by bucket size

Add-on to charge integration: Prevent bucket from overflowing by emptying it with spoons



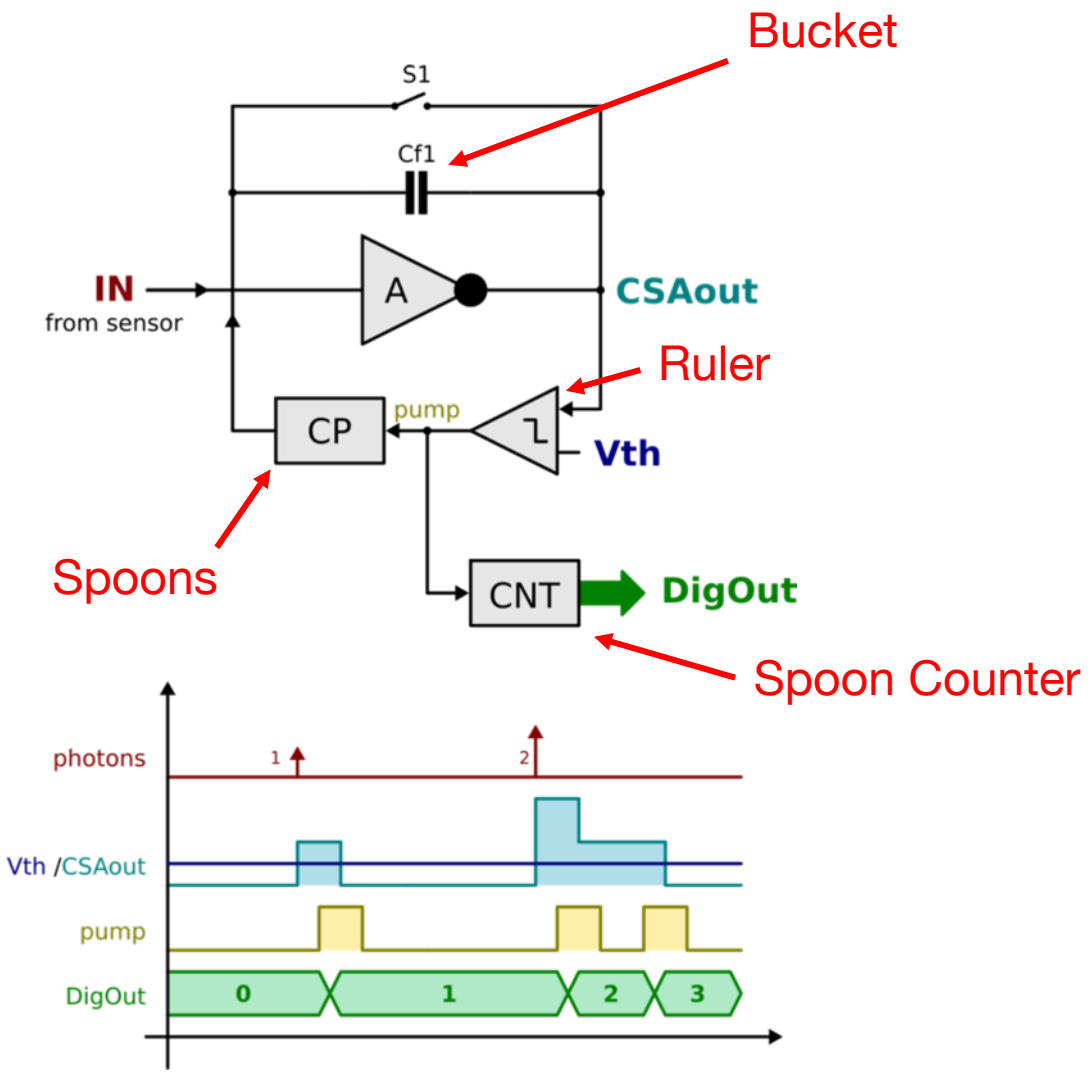
Single photon sensitivity & can handle high rates & dynamic range is not limited by bucket size



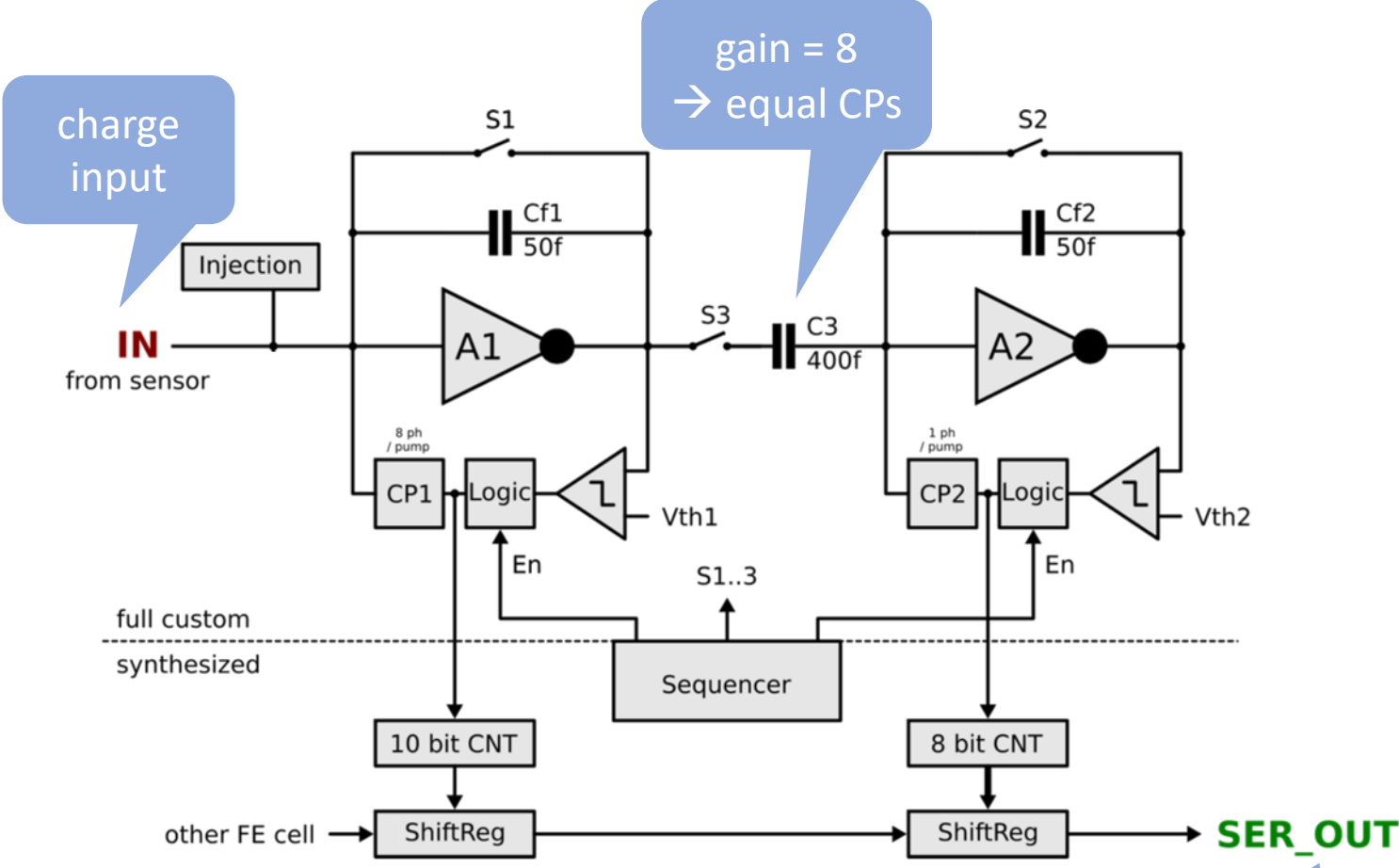
⇒ A second, smaller bucket with a smaller spoon allows for even bigger dynamic range, e.g.:

- Small spoon has size of single photon ⇒ Single photon sensitivity
- Big spoon has size of several photons ⇒ Higher rates

Continuous Conversion with Single Bucket



Continuous Conversion with Two Buckets



gain = 8
→ equal CPs

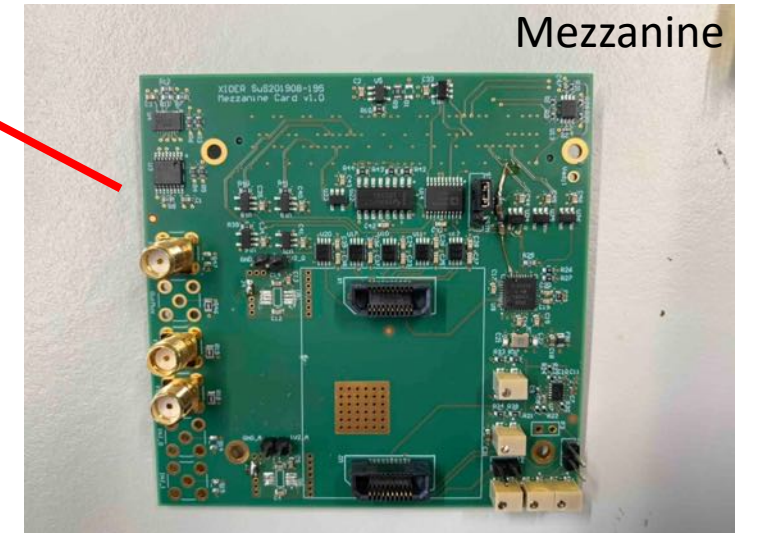
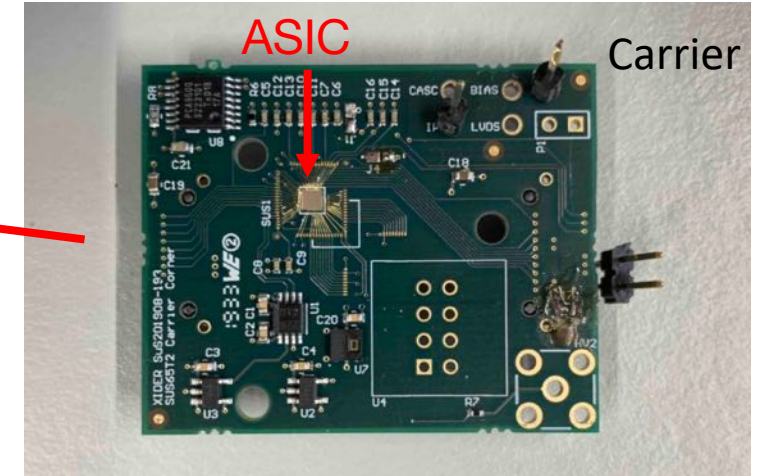
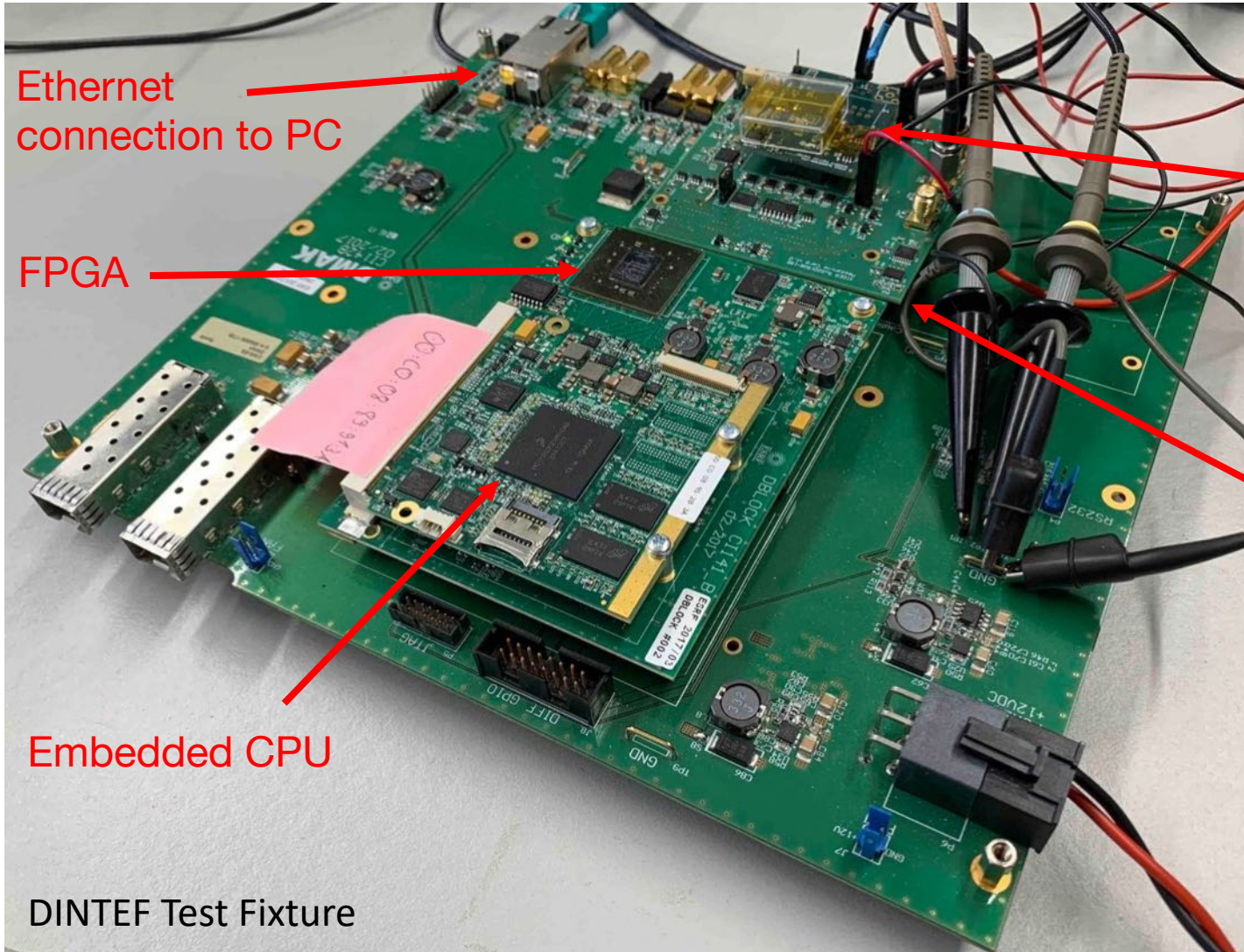
charge input

serial digital output

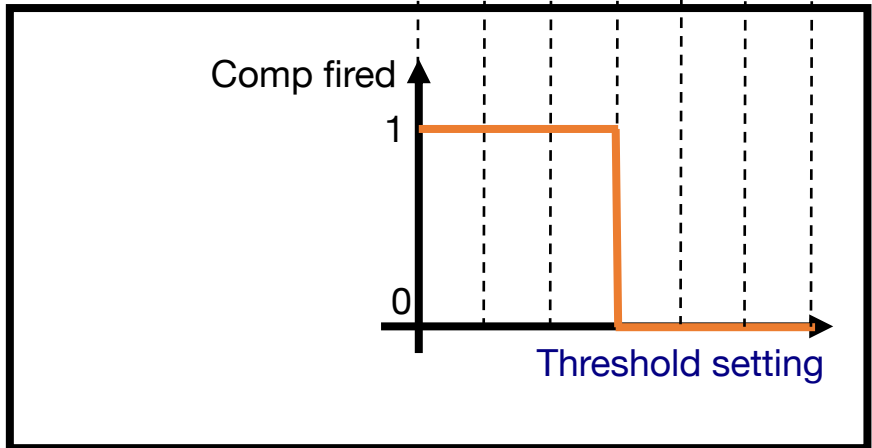
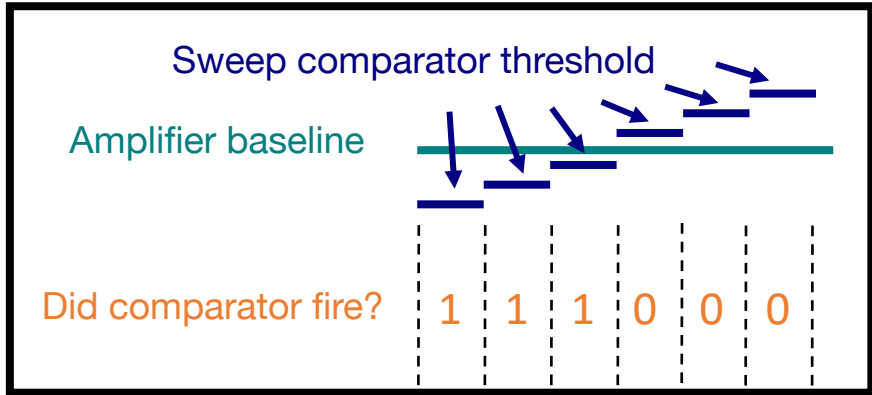
• Design choices and challenges:

- Spoon size
- Spoon rate
- Spoon ratio between stages
- Bucket sizes
- Charge pump (CP) topology
- CP matching
- Clean stage transition
- Power limitation
- Space limitation ((100µm)² pixels)

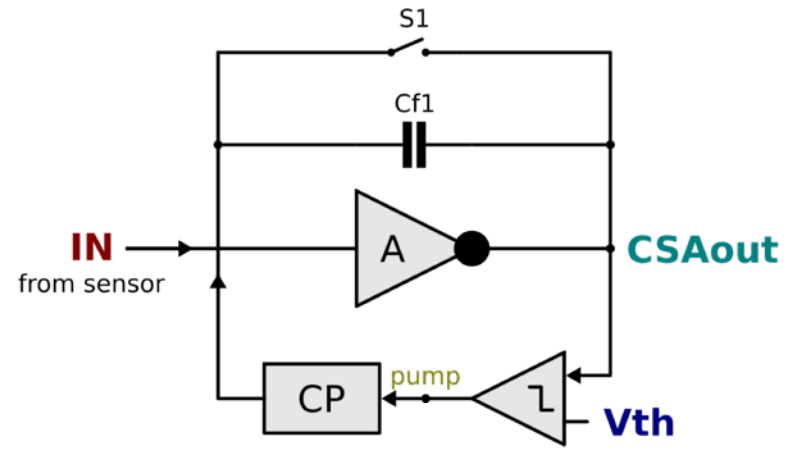
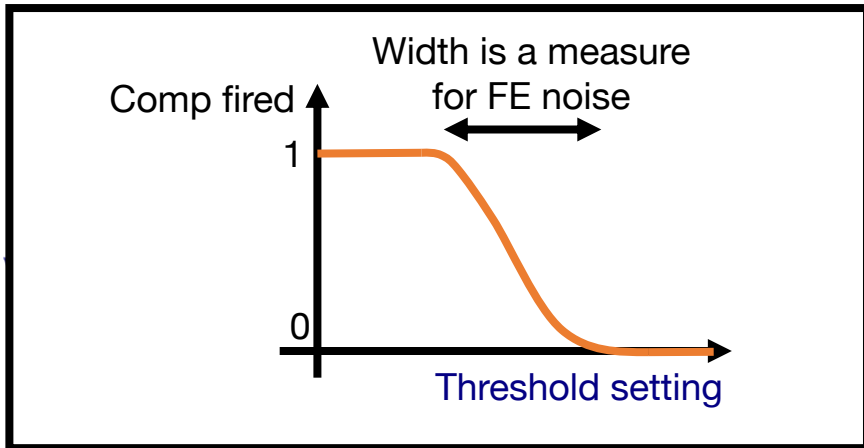
- 1st stage pumps 8 ph per spoon
- 2nd stage pumps 1 ph per spoon
- $f_{pump} \sim 100 \text{ MHz}$ (for now)
- 1st stage: $8 \cdot 10^8 \frac{ph}{pixel \cdot s}$



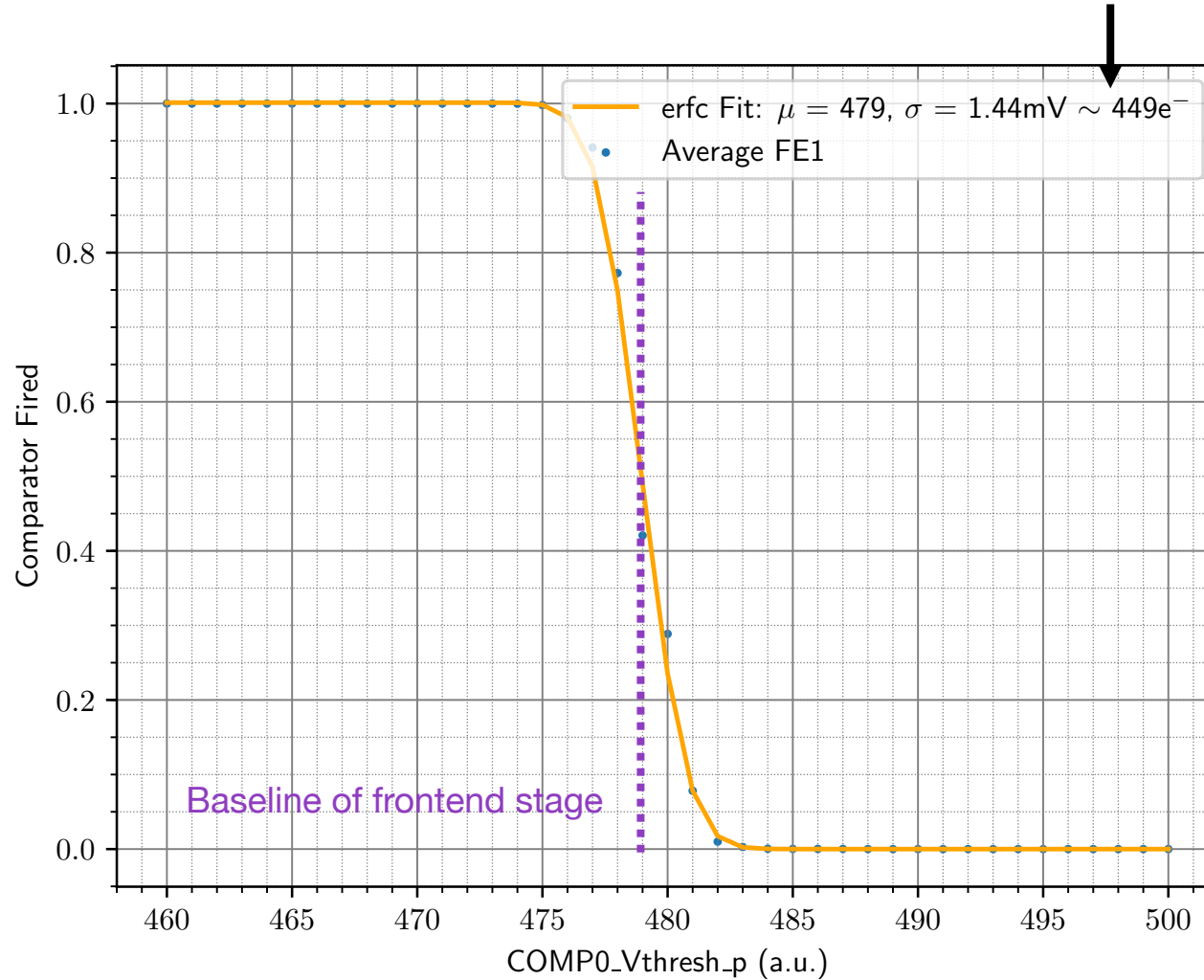
Frontend Noise Measurement



With noise
& statistics

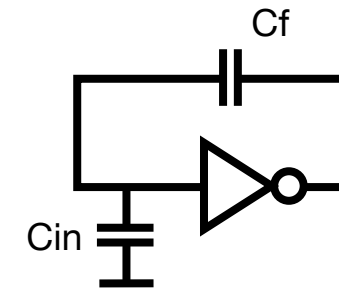
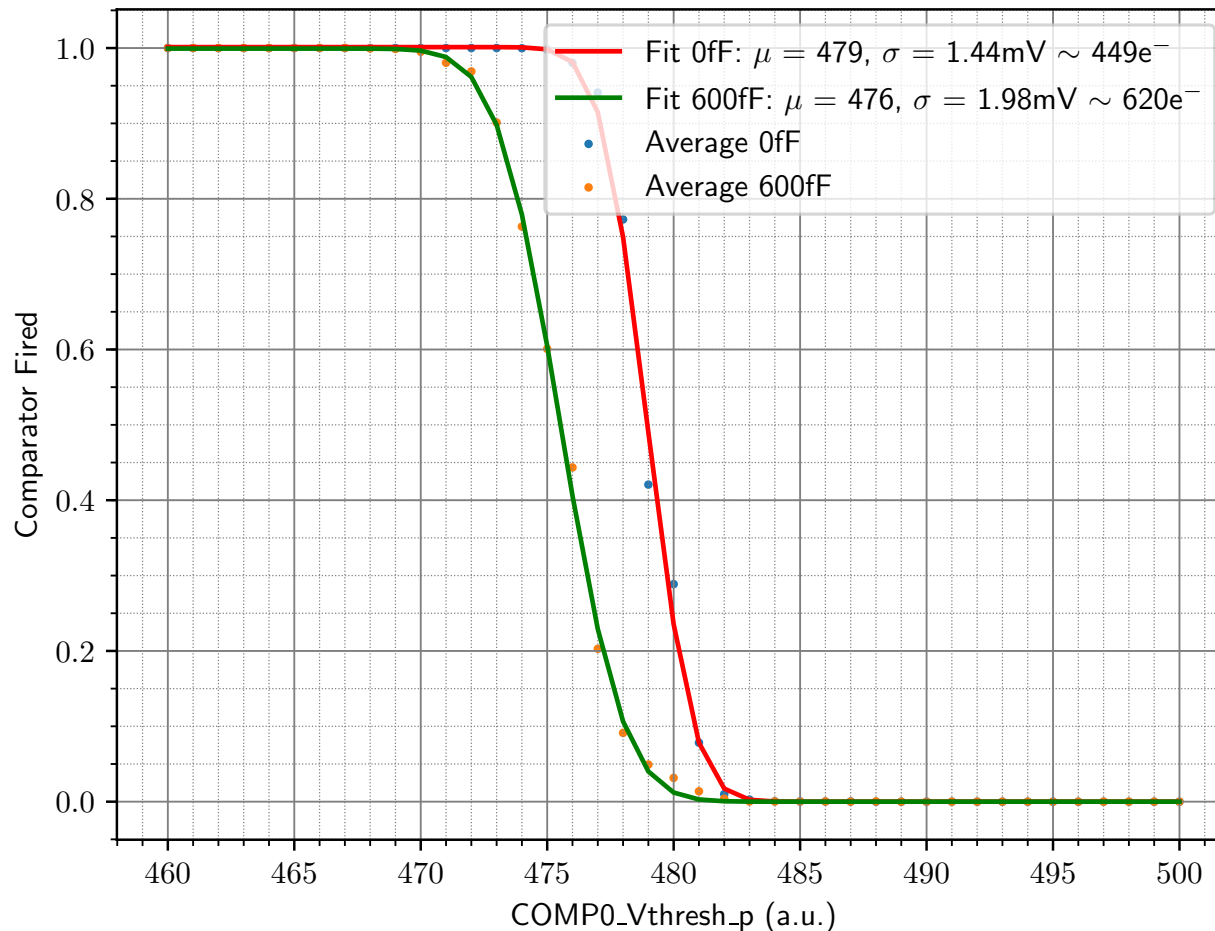


For this chip iteration, we want to be below 600e- (input referred noise)



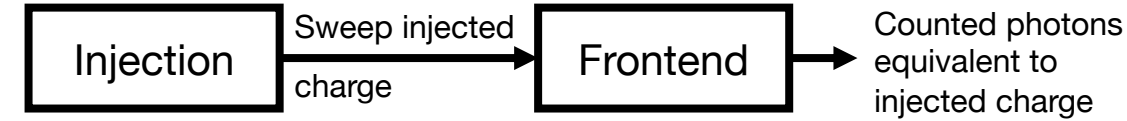
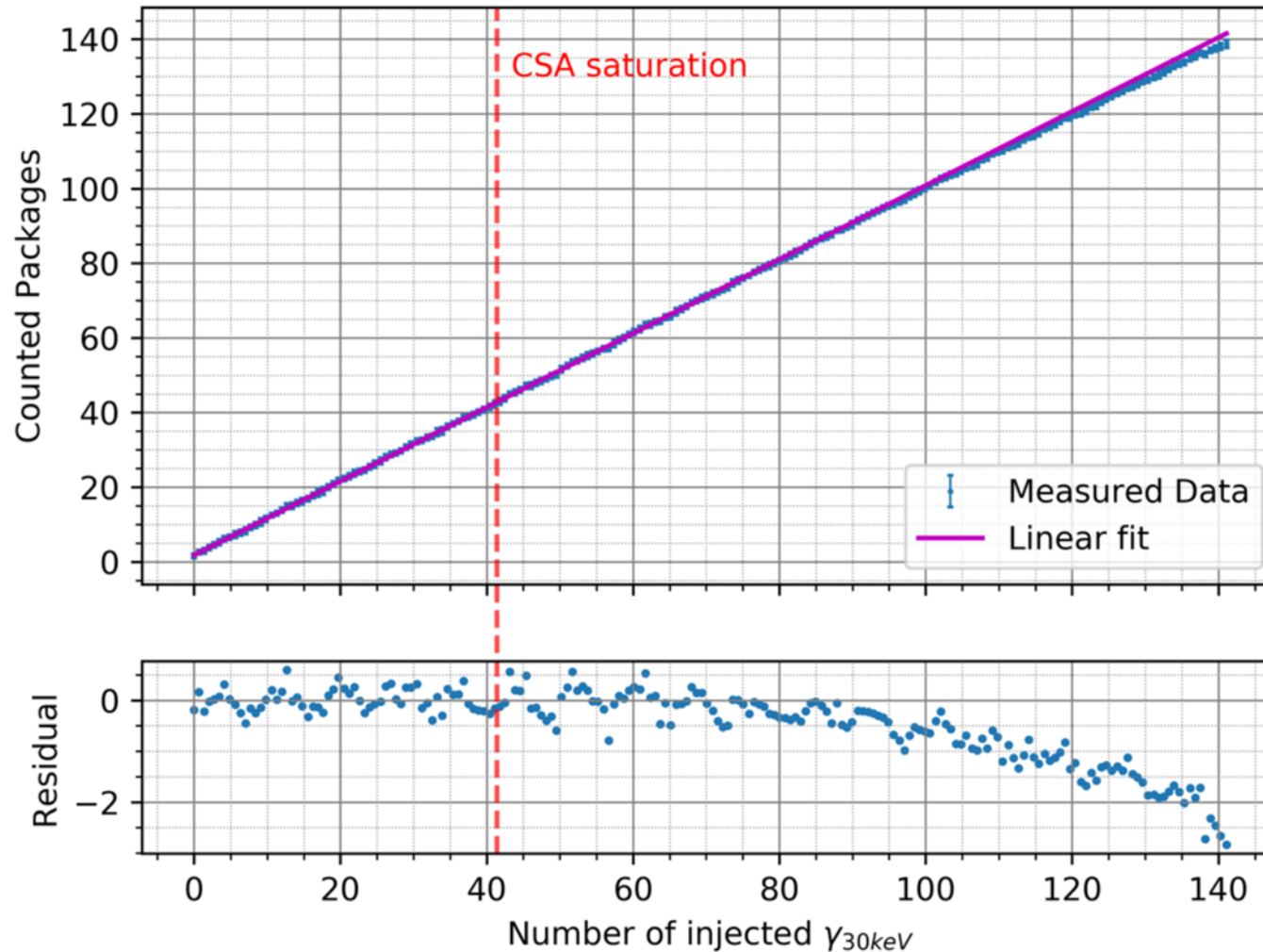
- Blue data points: Average of 4000 measurements for same comparator threshold
- Orange curve: Error function fit

- Different input capacitances (good sanity check)



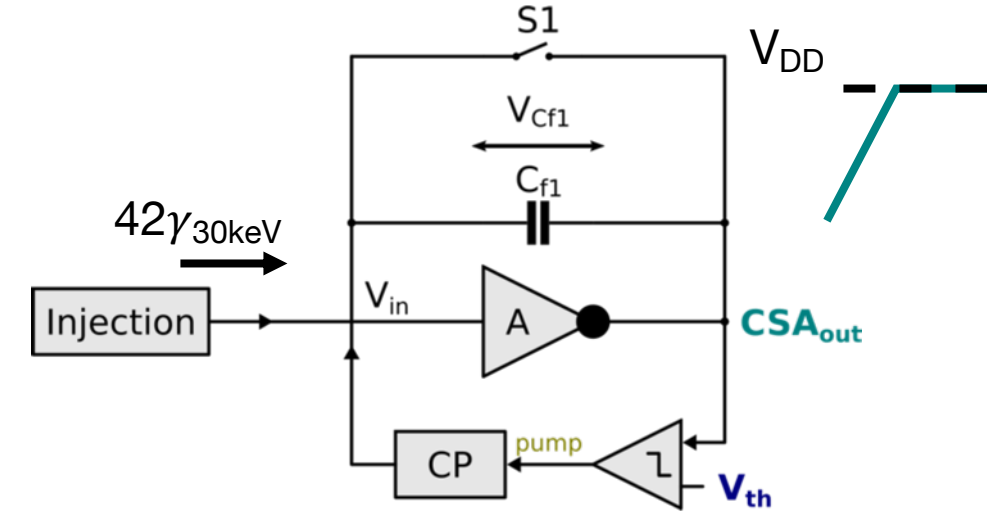
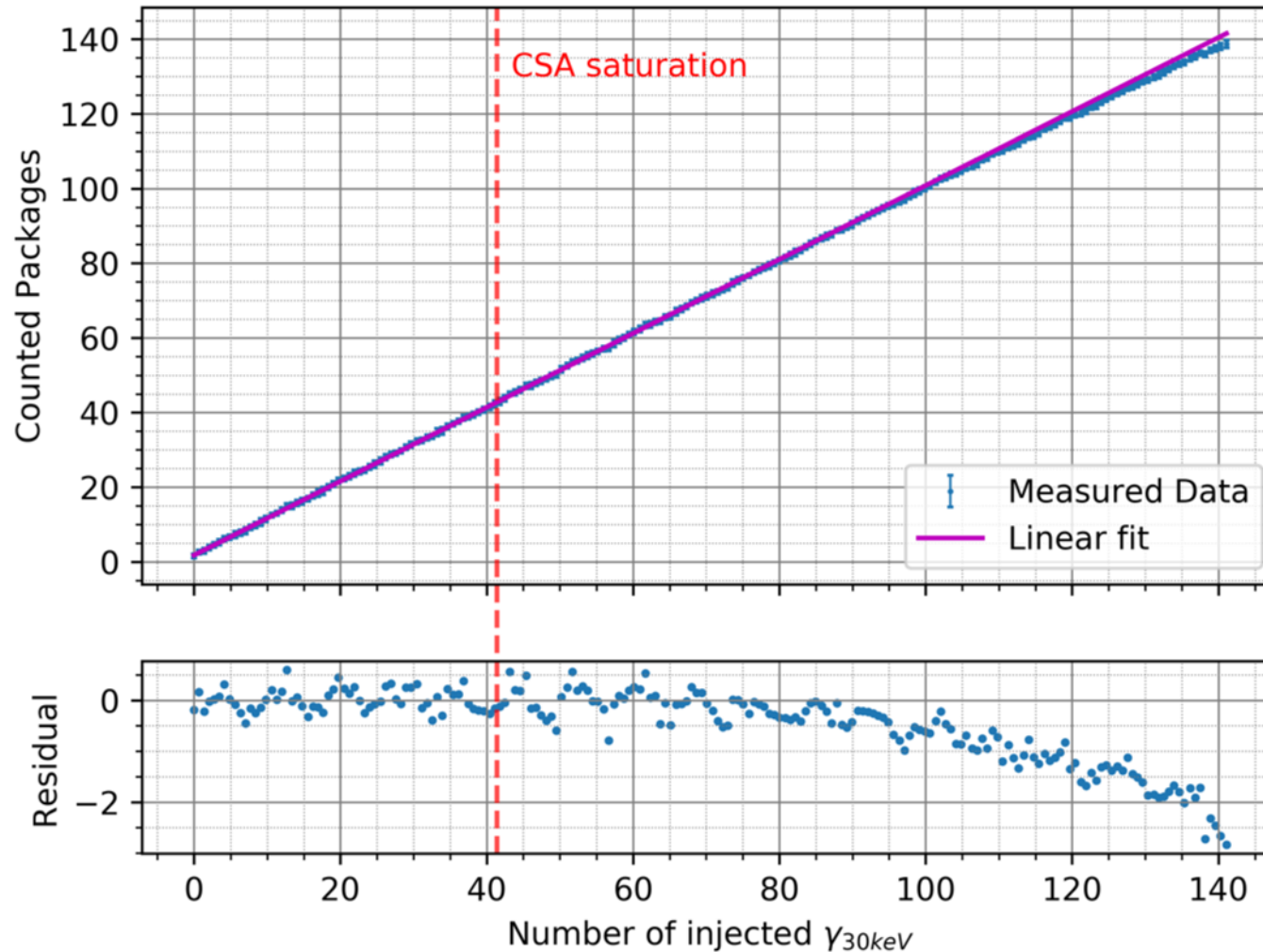
- Fits to simulation almost perfectly
- As expected: Noise rises by factor of ~ 1.4 (1.5 in sim) from 0fF to 600fF input capacitance

Measured linearity of T2



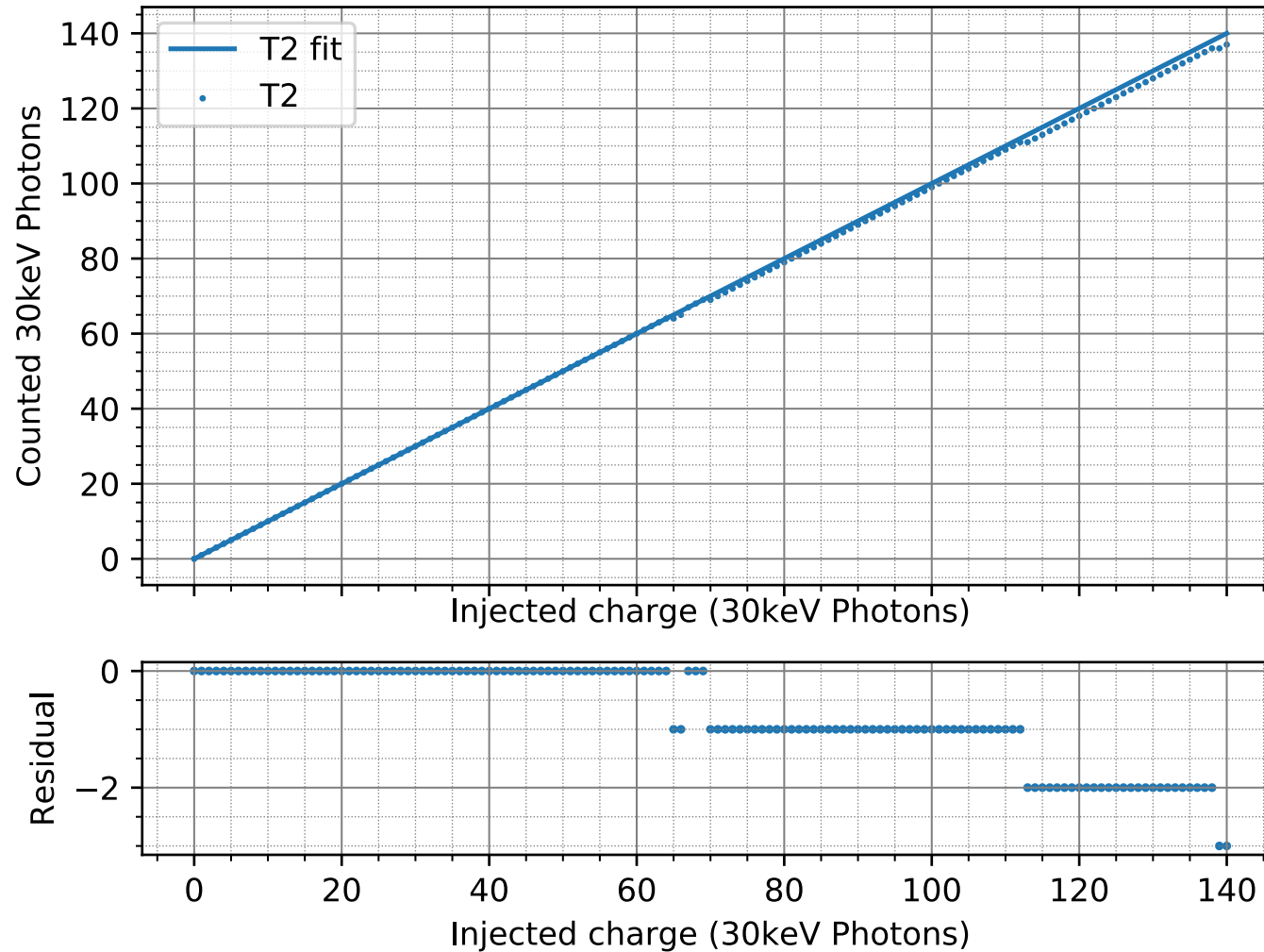
- Linear fit performed for injections $< 42 \gamma_{30keV}$ (explanation on next slides)
- Up to a point of $80 \gamma_{30keV}$, FE shows linear behaviour, maximum deviation of less than 1 count
- Above $80 \gamma_{30keV}$ the curve bends
- At $140 \gamma_{30keV}$ the maximum deviation is roughly 3 ADUs

Measured linearity of T2



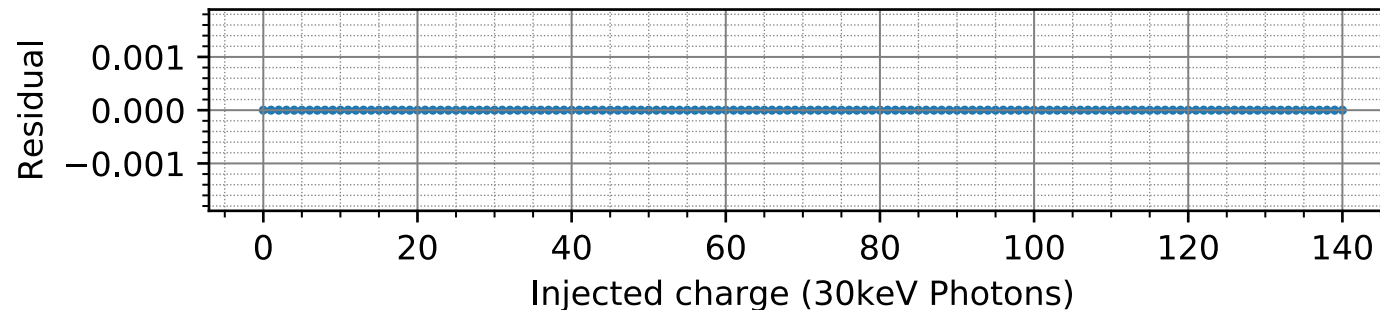
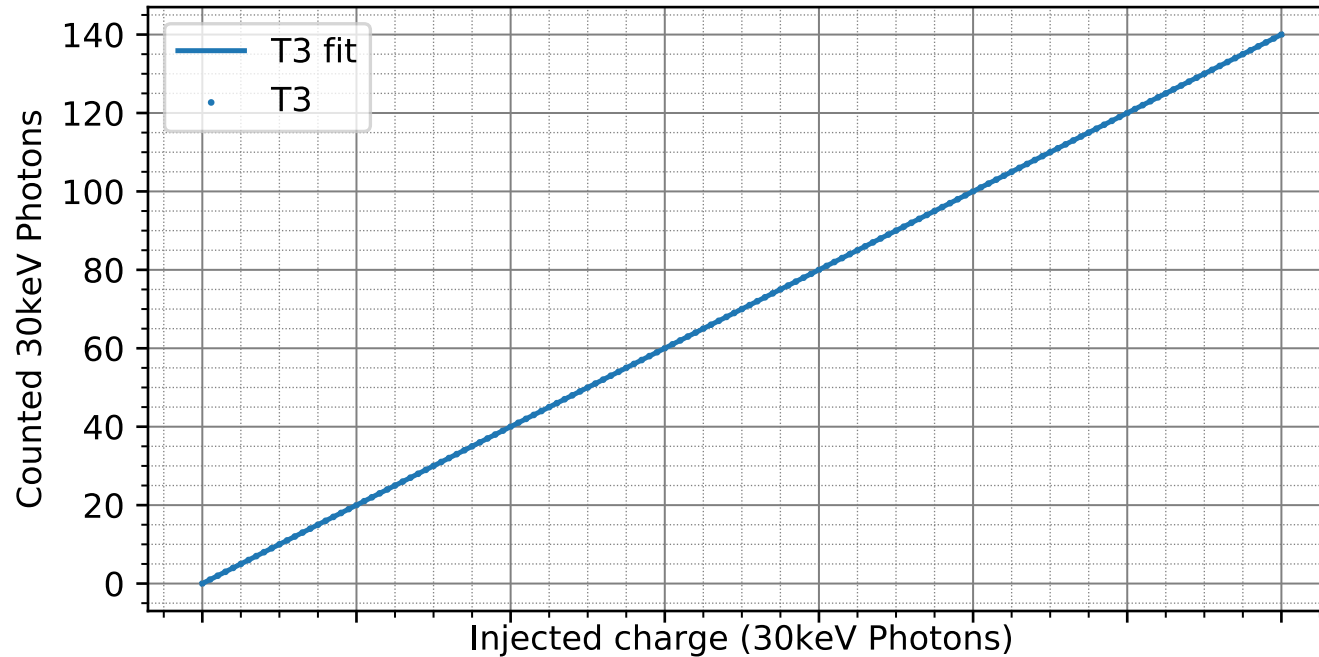
- At ~ 42 injected $\gamma_{30\text{keV}}$ the output voltage of the first stage is at the supply voltage (saturation)
- In first order: Frontend is robust against CSA saturation because additional charge is still stored on C_{f1} (it can't go anywhere else)
- If we go too far: Nonlinearities in charge pump cause error in measurement
- **Important:** Most of the experiments will be below $42 \gamma_{30\text{keV}}$ at the same time

Simulated linearity of T2

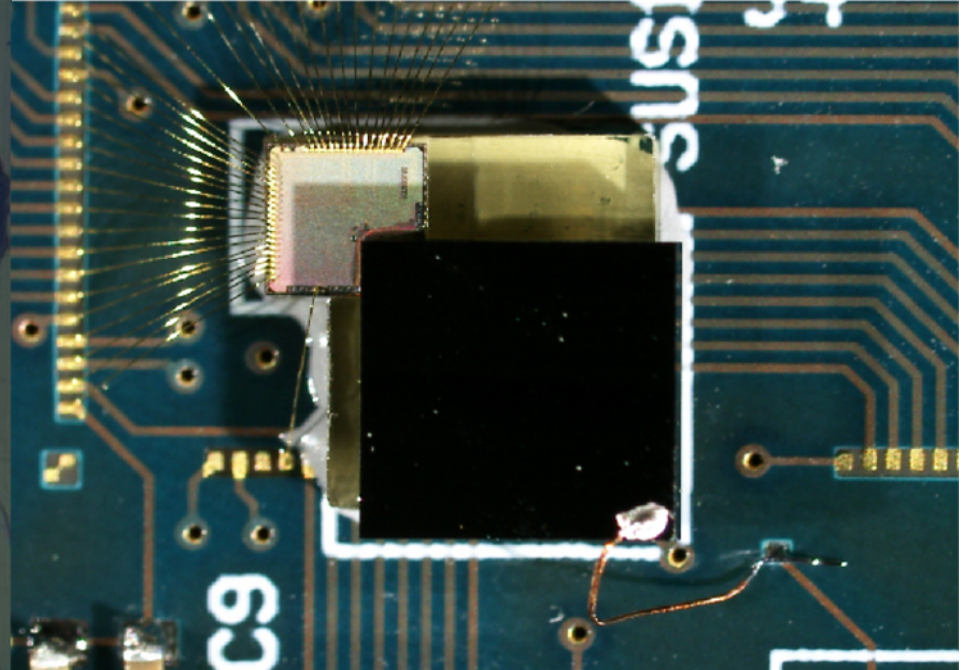
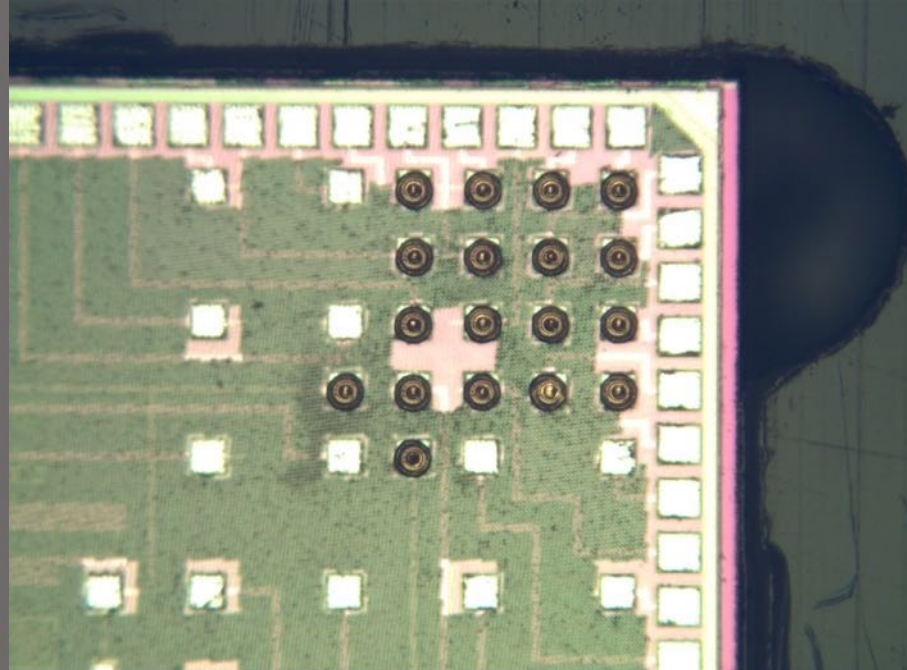
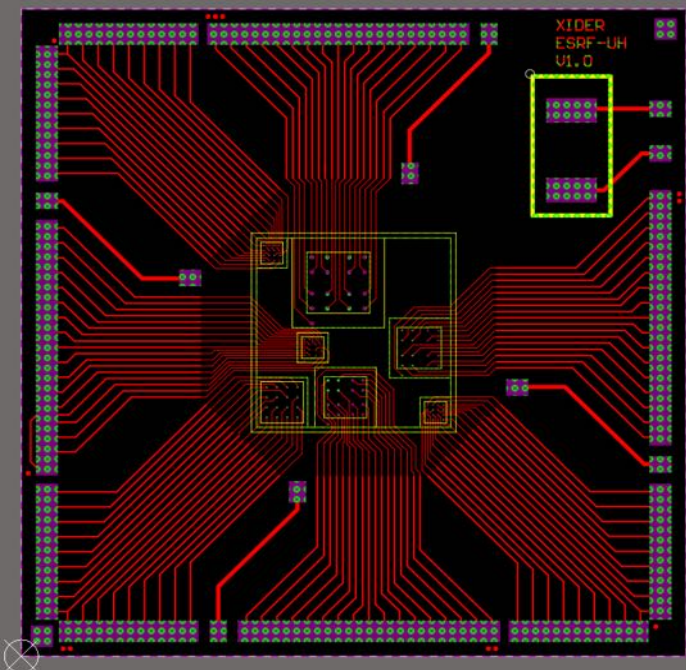


- Simulation shows similar behaviour:
 - Below $70\gamma_{30\text{keV}}$ the frontend is linear
 - For 140 injected $\gamma_{30\text{keV}}$ the deviation is 3 ADU
- Side note: This is without noise!

Simulated linearity of T3



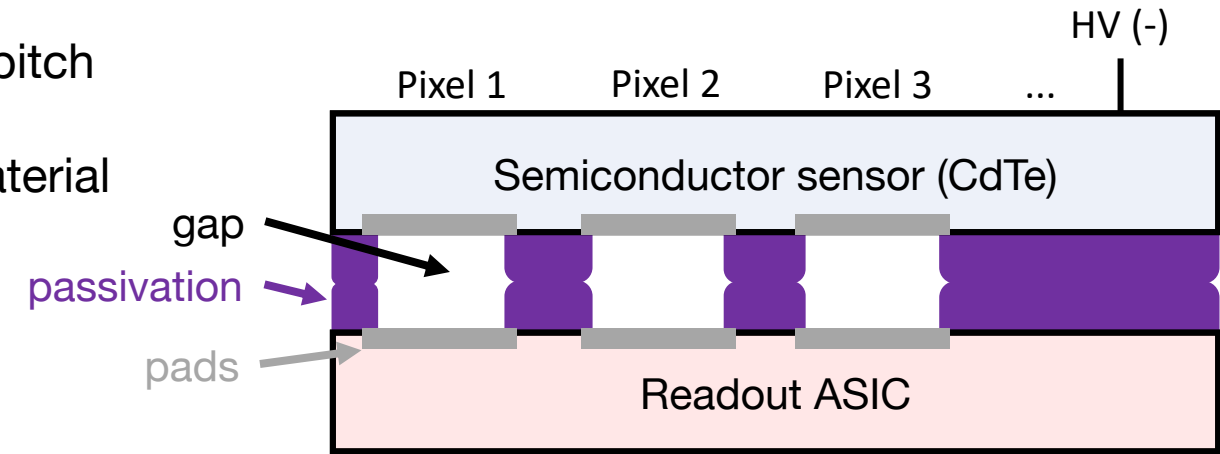
- Fixing parasitic effects in charge pump yields perfect linearity from 0 to 140 injected 30keV photons according to simulation (without noise!)
- Needs to be verified in lab measurement



Sensor/ASIC Assembly Prototypes

- Plan: Pixelwise flip-chip interconnection with $100\mu\text{m}$ pitch
- Need to fill gaps in between pads with conductive material
- Problems with CdTe:
 - No high temperatures ($>80^\circ\text{C}$)
 - No mechanical pressure

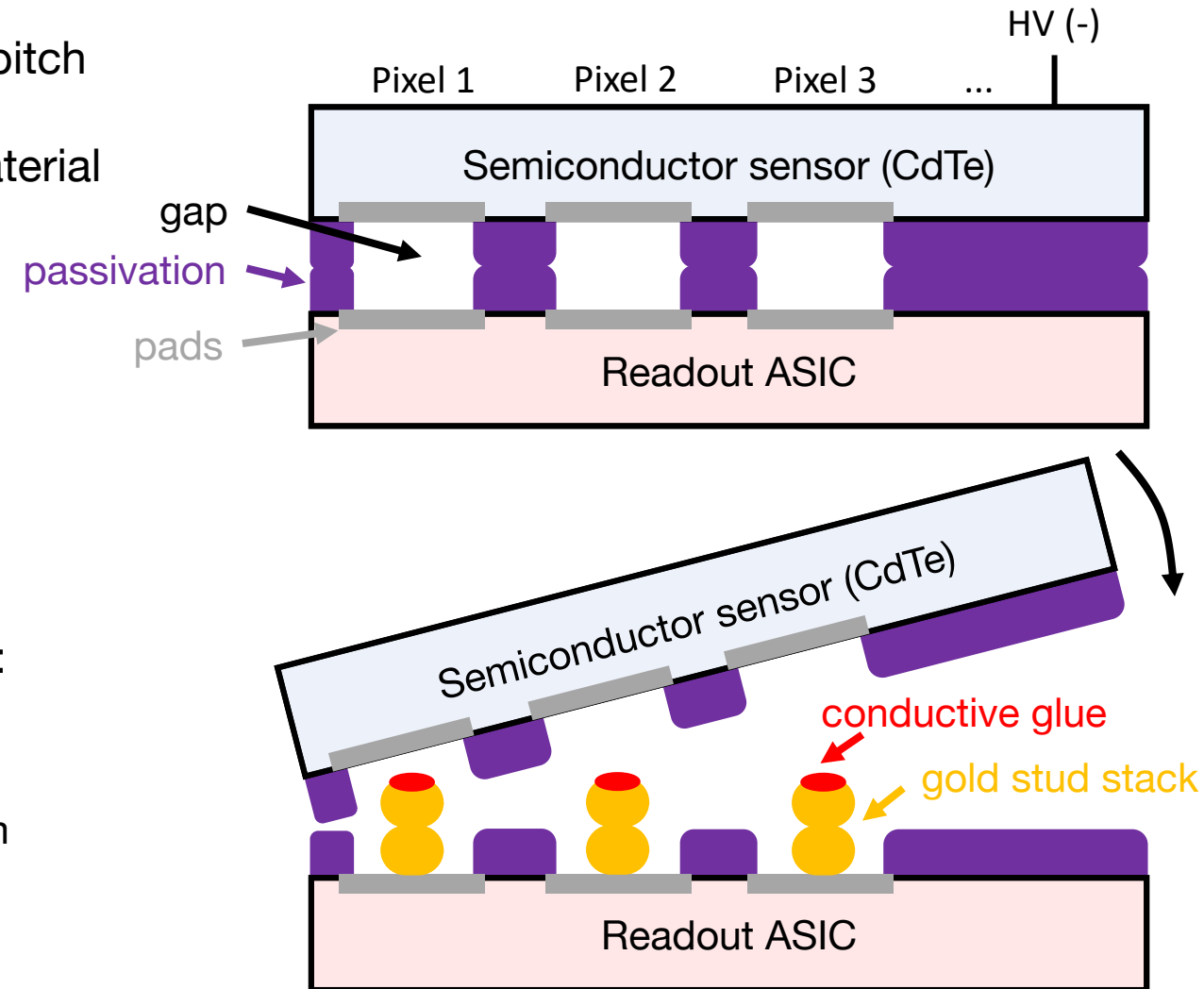
⇒ Soldering is out of question



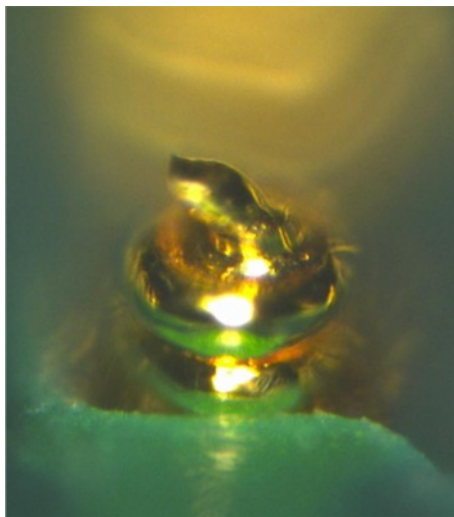
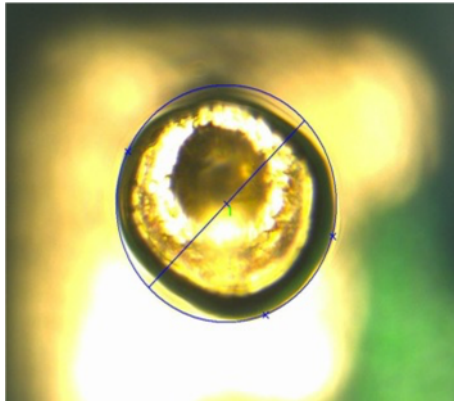
- Plan: Pixelwise flip-chip interconnection with 100 μ m pitch
- Need to fill gaps in between pads with conductive material
- Problems with CdTe:
 - No high temperatures (>80°C)
 - No mechanical pressure

⇒ Soldering is out of question

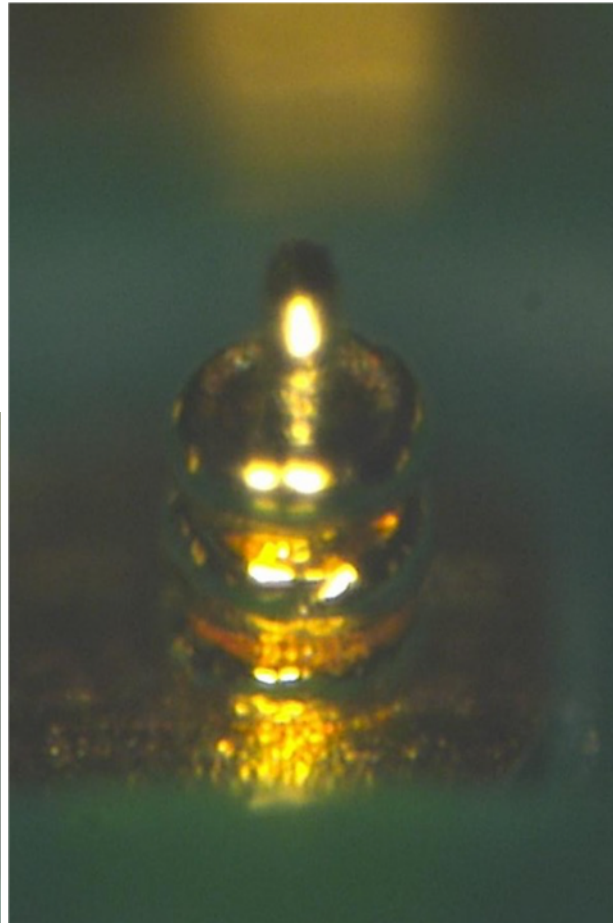
- Solution proposed and carried out by Christian Kreidl:
 - Place stack of gold studs on ASIC to fill gaps
 - Dip gold stud tips in conductive glue that cures at room temperature
 - Flip sensor on top



top view of 2 stacked gold studs, 80 μ m diameter

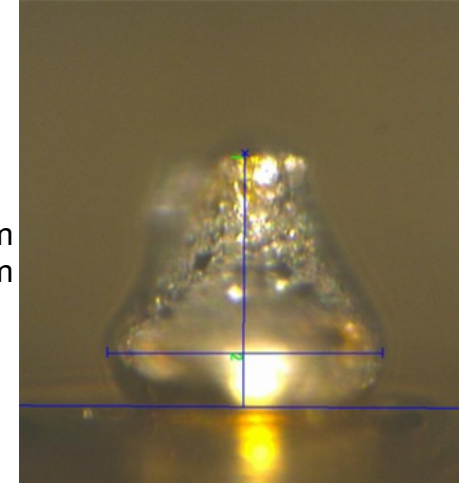


2 stacked gold studs with tail



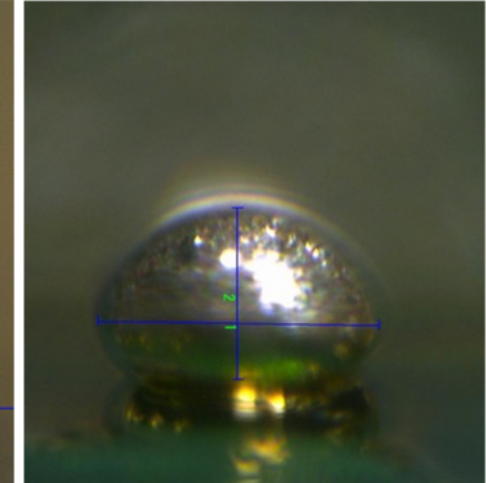
3 stacked gold studs with tail

1 gold stud with glue

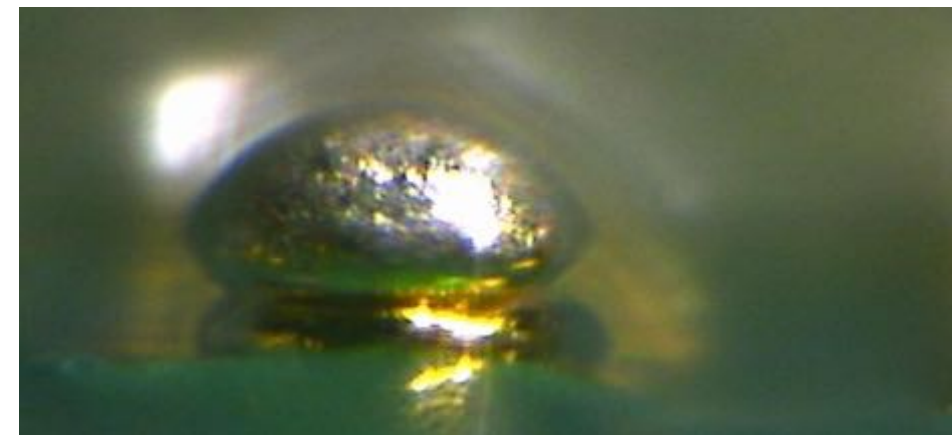


height: 80 μ m
width: 78 μ m

2 gold studs with glue

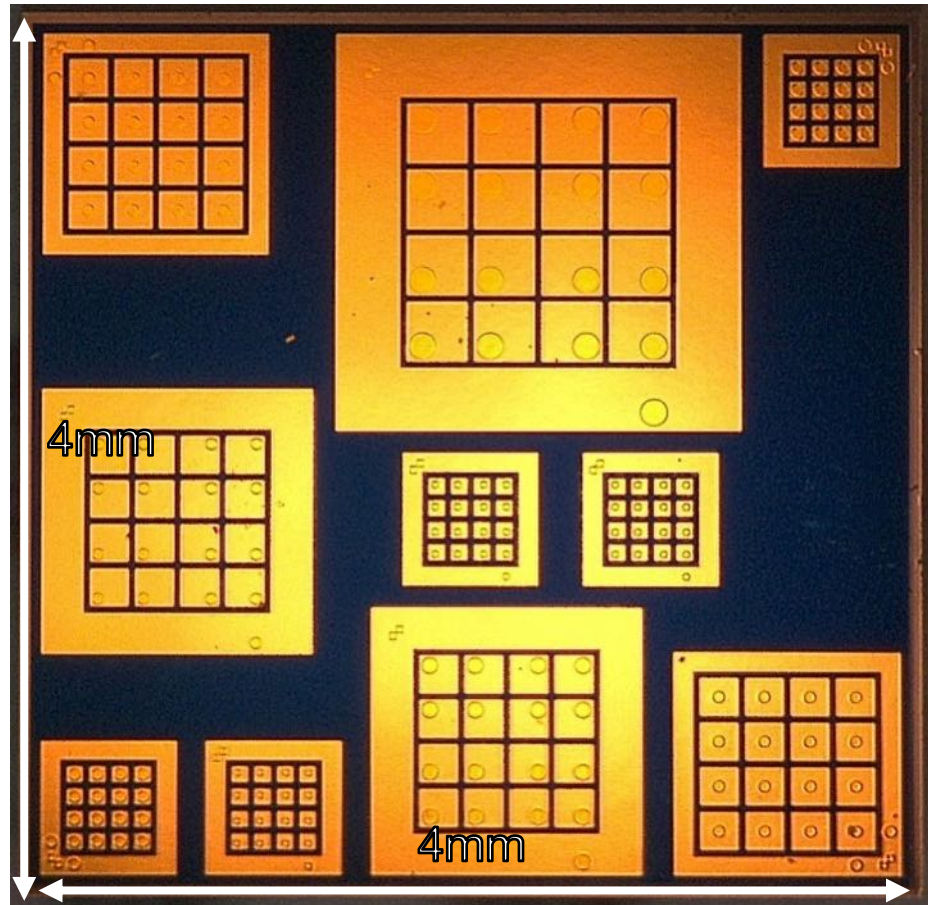


height: 83 μ m
width: 57 μ m



2 gold studs with glue

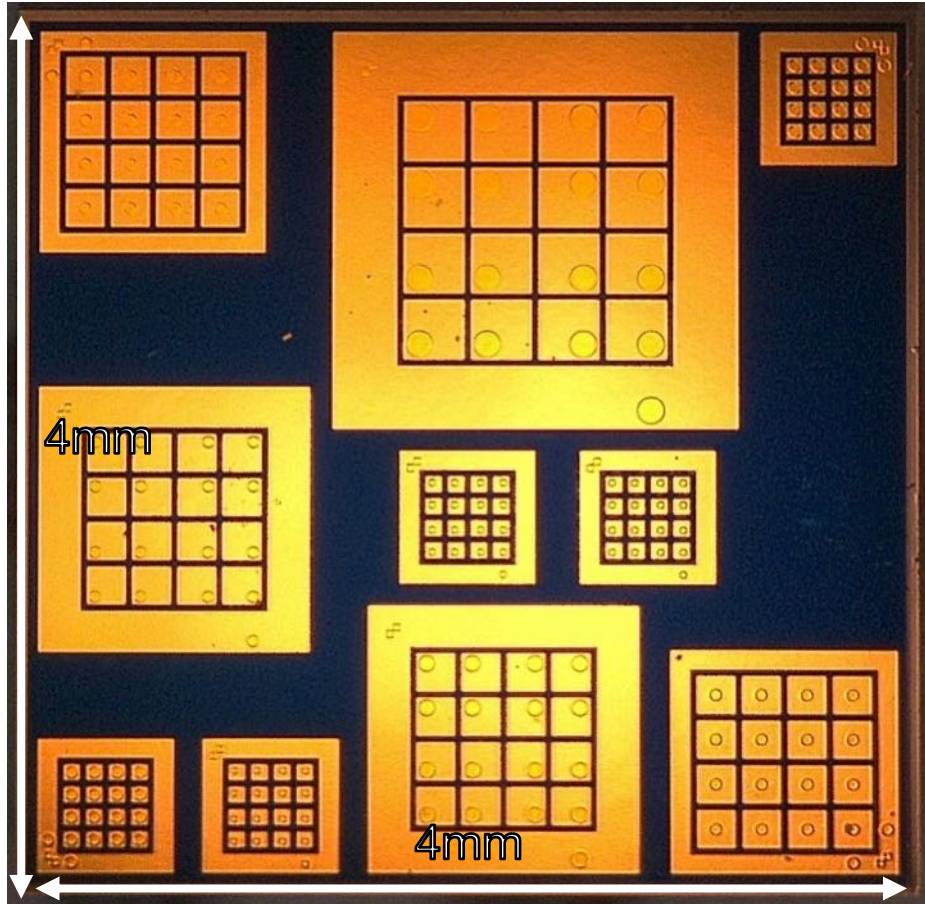
”Front” of CdTe prototype sensor



4x4 pixel test structures with guard ring and different pixels sizes and pitches (100µm, 200µm & 300µm)

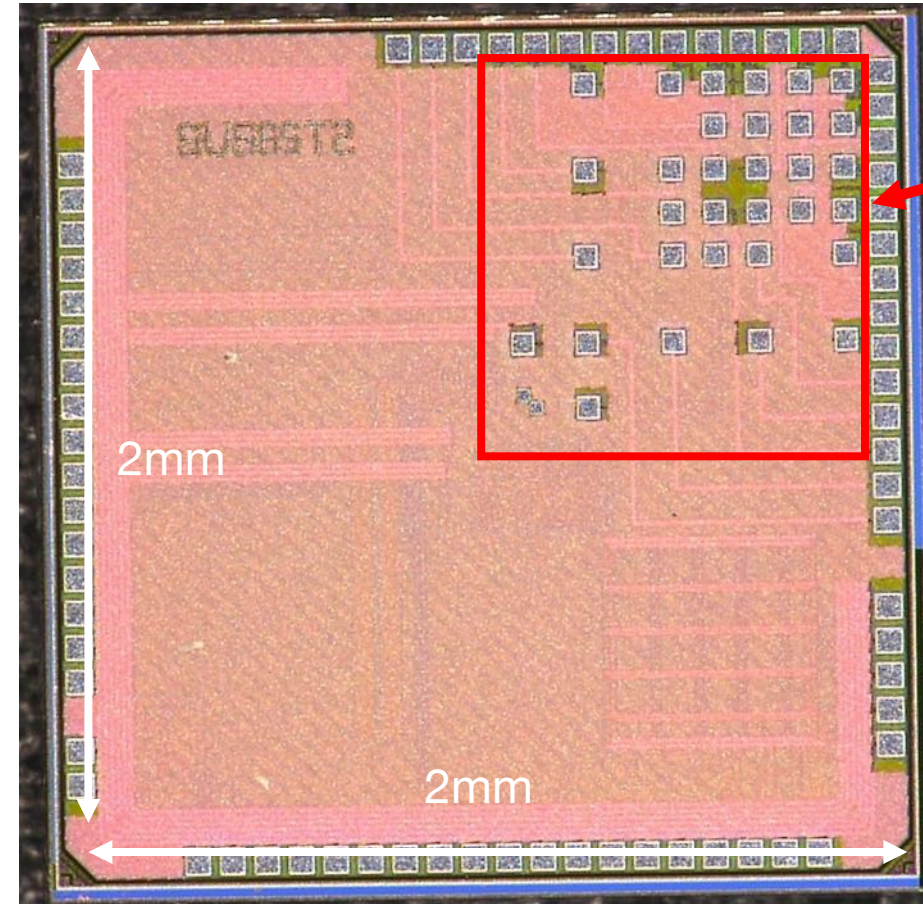
Design by ESRF, manufactured by Acrorad

”Front” of CdTe prototype sensor



Design by ESRF, manufactured by Acrorad

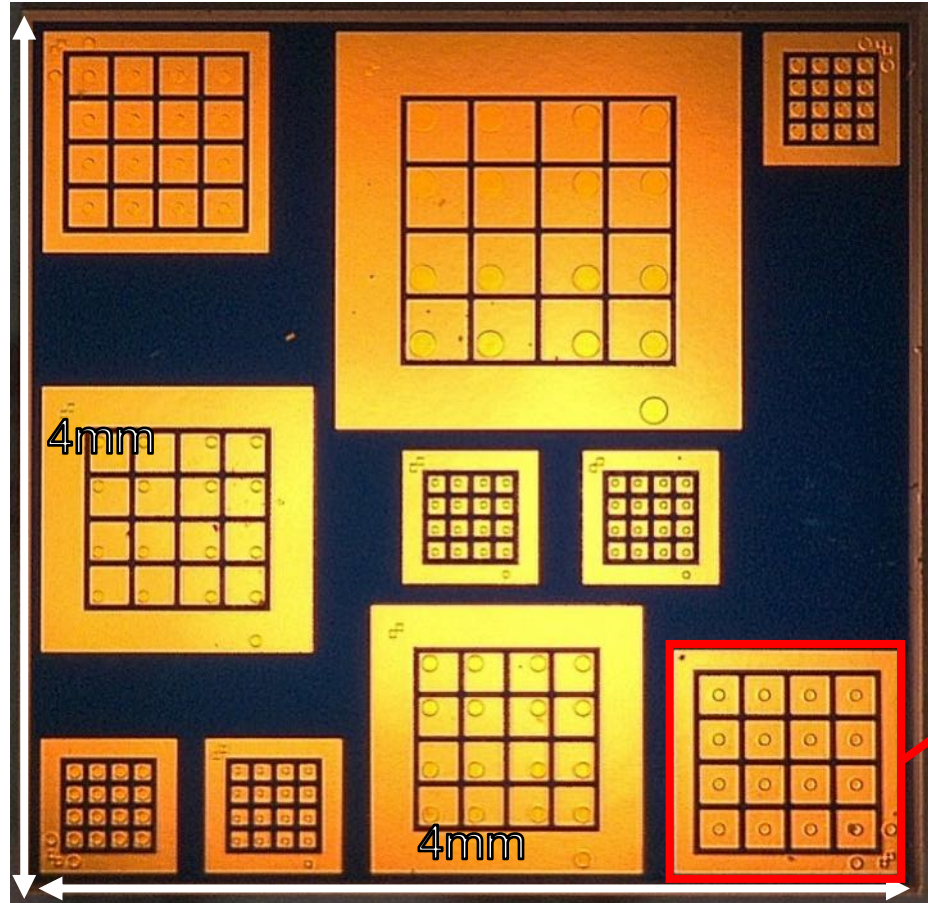
Top of ASIC prototype SUS65T2



Bump-bond
interconnection
area for 100 μ m
and 200 μ m pixel
pitch

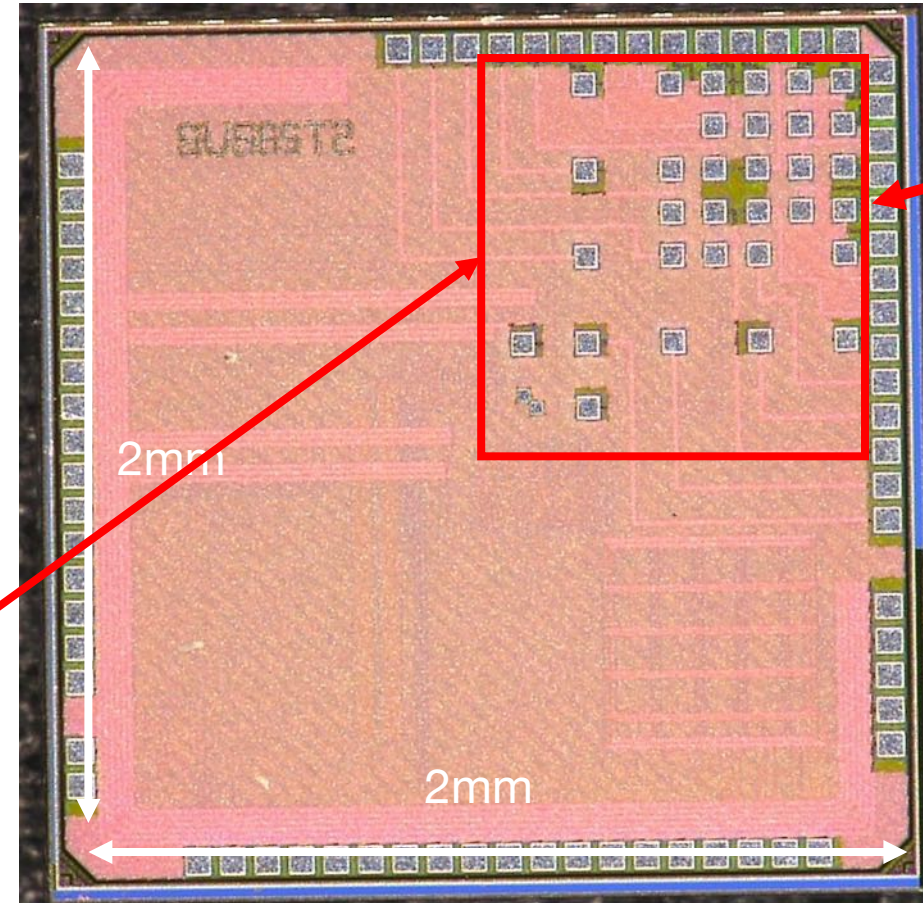
Design by HD, manufactured by TSMC

”Front” of CdTe prototype sensor



Design by ESRF, manufactured by Acrorad

Top of ASIC prototype SUS65T2



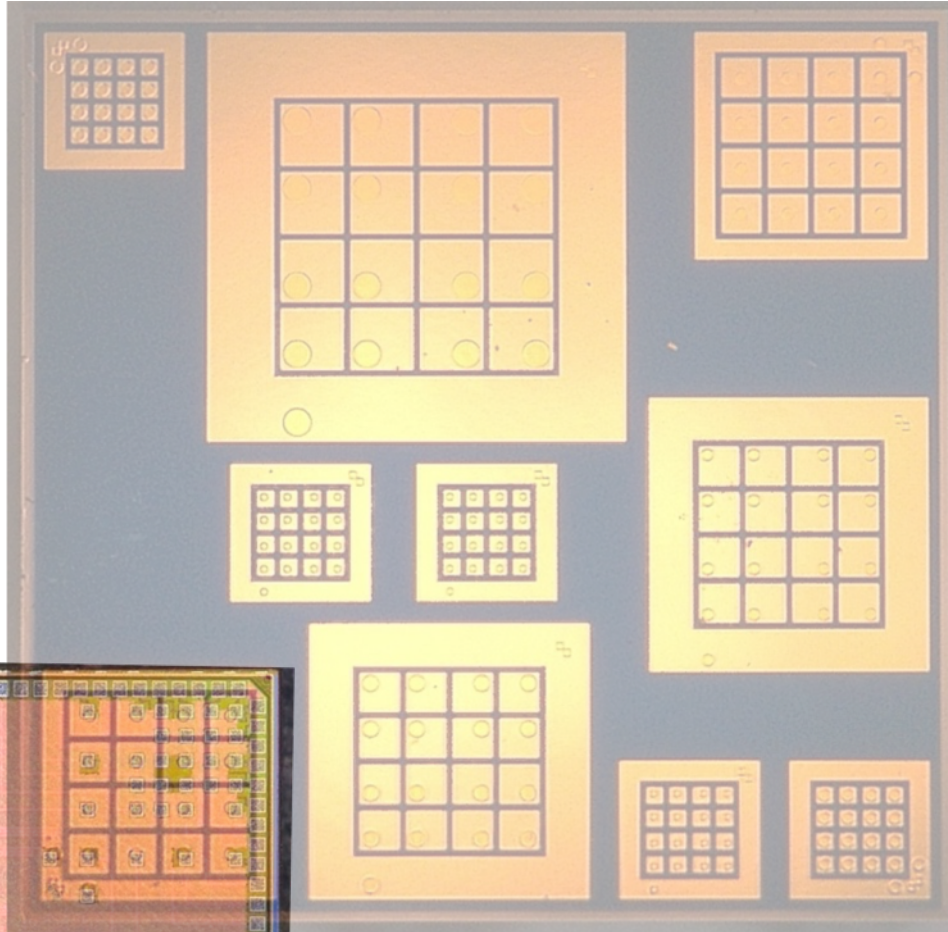
Design by HD, manufactured by TSMC

Flip on top

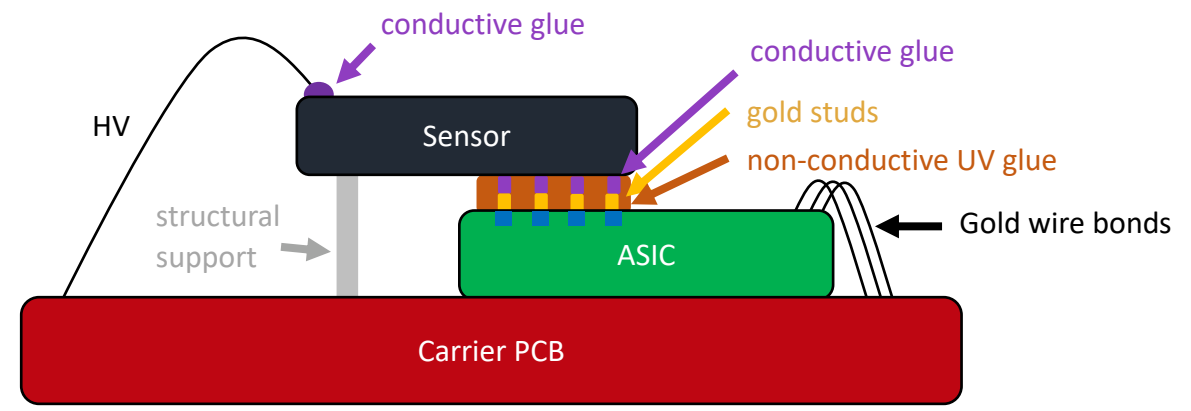
200 μ m
pitch

Bump-bond
interconnection
area for 100 μ m
and 200 μ m pixel
pitch

Huge overlap
Sensor needs mechanical support

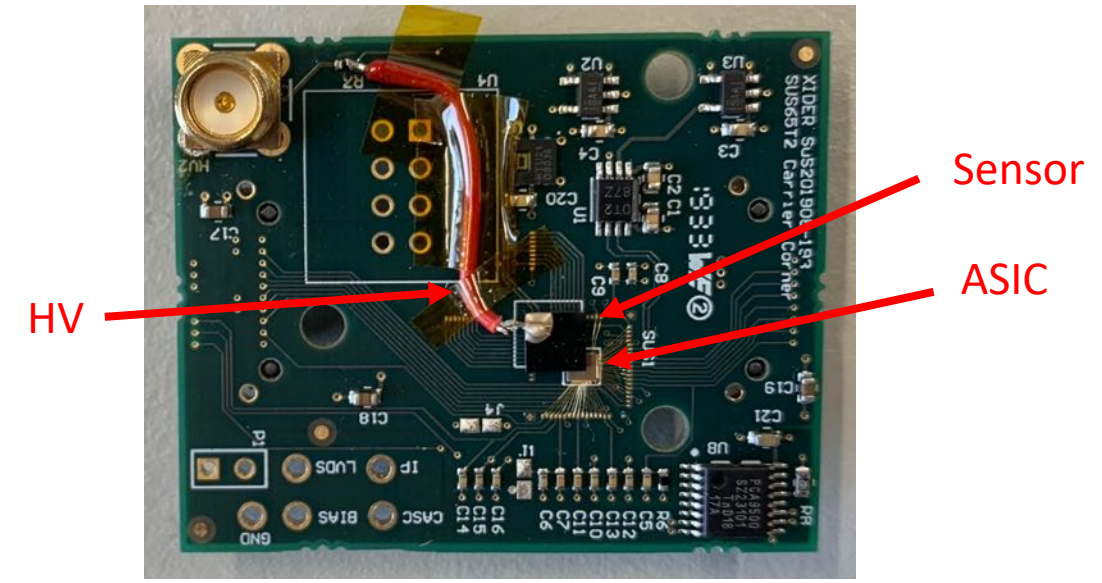


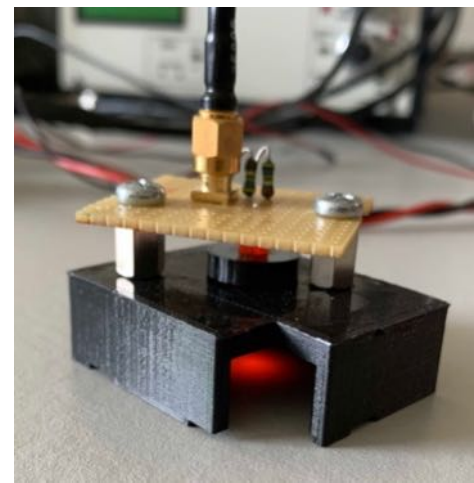
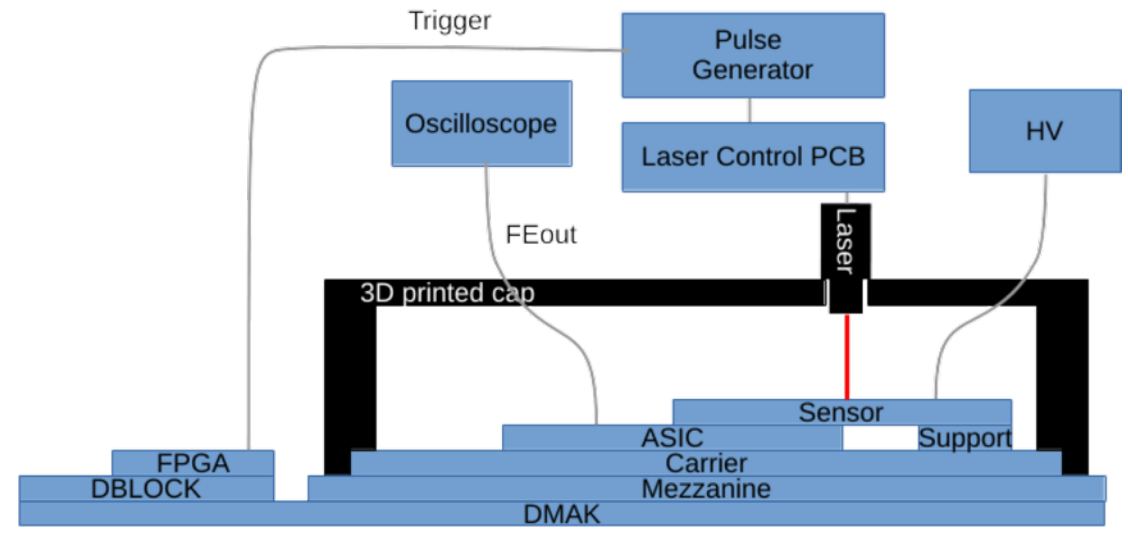
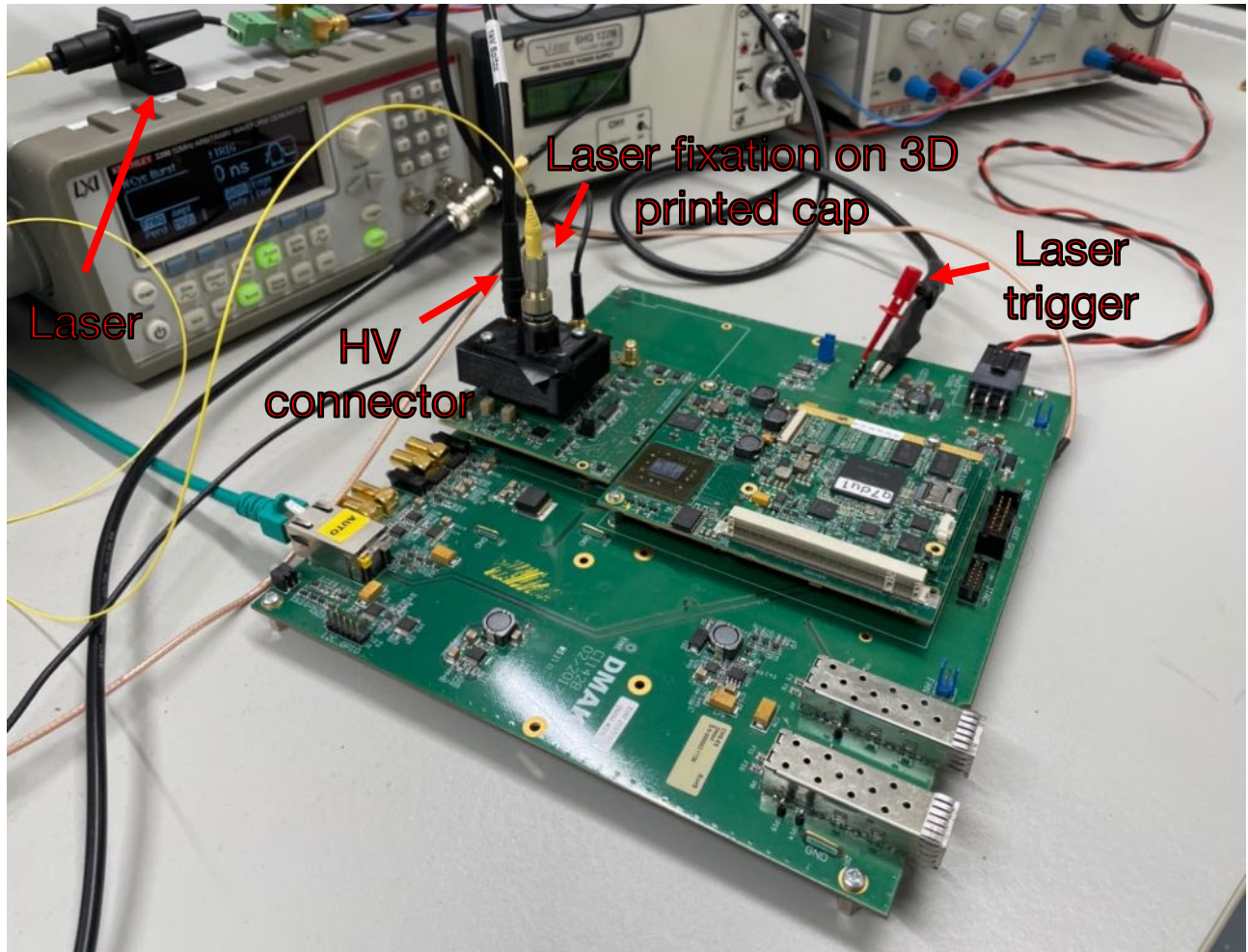
Schematic of ASIC/Sensor assembly on carrier PCB



Carried out by Christian Kreidl

After almost one year of trying: Our first ASIC/Sensor assembly built in-house!



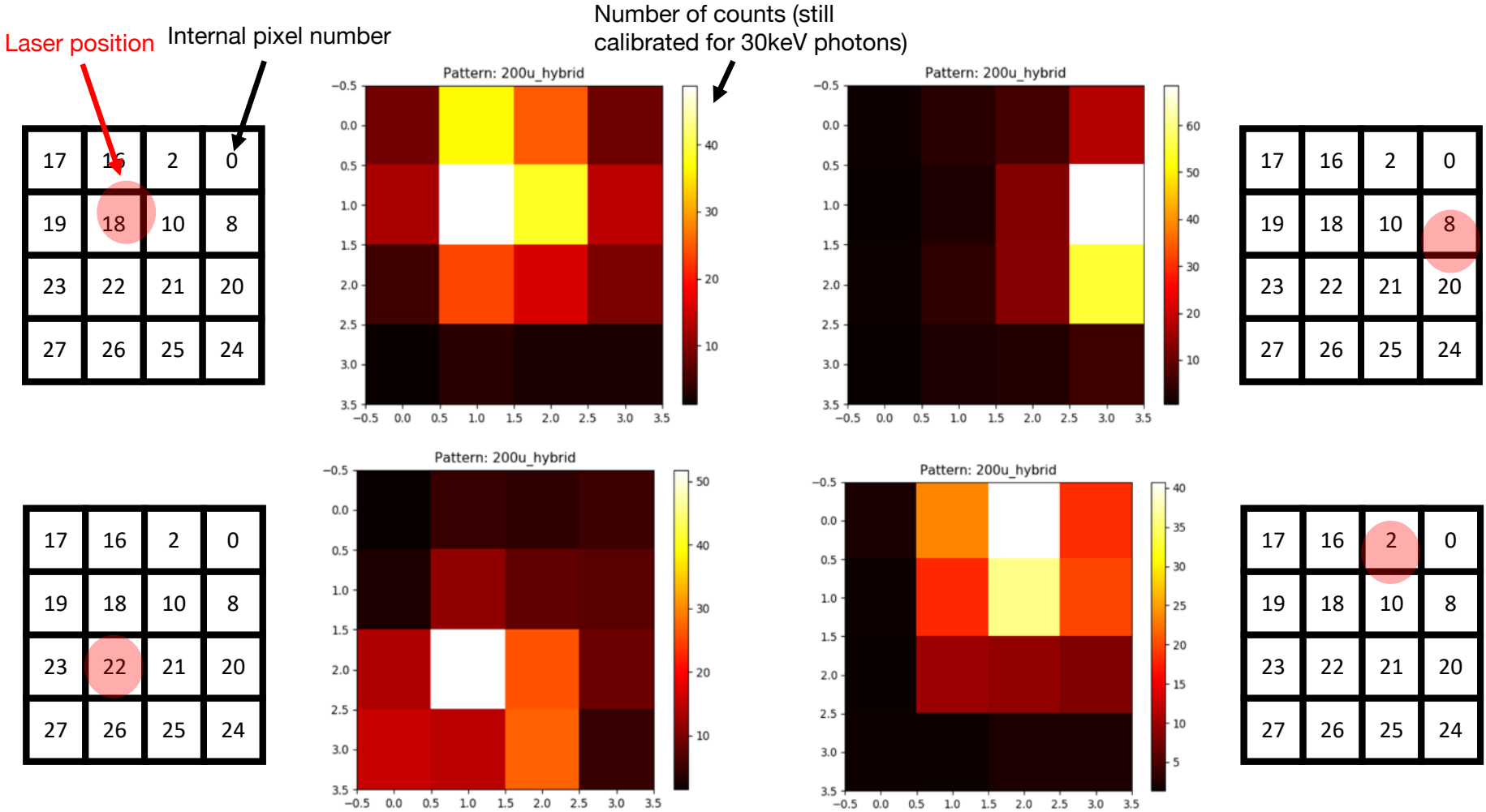


Unmounted 3D-printed cap with LED

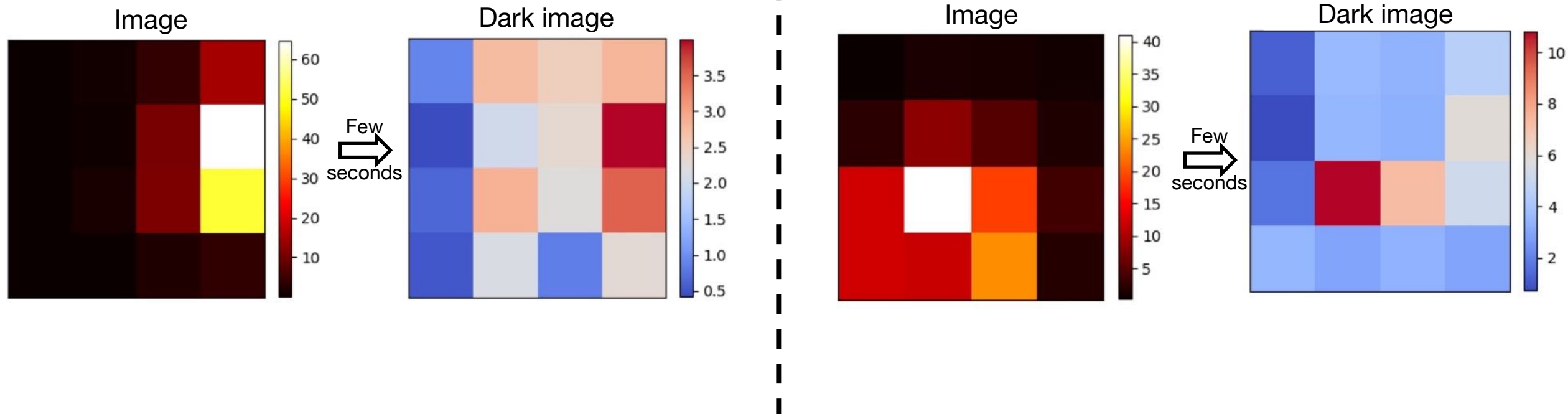


Mounted cap on carrier PCB

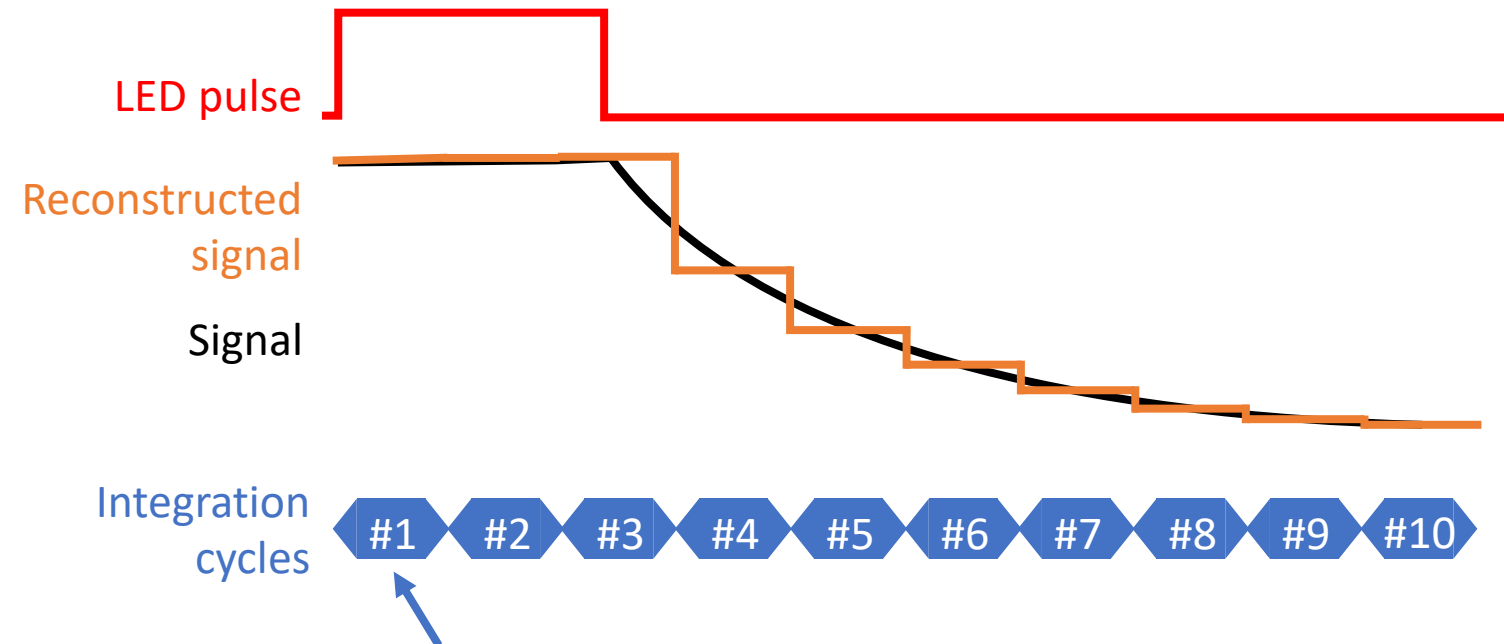
- Our first images taken with an actual CdTe sensor!
(2020 milestone)
- Proof for basic functionality of:
 - Sensor prototype
 - ASIC/Sensor interconnection
 - ASIC (Frontend, control, data readout, ..)



- But: Even seconds after taking an image, we still see a signal
⇒ Afterglow of CdTe Sensor

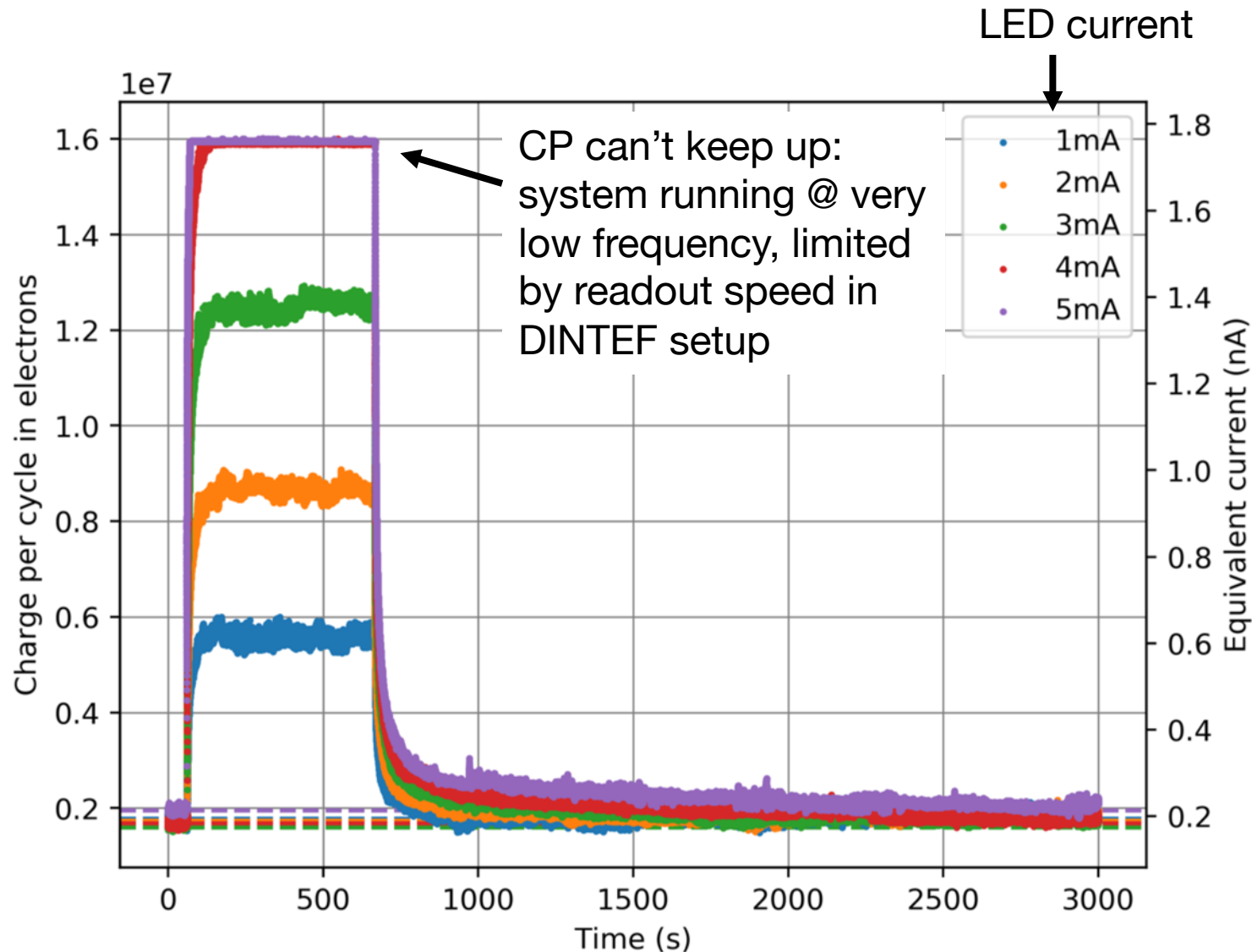


- Return to single pixel measurement
- Idea:
 - Shine LED on sensor for 10 minutes
 - Turn off LED
 - Measure signal throughout LED pulse & afterglow for 5 hours
- Aim:
 - Study time dependency of afterglow (does it depend on intensity of LED irradiation?)



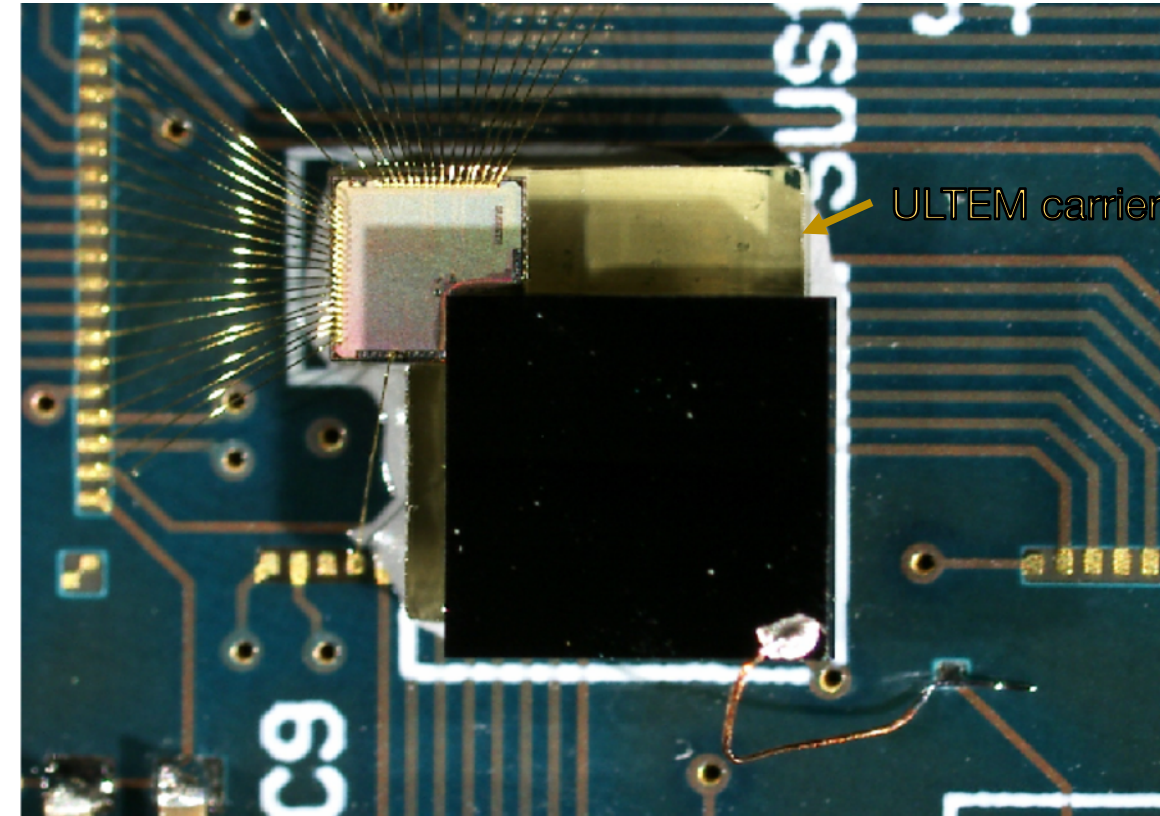
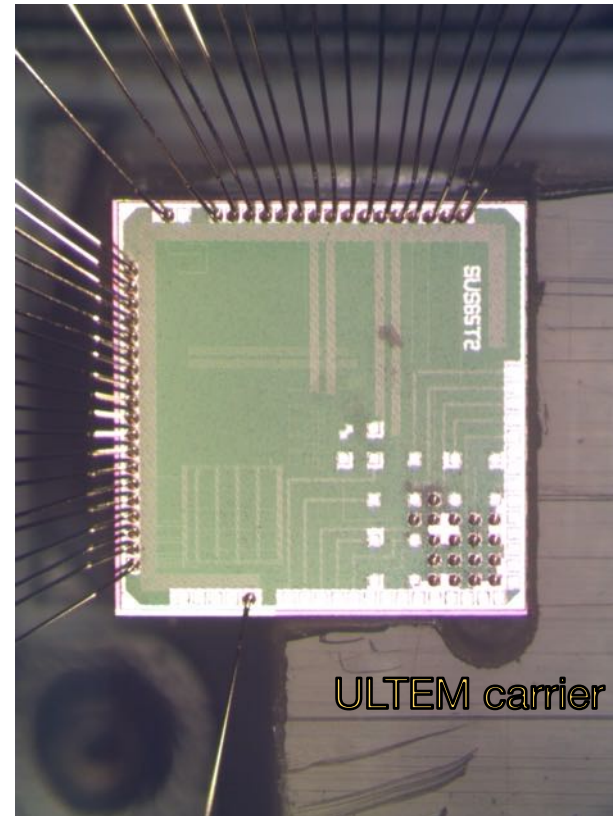
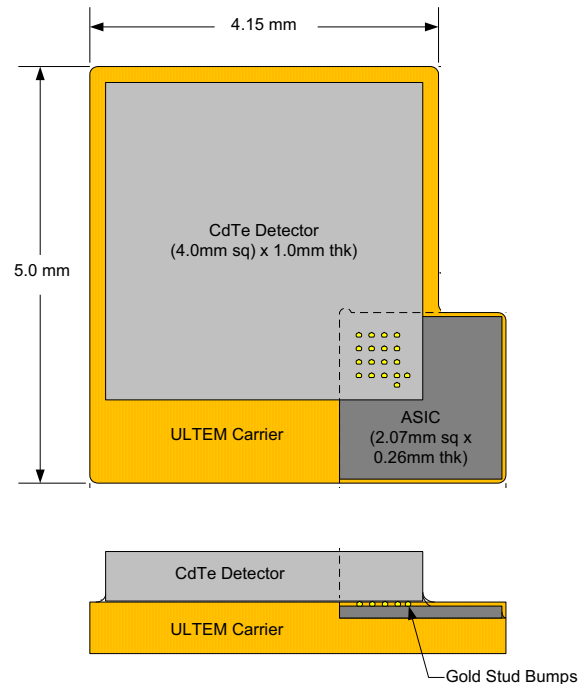
Size can be chosen in a wide range depending on input clock.
E.g. with 1MHz: 75us-2.2ms
In this measurement: 1.5ms

Trade-off between time resolution and signal sensitivity



- Even 30 minutes after LED irradiation, afterglow is still visible!
- Might be a show stopper for single photon sensitivity after high photon flux
- Needs further investigation (Marin Collonge)

- After more than a year, we finally found a commercial solution (Polymer Assembly Technology) for CdTe/ASIC interconnection
- Sensor prototype is supported by a plastic carrier
- First tests look very promising



- XIDer is a multi-purpose detector for time-resolved x-ray experiments at the ESRF
- Uses unconventional approach to combine single photon sensitivity and high dynamic range
- My tasks:
 - Design and characterise the readout ASIC
 - Verify feasibility
 - Develop design concepts for large scale integration
- ASIC prototypes SUS65T1, SUS65T2 and SUS65T3 have been characterised and show very satisfying performance
- No show stopper on chip side (yet)
- First sensor measurements after long interconnection struggle
- Is sensor material good enough? Should we start with Silicon? Hope for CZT...

- Solutions for large scale system integration (partially done):
 - Frame-wise frontend commands (called telegram)
 - Data storage
 - Design of output data links for high data rates (several tens of GB/s)
 - Automated frontend calibration, maybe via on-chip processor
- Array compatible layout
- Characterise sensor with new sensor/ASIC assemblies
- Perform beamline measurements at ESRF with Sensor/ASIC assemblies
- Use sensor measurement findings to further refine ASIC design
- Design first draft of final detector module
- Design "final testchip"

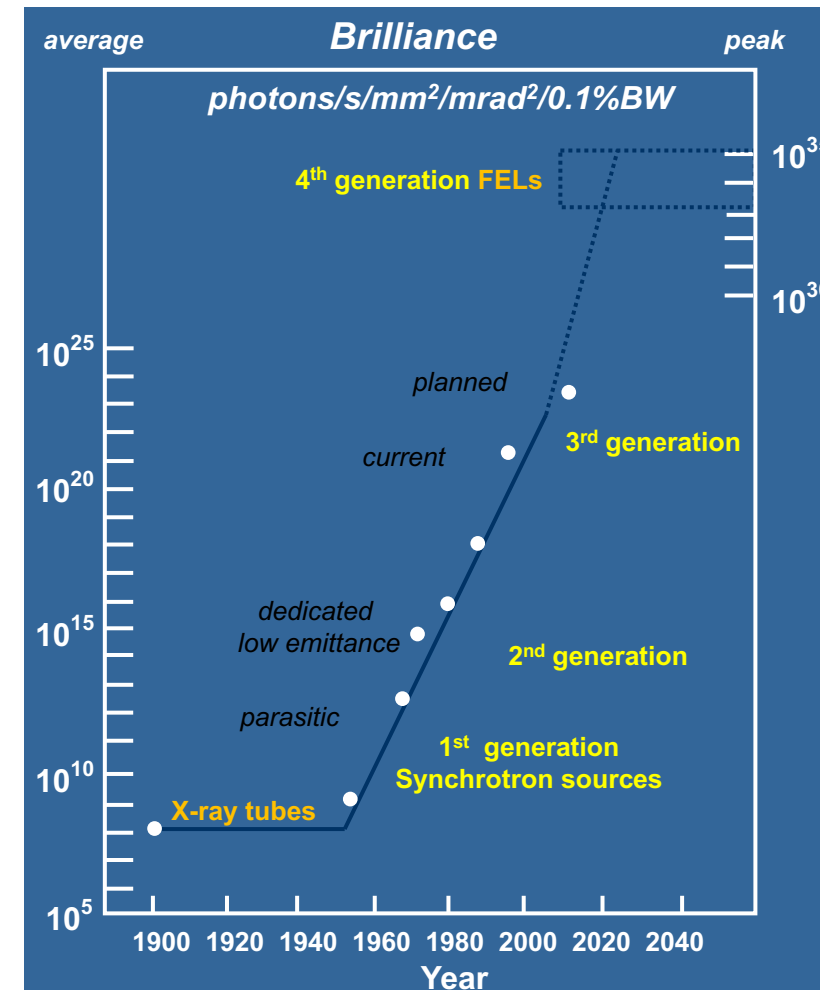
Backup

$$\text{SR Brilliance} = \frac{\text{photon flux}}{(\Delta A) (\Delta \Omega) (\Delta \lambda / \lambda)}$$

source area solid angle spectral interval

- **The** figure of merit for a synchrotron's performance
- High brilliance \triangleq high flux of useful photons at the sample and detector

- 1st : Particle accelerators that generate synchrotron light as a parasitic effect
- 2nd : Dedicated synchrotron light production
- 3rd : Higher brilliance by introducing insertion devices (wigglers/undulators)
- 4th : Even higher brilliance and coherence

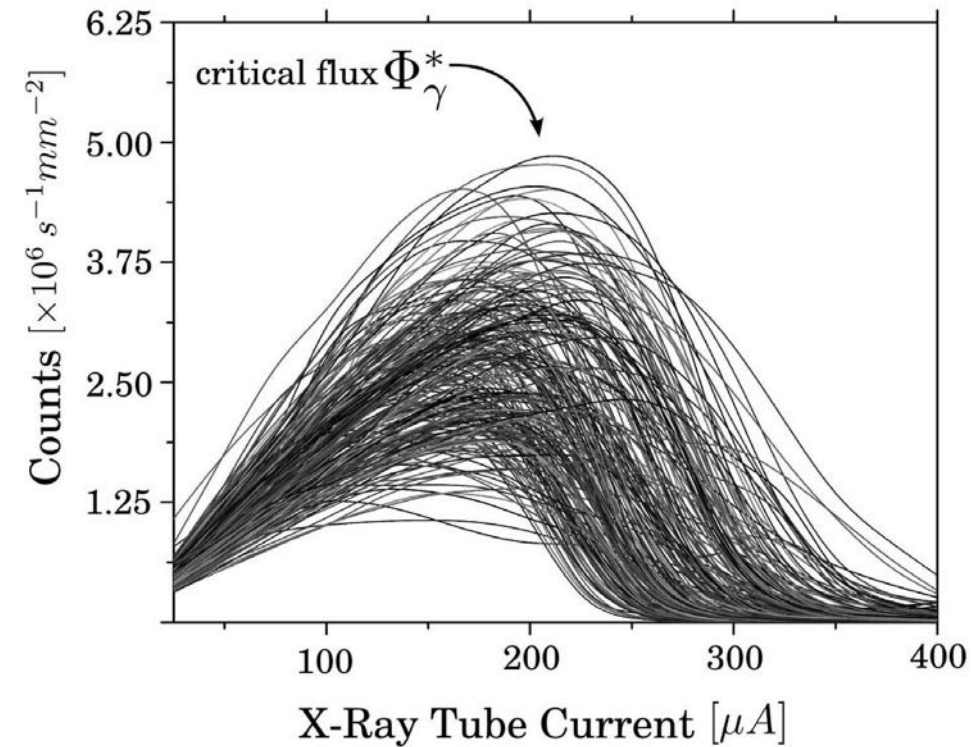




Taken from H. Shiraki et al „THM growth and characterization of 100 mm diameter CdTe single crystals“, IEEE Trans. Nucl. Sci, vol. 54, pp. 117-1723, 2009

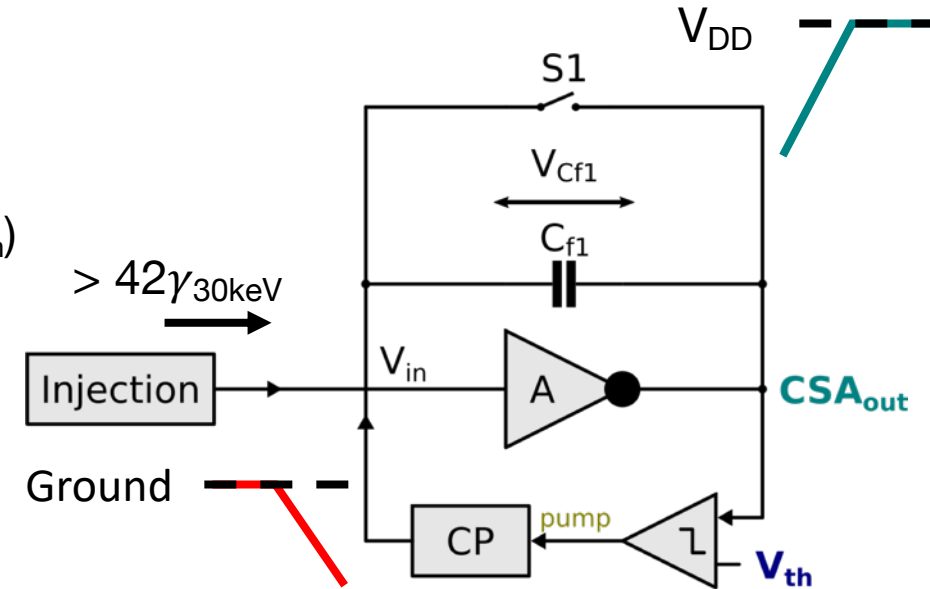
- 100mm diameter, 300mm length

Count rate collapses for high photon fluxes:



Taken from „Nature of polarization in wide-bandgap semiconductor detectors under high-flux irradiation: Application to semi-insulating $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$ “ (D. S. Bale, C. Szeles, Phys. Rev. B, 2008)

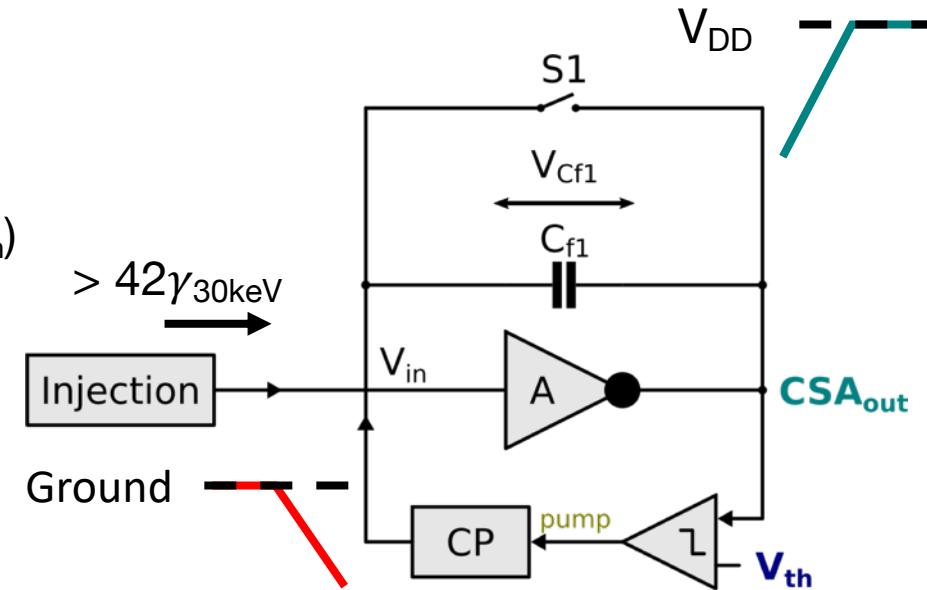
- Charge integration is still working due to charge conservation:
 - Injected charge has no other path to flow off
 - Charge has to be stored on C_{f1} following $Q = C_{f1} \cdot V_{Cf1} = C_{f1} \cdot (CSA_{out} - V_{in})$
 - CSA_{out} can't increase any further, so V_{in} **decreases instead**
 - In first order, this does not affect the measurement:
 - The continuous conversion only cares about the actual charge, not the voltages
- ⇒ Frontend still linear beyond injected charge of $42\gamma_{30keV}$

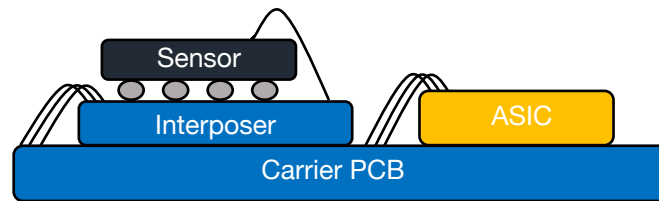


- Charge integration is still working due to charge conservation:
 - Injected charge has no other path to flow off
 - Charge has to be stored on C_{f1} following $Q = C_{f1} \cdot V_{Cf1} = C_{f1} \cdot (CSA_{out} - V_{in})$
 - CSA_{out} can't increase any further, so V_{in} **decreases instead**
- In first order, this does not affect the measurement:
 - The continuous conversion only cares about the actual charge, not the voltages

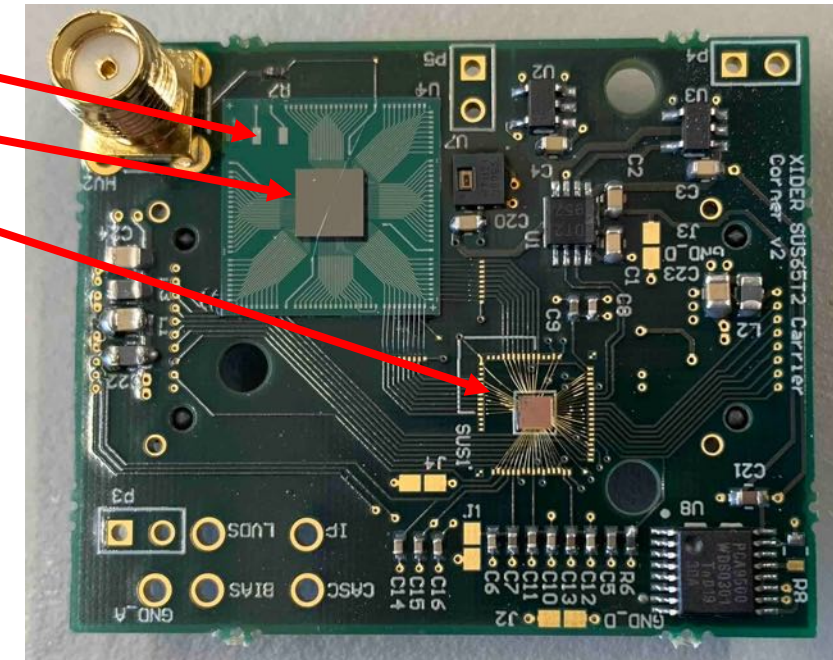
⇒ Frontend still linear beyond injected charge of $42\gamma_{30keV}$
- But: If V_{in} drifts off too far, the charge package size begins to change because of parasitic charge injection effects in the charge pump

⇒ Bend of the curve above roughly $80\gamma_{30keV}$

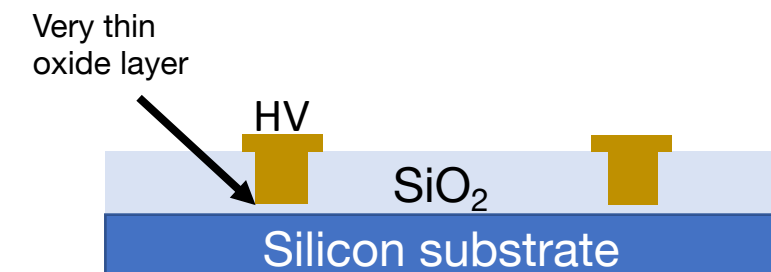


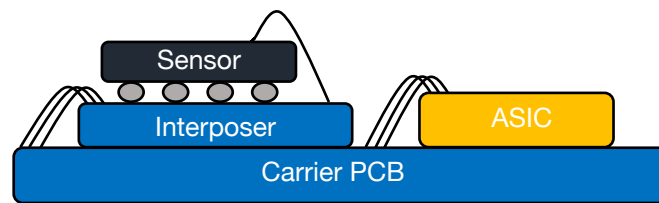


Interposer (design by ESRF)
Sensor (ESRF)
ASIC (HD)



- Use sensor interposer (silicon) for easier bump bonding process
- Sensor/interposer bump bonding performed by external company
- Glue and wire bond interposer to PCB
- Route sensor pixel outputs on PCB to ASIC and connect via wire-bonds
- Interposer needed Al-bonds (which we can't do in-house)
 - ⇒ Ask Ralf Achenbach from KIP for help
- Unfortunately: The interposer pad insulation is too weak to carry sensor HV (500V), even though the manufacturer knew that we route the HV across the interposer
 - ⇒ Every interposer in use breaks down as soon as sensor HV is applied

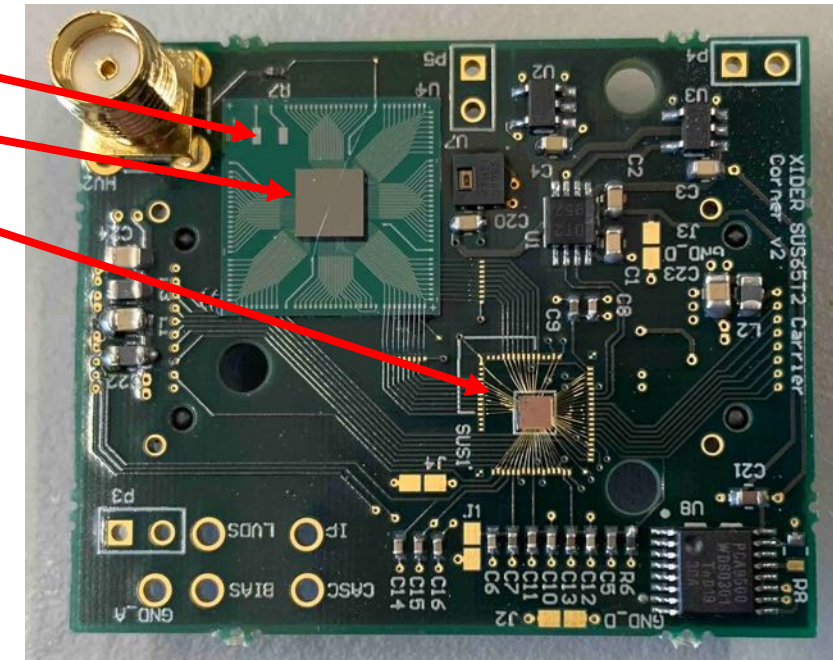




Interposer (design by ESRF)

Sensor

ASIC



- Use sensor interposer (silicon) for easier bump bonding process
- Sensor/interposer bump bonding performed by external company
- Glue and wire bond interposer to PCB
- Route sensor pixel outputs on PCB to ASIC and connect via wire-bonds
- Interposer needed Al-bonds (which we can't do in-house)
 - ⇒ Ask Ralf Achenbach from KIP for help
- Unfortunately: The interposer pad insulation is too weak to carry sensor HV (500V), even though the manufacturer knew that we route the HV across the interposer
 - ⇒ Every interposer in use breaks down as soon as sensor HV is applied

Very thin
oxide layer

