From small debugging steps to a GRAND result

for the SoC Interest Group Meeting, CERN

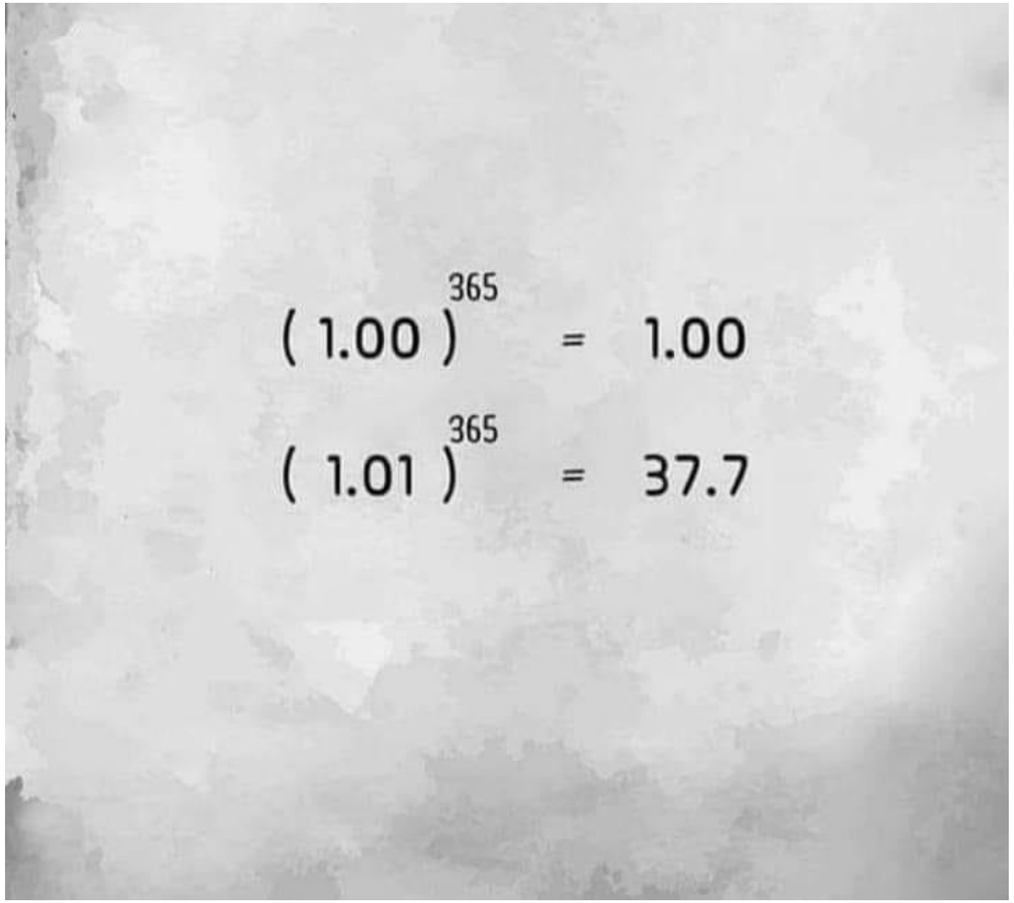
Oct 2020

Radboud University

From small debugging steps to a GRAND result

Agenda

– Project outline
– Strategy board design
– Debugging proces
– Results
– “Lessons learned”



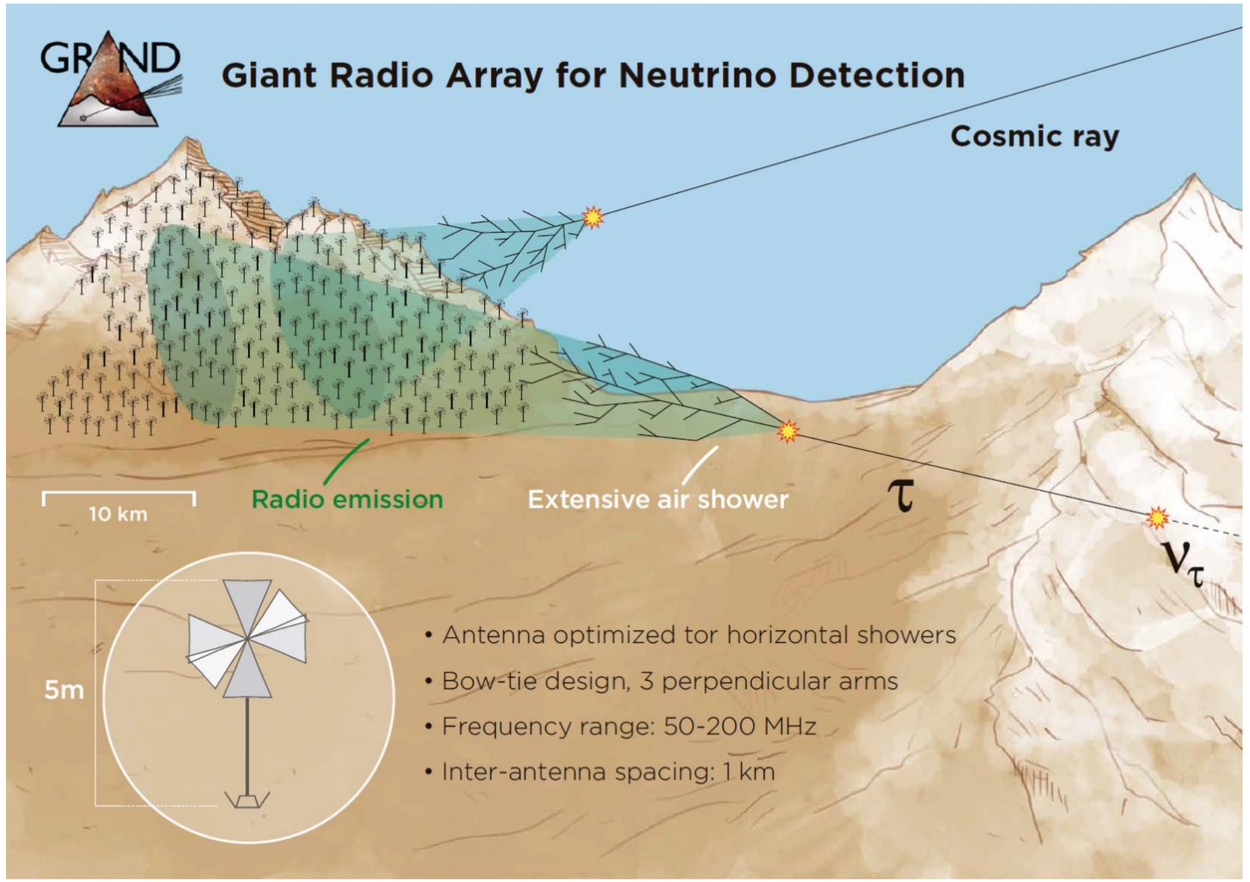
GRAND – Giant Radio Array for Neutrino Detection

Initiative of Olivier Martineau (scientist: LPNHE)
Group in Nijmegen working on GRAND

Department: High Energy Physics
– Sijbrand de Jong

GRAND:
– Charles Timmermans (scientist: Nikhef)
– Dániel Szálas-Motesiczky (engineer: RU)
– Floris Hahn (PCB designer: Techno Center)

– René Habraken (engineer: RU)
r.habraken@science.ru.nl

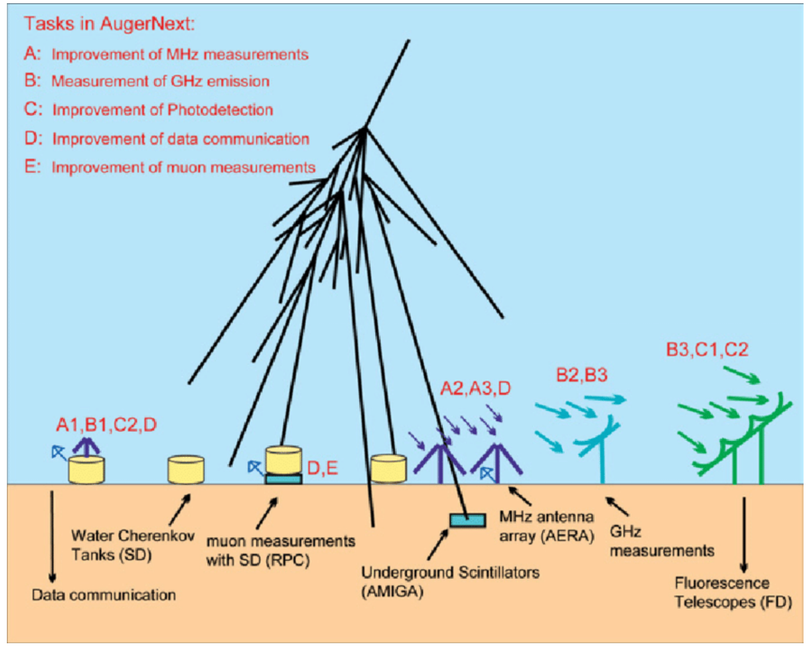


AERA

– *Electronics Auger Engineering Radio Area*

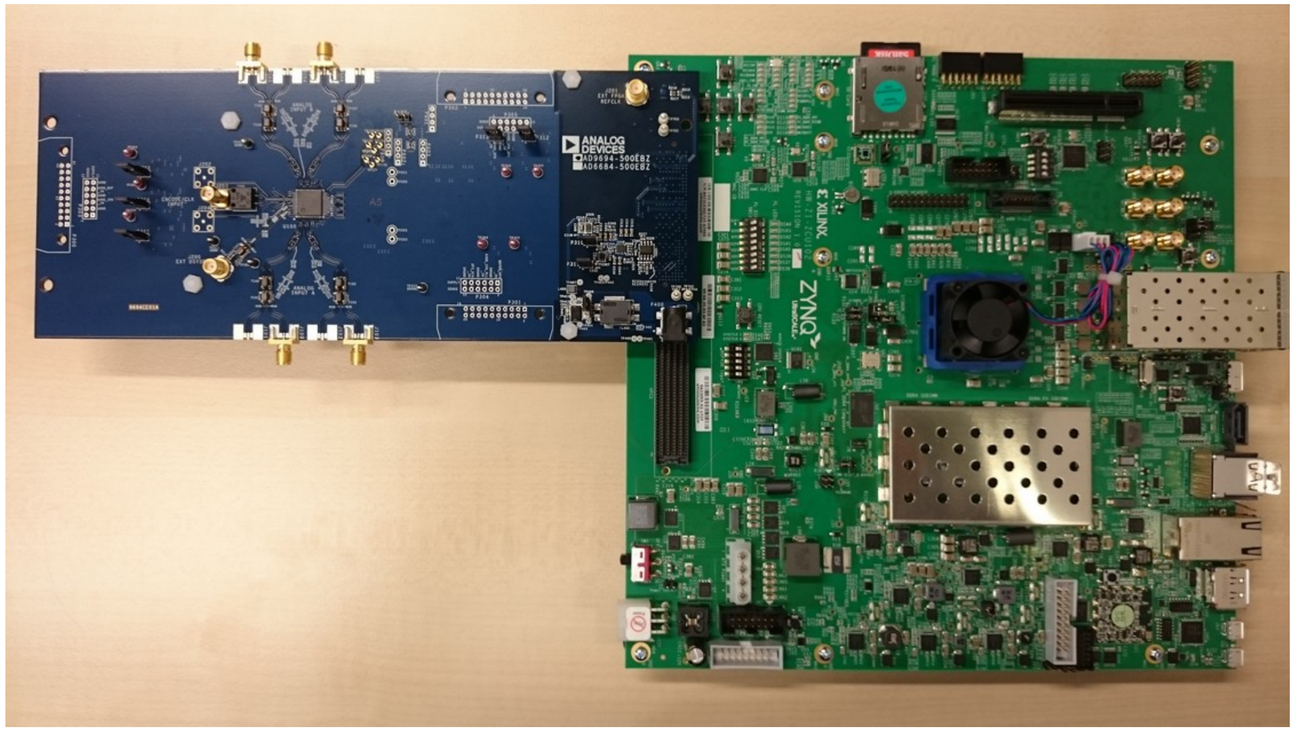
“SMALL” before “GRAND” ???
→ Not really!

Installment in May 2013 in Argentina
100 antennas
6 km2



Merge Analog Devices with Xilinx ref design

Analog Devices
ad9694-500ebz
reference board



Xilinx ZCU102
reference board

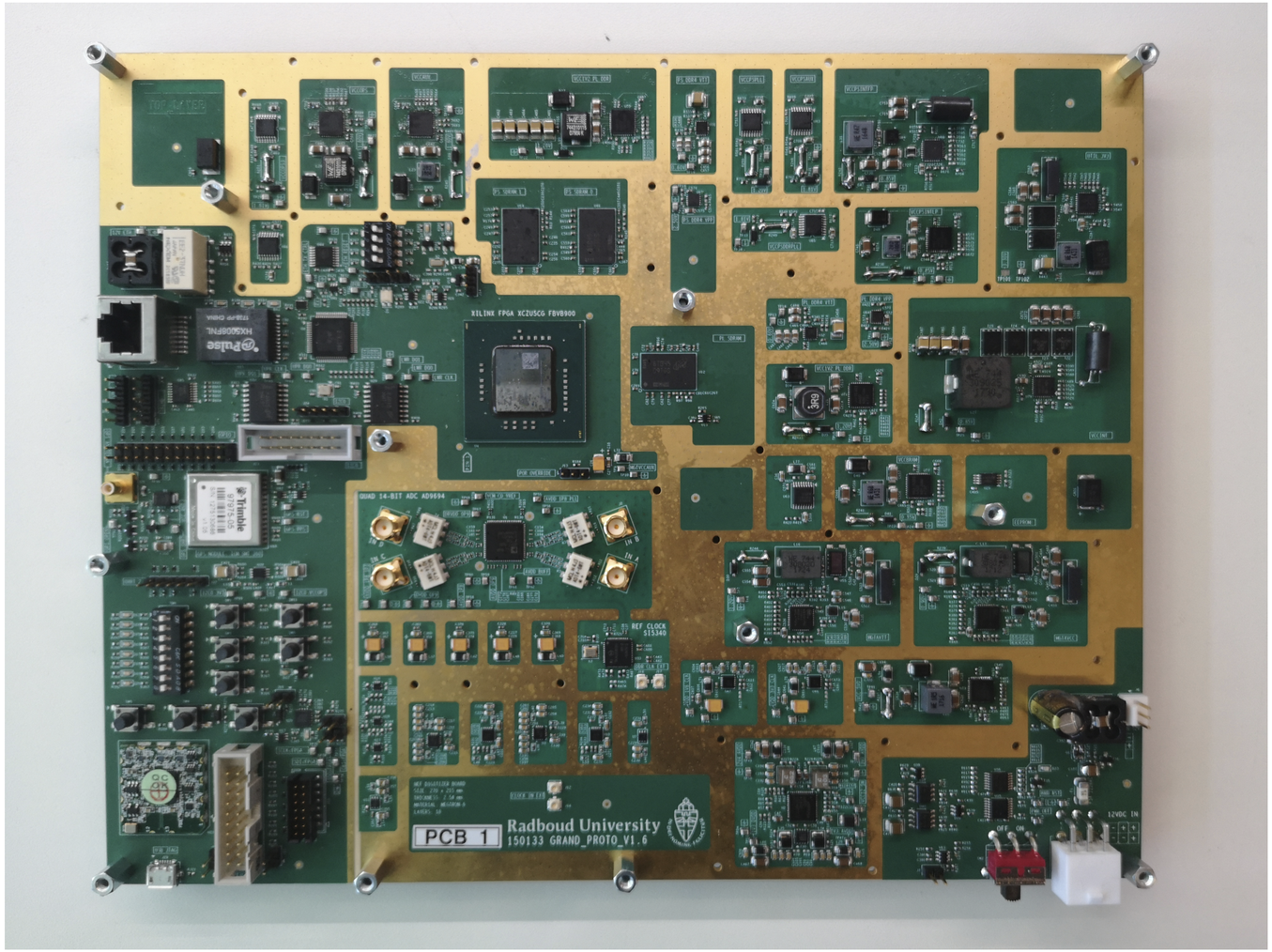
Both companies provide schematics, BoM, board layout

GRAND prototype V1

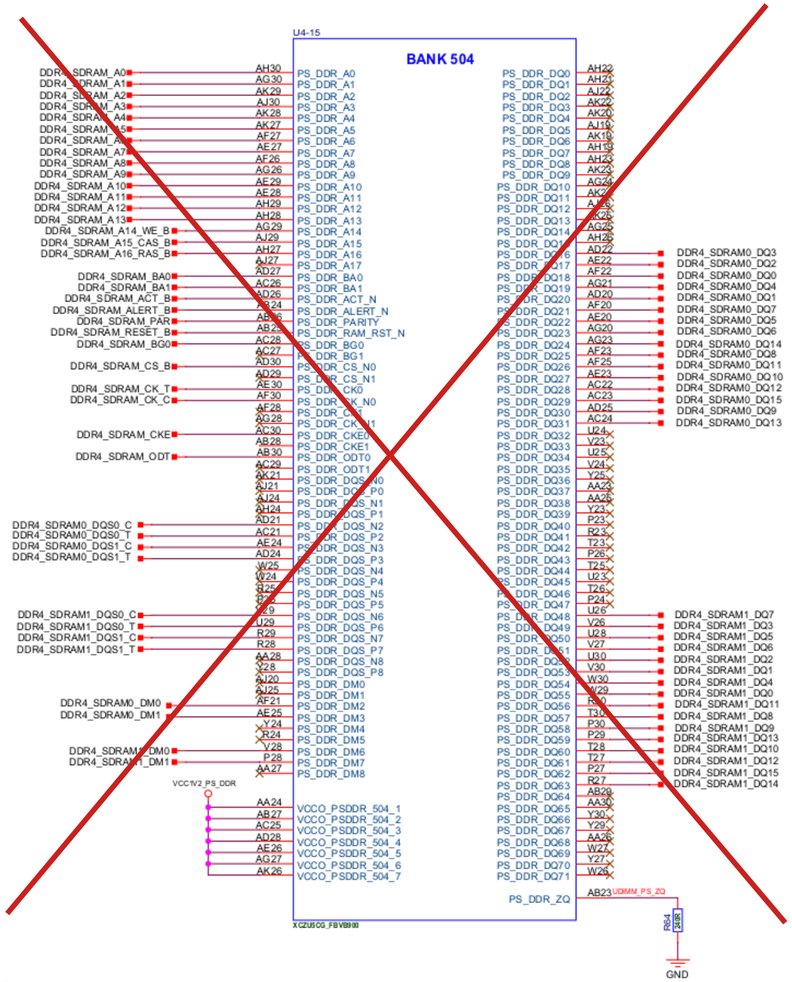
Key features DAQ
Trigger logic and control
FPGA+CPU
ZynqMP: XCZU7CG-1FBVB900E

4 channels
14 bit, 500MSPS ADC
30 – 200 MHz
GPS position and timing
Long range WiFi data transfer

Start development towards a more integrated, reliable and cheap DAQ while using less power.



DDR4 memory


U4-15
BANK 504
PS_DDR_A0
PS_DDR_A1
PS_DDR_A2
PS_DDR_A3
PS_DDR_A4
PS_DDR_A5
PS_DDR_A6
PS_DDR_A7
PS_DDR_A8
PS_DDR_A9
PS_DDR_A10
PS_DDR_A11
PS_DDR_A12
PS_DDR_A13
PS_DDR_A14
PS_DDR_A15
PS_DDR_A16
PS_DDR_A17
PS_DDR_BA0
PS_DDR_BA1
PS_DDR_ACT_N
PS_DDR_ALERT_N
PS_DDR_PARITY
PS_DDR_RAM_RST_N
PS_DDR_BG0
PS_DDR_BG1
PS_DDR_CS_N0
PS_DDR_CS_N1
PS_DDR_CK0
PS_DDR_CK_N0
PS_DDR_CK_N1
PS_DDR_CKE0
PS_DDR_CKE1
PS_DDR_ODT0
PS_DDR_ODT1
PS_DDR_DQS_N0
PS_DDR_DQS_P0
PS_DDR_DQS_N1
PS_DDR_DQS_P1
PS_DDR_DQS_N2
PS_DDR_DQS_P2
PS_DDR_DQS_N3
PS_DDR_DQS_P3
PS_DDR_DQS_N4
PS_DDR_DQS_P4
PS_DDR_DQS_N5
PS_DDR_DQS_P5
PS_DDR_DQS_N6
PS_DDR_DQS_P6
PS_DDR_DQS_N7
PS_DDR_DQS_P7
PS_DDR_DQS_N8
PS_DDR_DQS_P8
PS_DDR_DM0
PS_DDR_DM1
PS_DDR_DM2
PS_DDR_DM3
PS_DDR_DM4
PS_DDR_DM5
PS_DDR_DM6
PS_DDR_DM7
PS_DDR_DM8
PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31
PS_DDR_DQ32
PS_DDR_DQ33
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PS_DDR_DQ35
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PS_DDR_DQ37
PS_DDR_DQ38
PS_DDR_DQ39
PS_DDR_DQ40
PS_DDR_DQ41
PS_DDR_DQ42
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PS_DDR_DQ44
PS_DDR_DQ45
PS_DDR_DQ46
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PS_DDR_DQ58
PS_DDR_DQ59
PS_DDR_DQ60
PS_DDR_DQ61
PS_DDR_DQ62
PS_DDR_DQ63
PS_DDR_DQ64
PS_DDR_DQ65
PS_DDR_DQ66
PS_DDR_DQ67
PS_DDR_DQ68
PS_DDR_DQ69
PS_DDR_DQ70
PS_DDR_DQ71
PS_DDR_ZQ
VCCIO_PSDDR_504_1
VCCIO_PSDDR_504_2
VCCIO_PSDDR_504_3
VCCIO_PSDDR_504_4
VCCIO_PSDDR_504_5
VCCIO_PSDDR_504_6
VCCIO_PSDDR_504_7
VCCIO2_PS_DDR
UDIMM_PS_ZQ
DDR4_SDRAM0_A0
DDR4_SDRAM0_A1
DDR4_SDRAM0_A2
DDR4_SDRAM0_A3
DDR4_SDRAM0_A4
DDR4_SDRAM0_A5
DDR4_SDRAM0_A6
DDR4_SDRAM0_A7
DDR4_SDRAM0_A8
DDR4_SDRAM0_A9
DDR4_SDRAM0_A10
DDR4_SDRAM0_A11
DDR4_SDRAM0_A12
DDR4_SDRAM0_A13
DDR4_SDRAM0_A14_WE_B
DDR4_SDRAM0_A15_CAS_B
DDR4_SDRAM0_A16_RAS_B
DDR4_SDRAM0_BA0
DDR4_SDRAM0_BA1
DDR4_SDRAM0_ACT_B
DDR4_SDRAM0_ALERT_B
DDR4_SDRAM0_PAR
DDR4_SDRAM0_RESET_B
DDR4_SDRAM0_BG0
DDR4_SDRAM0_CS_B
DDR4_SDRAM0_CK_T
DDR4_SDRAM0_CK_C
DDR4_SDRAM0_CKE
DDR4_SDRAM0_ODT
DDR4_SDRAM0_DQS0_C
DDR4_SDRAM0_DQS0_T
DDR4_SDRAM0_DQS1_C
DDR4_SDRAM0_DQS1_T
DDR4_SDRAM1_DQS0_C
DDR4_SDRAM1_DQS0_T
DDR4_SDRAM1_DQS1_C
DDR4_SDRAM1_DQS1_T
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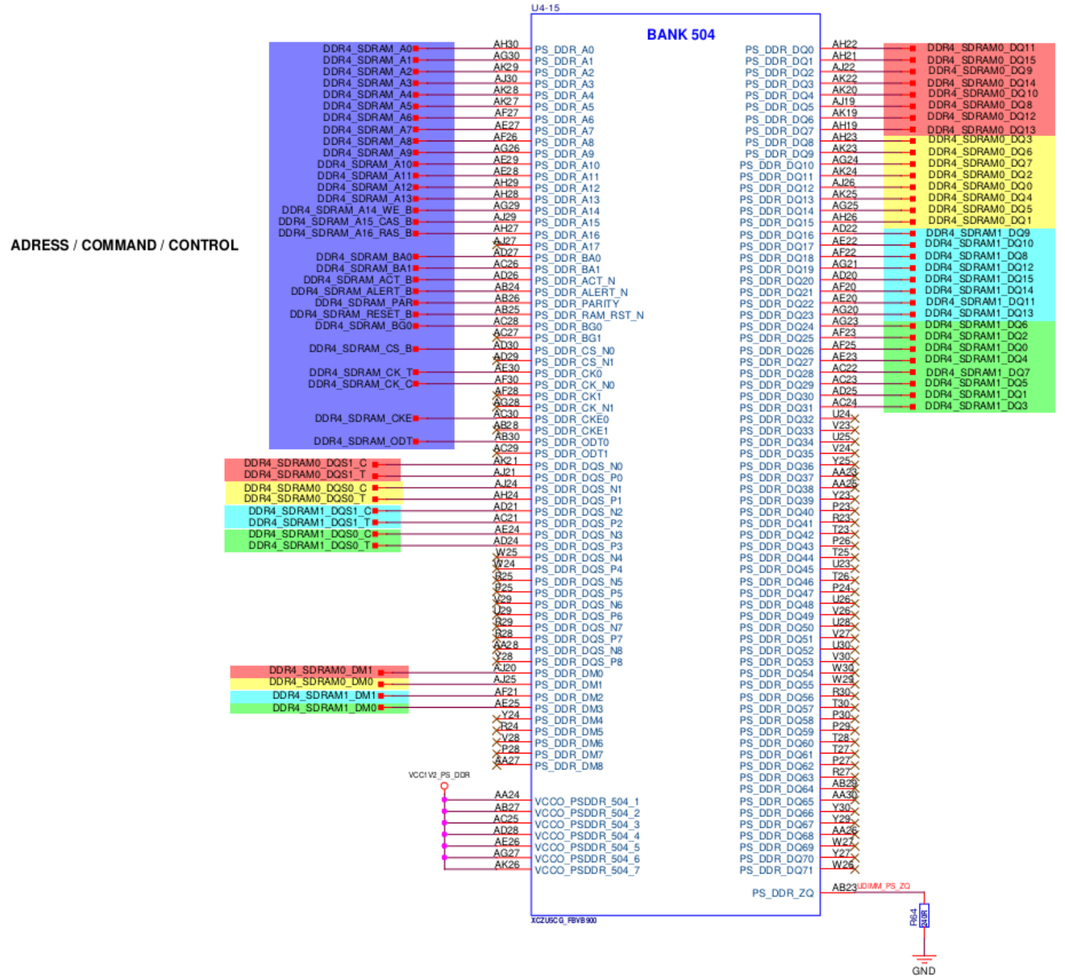
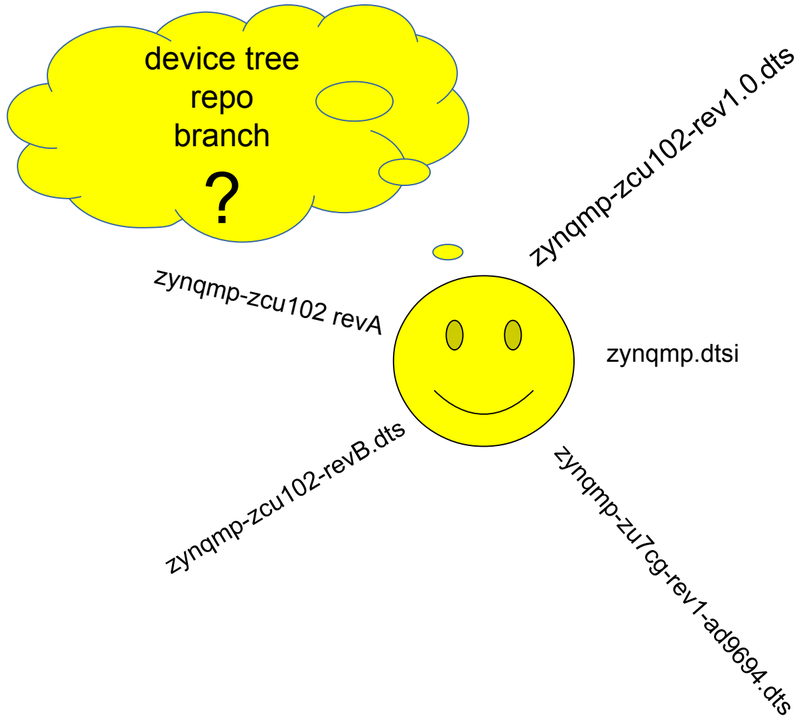
DDR4_SDRAM0_DM1
DDR4_SDRAM1_DM0
DDR4_SDRAM1_DM1
DDR4_SDRAM0_DQ3
DDR4_SDRAM0_DQ2
DDR4_SDRAM0_DQ0
DDR4_SDRAM0_DQ4
DDR4_SDRAM0_DQ1
DDR4_SDRAM0_DQ7
DDR4_SDRAM0_DQ5
DDR4_SDRAM0_DQ6
DDR4_SDRAM0_DQ14
DDR4_SDRAM0_DQ8
DDR4_SDRAM0_DQ11
DDR4_SDRAM0_DQ10
DDR4_SDRAM0_DQ12
DDR4_SDRAM0_DQ15
DDR4_SDRAM0_DQ9
DDR4_SDRAM0_DQ13
DDR4_SDRAM1_DQ7
DDR4_SDRAM1_DQ3
DDR4_SDRAM1_DQ5
DDR4_SDRAM1_DQ6
DDR4_SDRAM1_DQ2
DDR4_SDRAM1_DQ1
DDR4_SDRAM1_DQ4
DDR4_SDRAM1_DQ0
DDR4_SDRAM1_DQ11
DDR4_SDRAM1_DQ8
DDR4_SDRAM1_DQ9
DDR4_SDRAM1_DQ13
DDR4_SDRAM1_DQ10
DDR4_SDRAM1_DQ12
DDR4_SDRAM1_DQ15
DDR4_SDRAM1_DQ14
R64
200R
GND
XCZU5CG_FBVB900


ADRESS / COMMAND / CONTROL
U4-15
BANK 504
BYTELANE 0
SDRAM 0
BYTELANE 1
BYTELANE 0
SDRAM 1
BYTELANE 1
R64
200R
GND
XCZU5CG_FBVB900

Device tree



"Building with Petalinux" from Analog Devices works "out of the box" for standards ADC development boards and a number of FPGA boards. (https://wiki.analog.com/resources/tools-software/linux-build/generic/petalinux)

– The Device Tree Compiler (dtc) is an easy tool to get the details of what is actually built

→ dtc -I dtb images/linux/system.dtb -O dts -o ../devicetree/recompiledDTBs/xxx.dts

– But, where is all this information coming from?

→ user layer from meta-adi-xilinx, meta-adi-core, .../project-spec/meta-user/recipes-bsp/device-tree/files/xxx.dts

– And, if you know where it comes from how to modify this to your own needs?

→ Added custom device tree to the files directory and reference it directly in /meta-adi/meta-adi-xilinx/recipes-bsp/device-tree/device-tree.bbappend

QSPI

Boot from QSPI
– Make sure there is a backup solution available.

– Match the size of the “partitions” to the MTD erase size = 131072 (128K) and set this also in Petalinux

– Uncheck “Use small 4096 B erase sectors” in the kernel config (petalinux-config -c kernel)

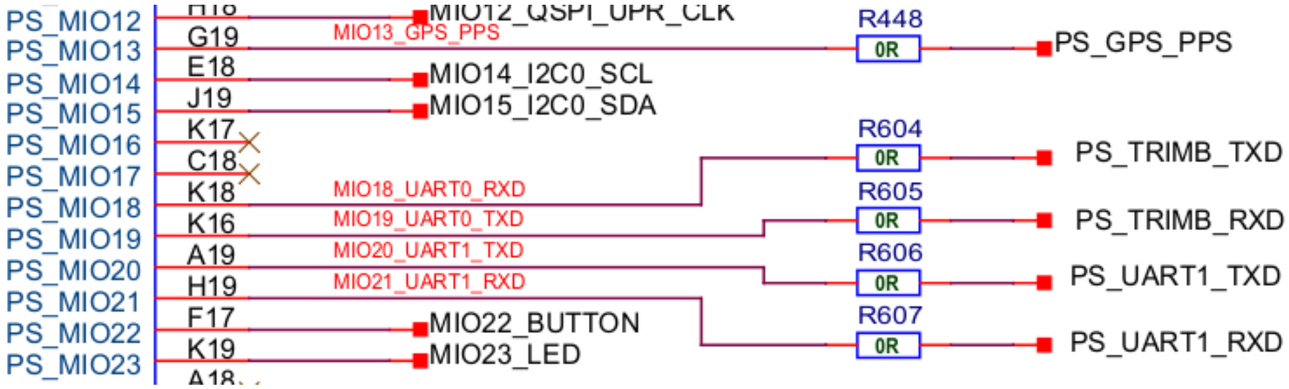
```
&qspi {
    status = "okay";
    is-dual = <1>;
    has-io-mode = <1>;
    /delete-node/ flash@0;
flash@0 {
    compatible = "micron,m25p80", "spi-flash", "n25q512a"; /* dual 512Mb, 1Gb total */
    < – – – snip – – – >

    •partition@boot {
        label = "boot";
        reg = <0x0 0x1e00000>;
    };
    partition@bootenv {
        label = "bootenv";
        reg = <0x1e00000 0x40000>;
    };
    partition@kernel {
        label = "kernel";
        reg = <0x1e40000 0x2400000>;
    };
    partition@jffs2 {
        label = "jffs2";
        reg = <0x4240000 0x2EE0000>;
    };
    partition@spare {
        label = "spare";
        reg = <0x7120000 0x20000>;
};
```

Boot Linux

Set boot arguments in U-boot:
jffs2 boot:
setenv bootargs "console=ttyPS0,115200 earlyprintk
clk_ignore_unused root=mtd:jffs2 rw rootfstype=jffs2"

nfs boot:
setenv bootargs "earlyprintk console=ttyPS0,115200
clk_ignore_unused root=/dev/nfs
nfsroot=192.168.10.1:/srv/nfs,vers=3,nolock,tcp
ip=192.168.10.2:192.168.10.1 rw nfsrootdebug"

– serial interface → never connect the default serial output to the 2nd uart interface on the ZynqMP.



Hardware HDL

Take time to find the best match for the HDL project (PL-firmware), device tree and Linux device drivers (PS-software). The best match depends on the ADC, FPGA, peripherals, clocks and power supplies on the board.

HDL projects:
→ https://github.com/analogdevicesinc/hdl/tree/master/projects

Sometimes the ADC occurs in several ADC hdl projects. It can be beneficial to use a more recent project and accept a mismatch with the used ADC to be able to profit from new (or more flexible) software or firmware.

Start the puzzle here to match the FPGA software version with the HDL release from Analog Devices. Take care, year numbers do not match with FPGA software release! (e.g. release hdl_2019_r1 should be used with Quartus 18.1 or Vivado 2018.3)
→ https://wiki.analog.com/resources/fpga/docs/releases

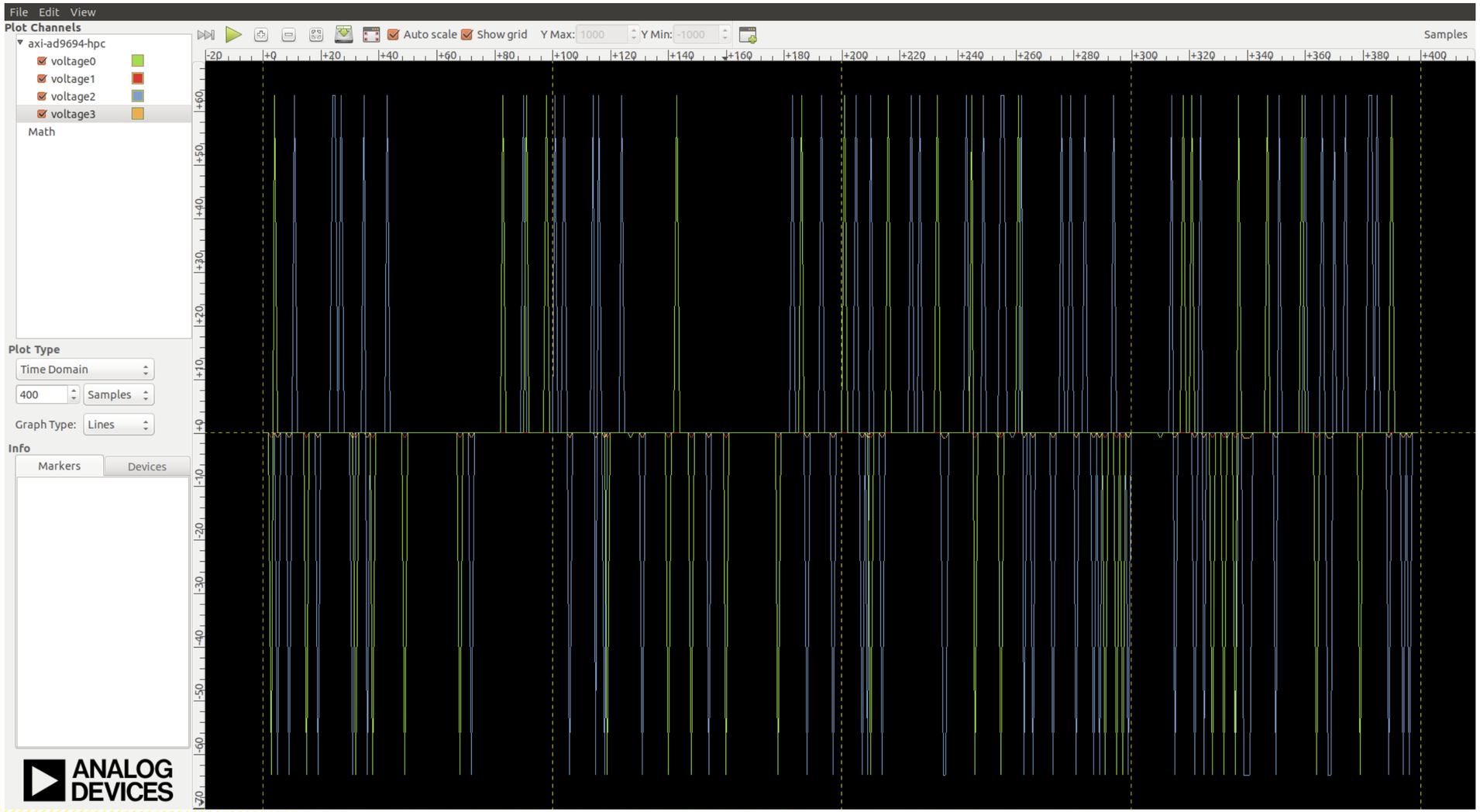
Debug axi busses, hdl, ADC setting and JESD204 lane parameters

Call in help from Analog Devices via EngineerZone forum:
→ https://ez.analog.com/

A lot of information can be subtracted from:
grep "" /sys/bus/platform/devices/*.axi-jesd*/status*
grep "" /sys/bus/platform/devices/*.axi-jesd*/lane*

But before the ADC shows up as an IIO device (iio_info):
– take care of clocking (in the device tree)
– make sure the clock can be reconfigured with a “clk_set_rate” from a device driver.
– enable debug messages in device driver add:
  #define DEBUG
  Before the first include and then rebuild your kernel (with the default log level in the kernel config to print debug messages)

First data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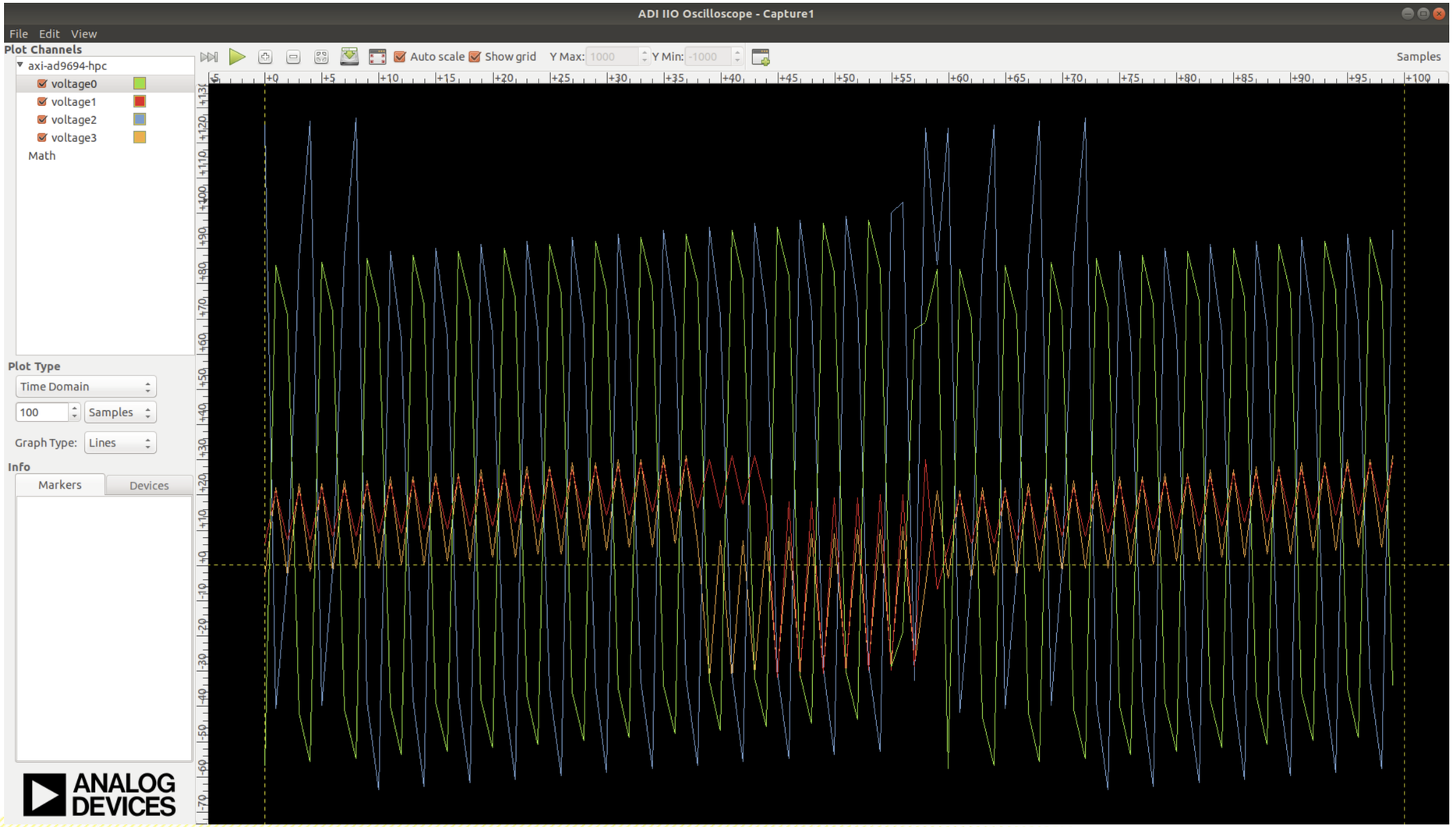
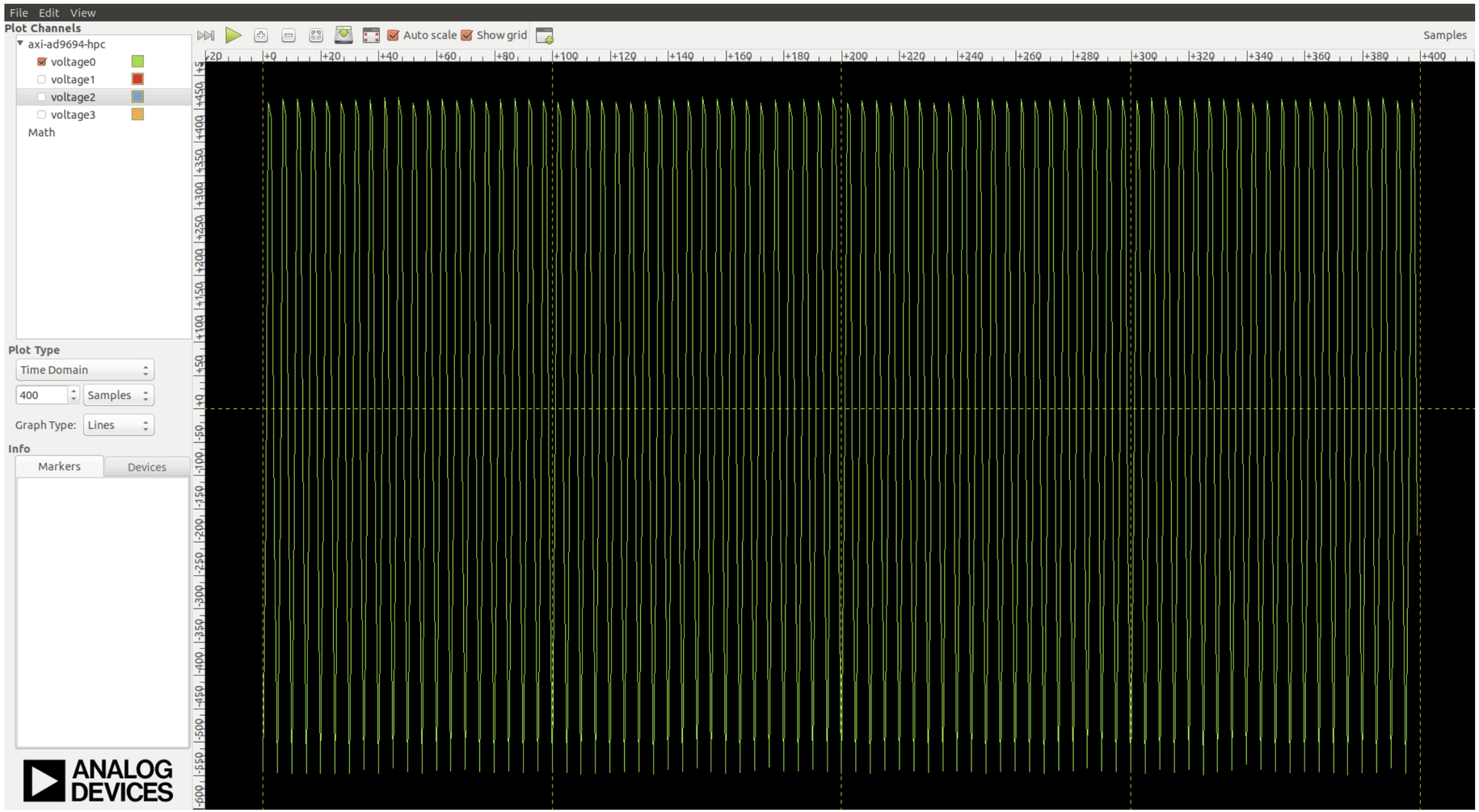
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Auto scale
Show grid
Y Max: 1000
Y Min: -1000
Samples
Plot Type
Time Domain
400
Samples
Graph Type: Lines
Info
Markers
Devices
ANALOG DEVICES

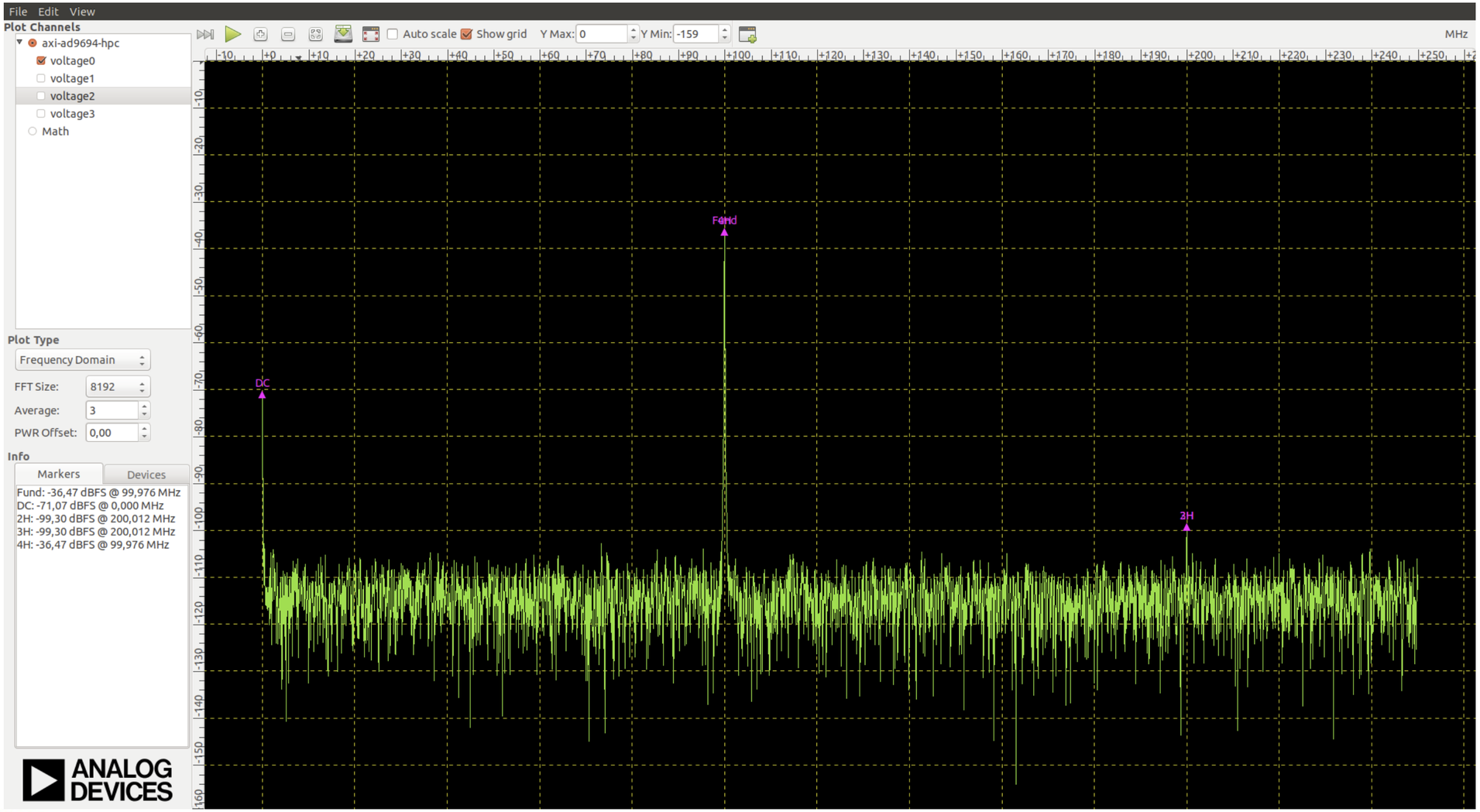
First data


ADI IIO Oscilloscope - Capture1
File Edit View
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Auto scale
Show grid
Y Max: 1000
Y Min: -1000
Samples
Plot Type
Time Domain
100
Samples
Graph Type: Lines
Info
Markers
Devices
ANALOG DEVICES

Results


File Edit View
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Plot Type
Time Domain
400
Samples
Graph Type:
Lines
Info
Markers
Devices
Auto scale
Show grid
Samples
ANALOG DEVICES

Results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Plot Channels
axi-ad9694-hpc
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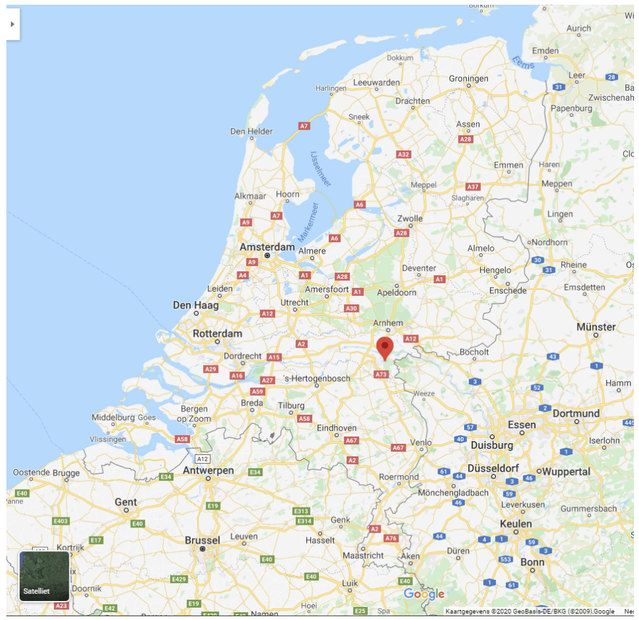
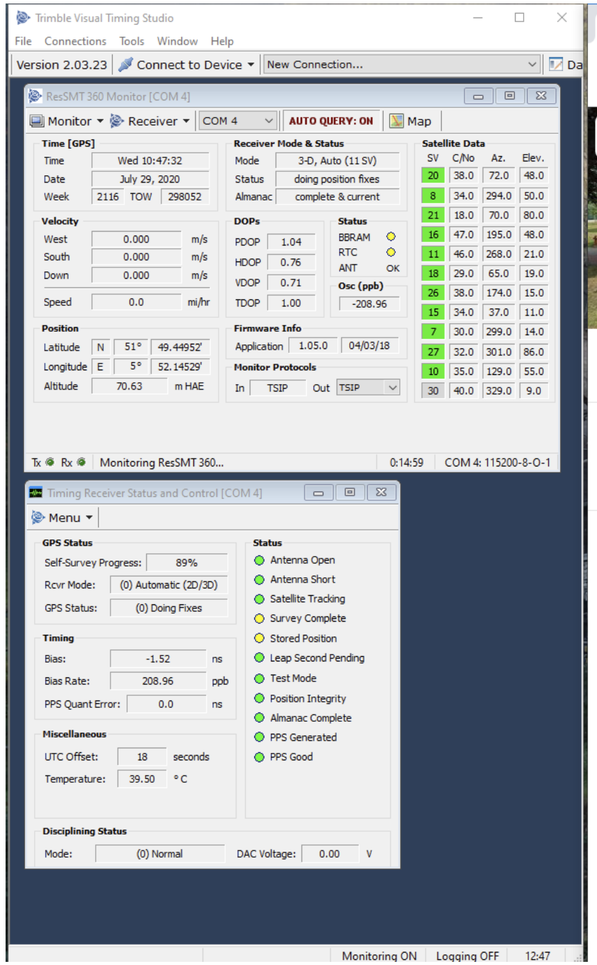
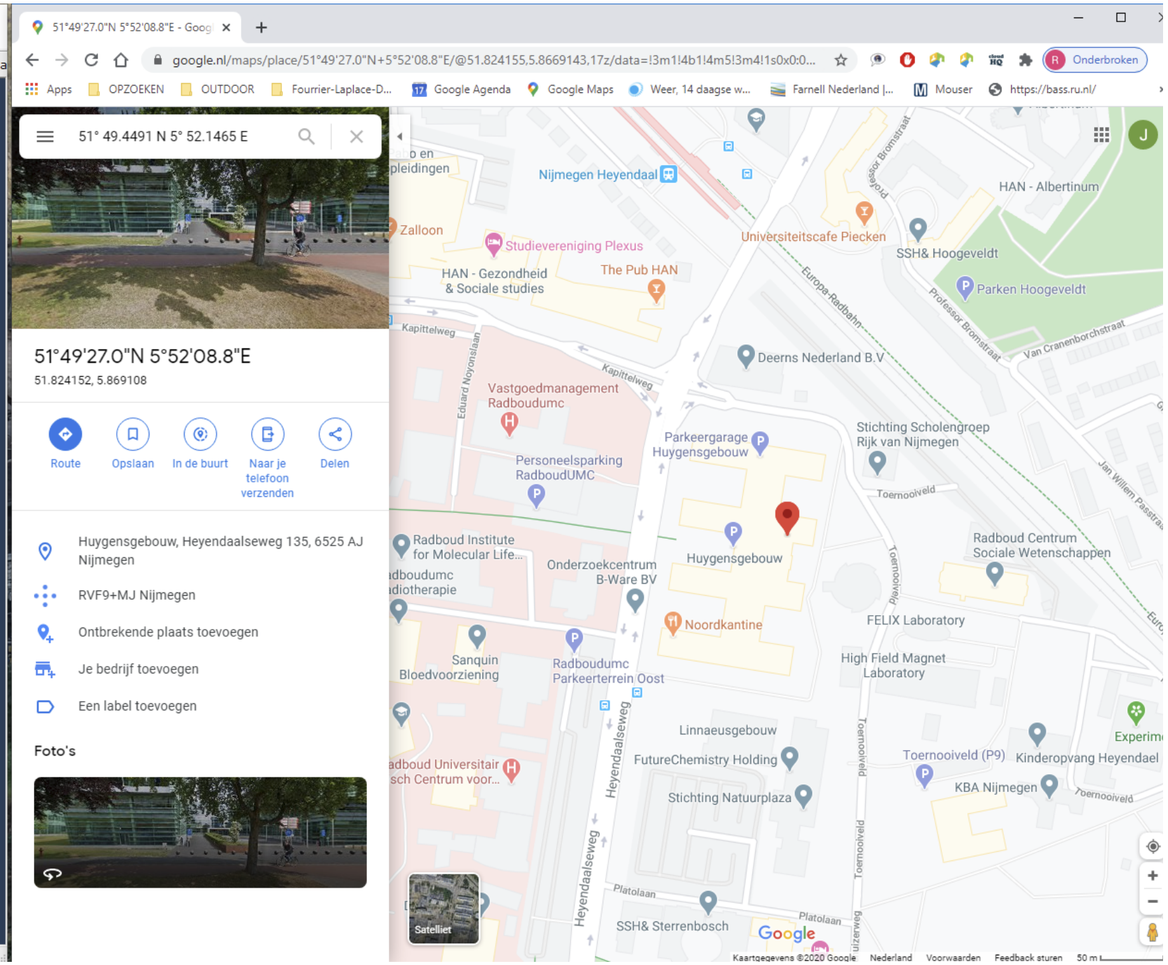
voltage1
voltage2
voltage3
Math
Auto scale
Show grid
Y Max: 0
Y Min: -159
MHz
Plot Type
Frequency Domain
FFT Size: 8192
Average: 3
PWR Offset: 0,00
Info
Markers
Devices
Fund: -36,47 dBFS @ 99,976 MHz
DC: -71,07 dBFS @ 0,000 MHz
2H: -99,30 dBFS @ 200,012 MHz
3H: -99,30 dBFS @ 200,012 MHz
4H: -36,47 dBFS @ 99,976 MHz
DC
3H
ANALOG DEVICES

Results GPS


Amsterdam
Rotterdam
Den Haag
Utrecht
Antwerpen
Gent
Brussel
Eindhoven
Arnhem
Nijmegen
Duisburg
Düsseldorf
Essen
Dortmund
Wuppertal
Bonn
Keulen
Satelliet
Google


Trimble Visual Timing Studio
File Connections Tools Window Help
Version 2.03.23
Connect to Device
New Connection...
ResSMT 360 Monitor [COM 4]
Monitor
Receiver
COM 4
AUTO QUERY: ON
Map
Time [GPS]
Time Wed 10:47:32
Date July 29, 2020
Week 2116 TOW 298052
Velocity
West 0.000 m/s
South 0.000 m/s
Down 0.000 m/s
Speed 0.0 mi/hr
Position
Latitude N 51° 49.44952'
Longitude E 5° 52.14529'
Altitude 70.63 m HAE
Receiver Mode & Status
Mode 3-D, Auto (11 SV)
Status doing position fixes
Almanac complete & current
DOPs
PDOP 1.04
HDOP 0.76
VDOP 0.71
TDOP 1.00
Status
BBRAM
RTC
ANT OK
Osc (ppb)
-208.96
Firmware Info
Application 1.05.0 04/03/18
Monitor Protocols
In TSIP Out TSIP
Satellite Data
SV C/No Az. Elev.
20 38.0 72.0 48.0
8 34.0 294.0 50.0
21 18.0 70.0 80.0
16 47.0 195.0 48.0
11 46.0 268.0 21.0
18 29.0 65.0 19.0
26 38.0 174.0 15.0
15 34.0 37.0 11.0
7 30.0 299.0 14.0
27 32.0 301.0 86.0
10 35.0 129.0 55.0
30 40.0 329.0 9.0
Tx Rx Monitoring ResSMT 360...
0:14:59
COM 4: 115200-8-O-1
Timing Receiver Status and Control [COM 4]
Menu
GPS Status
Self-Survey Progress: 89%
Rcvr Mode: (0) Automatic (2D/3D)
GPS Status: (0) Doing Fixes
Timing
Bias: -1.52 ns
Bias Rate: 208.96 ppb
PPS Quant Error: 0.0 ns
Miscellaneous
UTC Offset: 18 seconds
Temperature: 39.50 °C
Status
Antenna Open
Antenna Short
Satellite Tracking
Survey Complete
Stored Position
Leap Second Pending
Test Mode
Position Integrity
Almanac Complete
PPS Generated
PPS Good
Disciplining Status
Mode: (0) Normal
DAC Voltage: 0.00 V
Monitoring ON
Logging OFF
12:47


51°49'27.0"N 5°52'08.8"E - Goog
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Onderbroken
Apps
OPZOEKEN
OUTDOOR
Fourrier-Laplace-D...
Google Agenda
Google Maps
Weer, 14 daagse w...
Farnell Nederland |...
Mouser
https://bass.ru.nl/
51° 49.4491 N 5° 52.1465 E
51°49'27.0"N 5°52'08.8"E
51.824152, 5.869108
Route
Opslaan
In de buurt
Naar je telefoon verzenden
Delen
Huygensgebouw, Heyendaalseweg 135, 6525 AJ Nijmegen
RVF9+MJ Nijmegen
Ontbrekende plaats toevoegen
Je bedrijf toevoegen
Een label toevoegen
Foto's
Nijmegen Heyendaal
HAN - Albertinum
Zalloon
Studievereniging Plexus
Universiteitscafe Piecken
SSH& Hoogeveldt
HAN - Gezondheid & Sociale studies
The Pub HAN
Parken Hoogeveldt
Deerns Nederland B.V
Vastgoedmanagement Radboudumc
Personeelsparking RadboudUMC
Parkeergarage Huygensgebouw
Stichting Scholengroep Rijk van Nijmegen
Radboud Institute for Molecular Life...
Onderzoekcentrum B-Ware BV
Huygensgebouw
Radboud Centrum Sociale Wetenschappen
Noordkantine
FELIX Laboratory
Sanquin Bloedvoorziening
Radboudumc Parkeerterrein Oost
High Field Magnet Laboratory
Linnaeusgebouw
FutureChemistry Holding
Toernooiveld (P9)
Kinderopvang Heyendael
KBA Nijmegen
Stichting Natuurplaza
SSH& Sterrenbosch
Satelliet
Google
Kaartgegevens ©2020 Google
Nederland
Voorwaarden
Feedback sturen
50 m

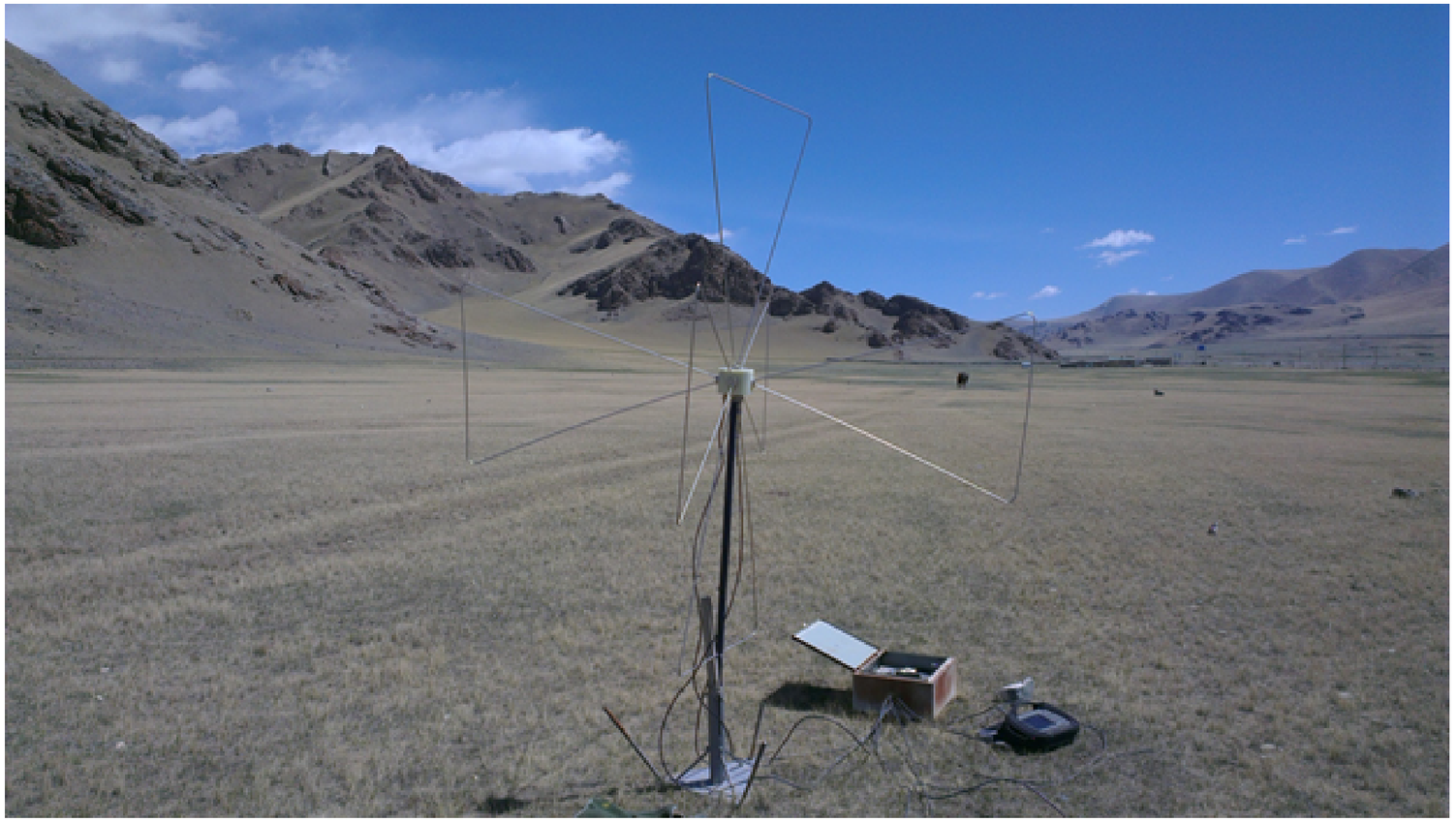
Results

- Testing of first prototype was finished before summer holiday.

- Ready to produce 100 stations using the next iteration of the prototype.

- Next year 100 stations will be installed in remote area in China. Hopefully, 200 more will follow soon after installment

Then there is a lot of work to do to go to 1000, 10.000 and 100.000.



Lessons learned

- It takes a lot of time to debug the boot from QSPI memory. Mainly building and programming the flash.
- Select the Analog Devices HDL project based on available knowledge in you(r team) and on the daq board.
- Learn git, how to make a patch in git and how to apply this patch in Yocto / Petalinux. To be able to add new code you sometimes need a patch…
- Invest time in the development environment especially when booting from QSPI memory. Switch to NFS boot as soon as possible.
- During boot do not reconfigure the clock (chip) that provides the ps_ref_clk. (Thanks Pieter and Ralf :-))
- A clock is not a static signal with a fixed frequency. During boot the device driver of Analog Devices tries several clock settings to be able to set up the JESD204 interface correctly.

- You learn a lot from making your “own” high speed data acquisition board.