LIU-BWS electronics & systems

15.09.2020

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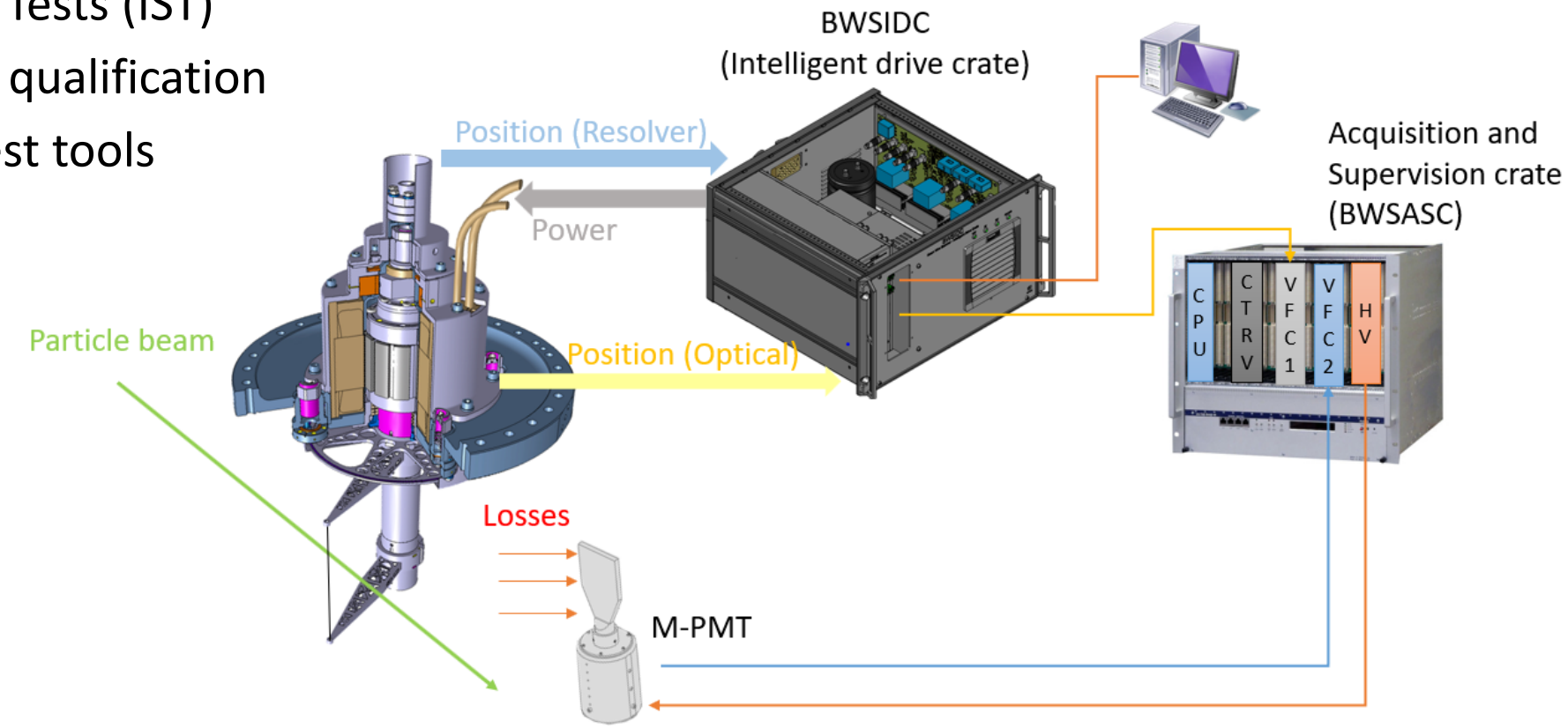
Outlook

1. Installations
2. Individual System Tests (IST)
3. Design status and qualification
4. Production and test tools
5. Firmware



BWS-LIU Installations

- Mechanics ready in PSB and PS, partially missing in the SPS
- PSB tunnel cablings done & tested (Aurelie, Jean, Guillaume, Jose)
- PS On-going tunnel cabling this week (Guillaume, Jose)
- SPS to start next
- Surface installations are waiting for our electronics (IDC drives, MPMT amplifiers, VFC-HD+ADC)

PS installation today (Guillaume/Jose)

BWS-LIU Installations

INSTALLATION STATUS 15.09.2020				TUNNEL					SURFACE				
Machine	position	Orientation	Ring	cables	fibers	mechanism	mpmt	patchbox	idc drive	amp	vfc+adc	ISEG	cabling
PSB	4L1	H	R1	ready					not installed				partial
	4L1	H	R2			not moving							
	4L1	H	R3										
	4L1	H	R4										
	11L1	V	R1										
	11L1	V	R2										
	11L1	V	R3										
	11L1	V	R4										
PS	54	H		ready		not tested	sig. cables	not installed					
	64	V					missing						
	65	H											
	68	H											
	85	V											
SPS	41677	V		ready	not installed								
	41678	V											
	51638	H											
	51639	H											

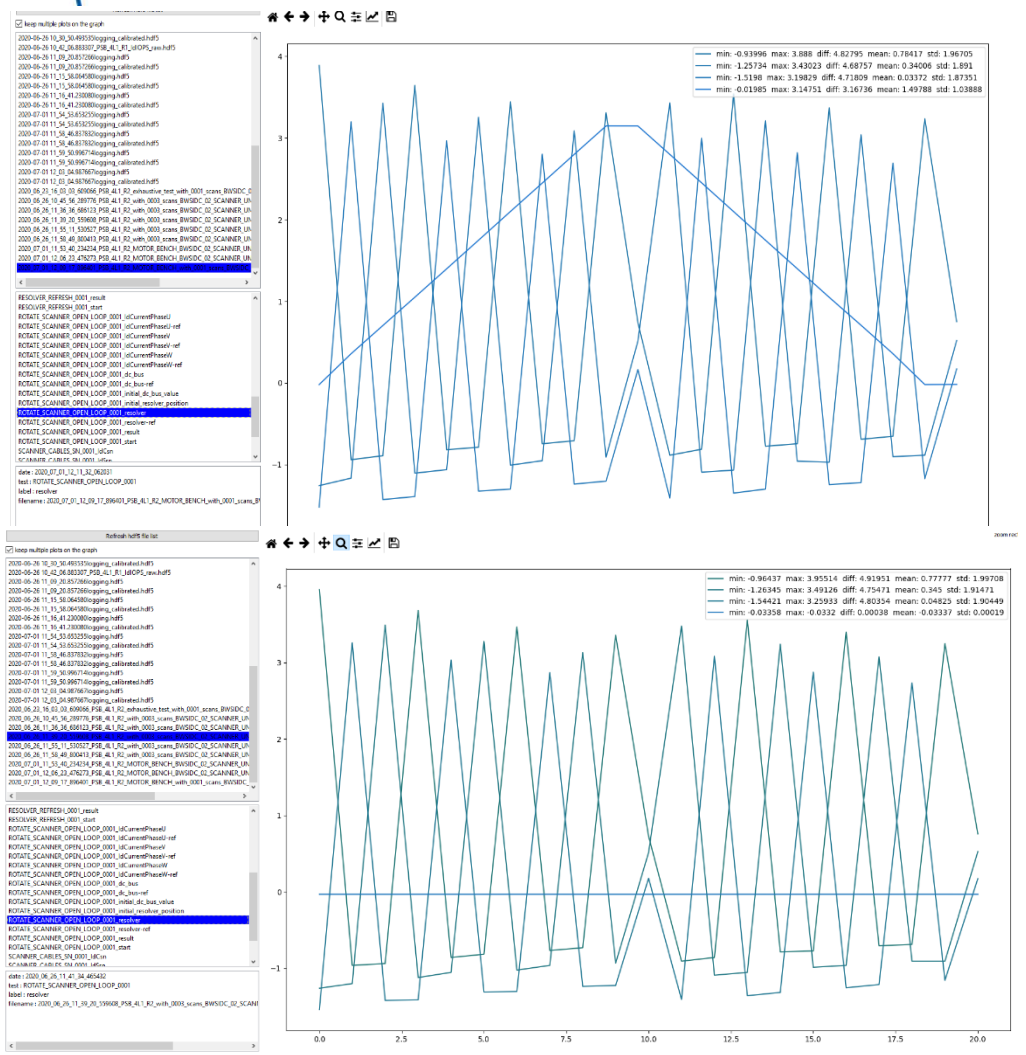
BWS-LIU Individual System Test

- New system able to discover issues of resolver, motor or cabling without need of dummy scanner in the tunnel (OPEN LOOP TEST).
- Test procedure for the drive related function automatized.
  Includes open loop tests, scans, wire check, etc.
  Uses python scripts (library for the IDC), eventually part will be integrated to FW
- PSB 7 out of 8 mechanism operated at nominal speed (20m/s) using the same IDC controller with local link (python).
- One scanner mechanism to be exchanged
- PSB Acquisition installation successfully tested manually by Aurelie/Guillaume
- Acquisition test will be automatized ones we have full system installed (MPMT amplifier + VFC-HD + ADC)

BWS-LIU Individual System Test

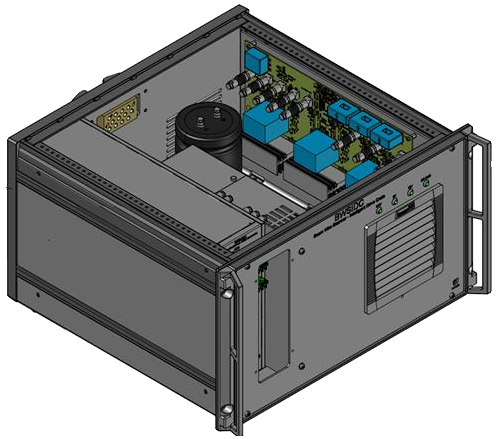
Individual System Tests	position	Orientation	Ring	Asset Mechanism Asset Mechanism deduced from the electronics SN (from the surface)	Electronic SN (ESN)	ESN decoded	cables electronic check	control patchcord install	Dummy scanner test	open loop rotation	scans @140 rad/s	Optical encoder	wire check	MPMT assembly	patch cords HV+SIG	MPMT surface test
PSB	4L1	H	R1	PXBWSRA005-CR000010	74	PSB_0_10	9				6		to check			
	4L1	H	R2	PXBWSRA005-CR000007	71	PSB_0_07	9			can't move	-		to check			
	4L1	H	R3	PXBWSRA005-CR000008	72	PSB_0_08	9				4		to check			
	4L1	H	R4	PXBWSRA005-CR000005	69	PSB_0_05	9				10		to check			
	11L1	V	R1	PXBWSRA005-CR000004	68	PSB_0_04	9				18		to check			
	11L1	V	R2	PXBWSRA005-CR000009	73	PSB_0_09	9				14		to check			
	11L1	V	R3	PXBWSRA005-CR000006	70	PSB_0_06	9				13		to check			
	11L1	V	R4	PXBWSRA005-CR000003	67	PSB_0_03	9				13		to check			
PS	54	H														
	64	V														
	65	H														
	68	H														
	85	V														
SPS	41677	V														
	41678	V														
	51638	H														
	51639	H														

Individual system tests (IST) PS Booster – 4L1-R2

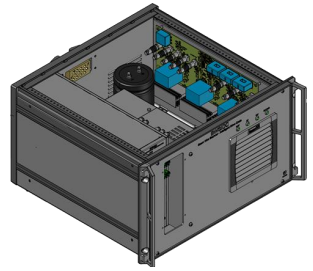


Hardware design and qualification - Control

- Power boards issues (Jan-Feb 2020) fixed and pre-production corrected
  Thanks to Miguel, Ervin and Guillaume to solve this issue
- IDC drive extensive validation performed during confinement
  24 April – 22 June – more than 13’000 scans with various temperature 23-55 [◦C]
- Final designs modifications & go-ahead PCB production (June 2020)
- Go-ahead PCB assemblies (July 2020) after additional tests



Intelligent Drive Crate (IDC) architecture



Analog Interfaces FMC (BWS-AIF)

Feb. 2019

Motor Inverter Board (BWS-MIB)

Feb. 2020

Capacitor Power Charger (BWS-CPC)

VFC-HD

SPI ‘robust’

Gate ctrl

Analog I - Ubus

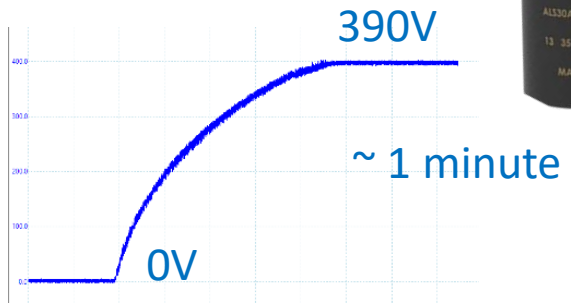
400V – 16mF

Resolver/C-wire

Optical encoder

3 phases

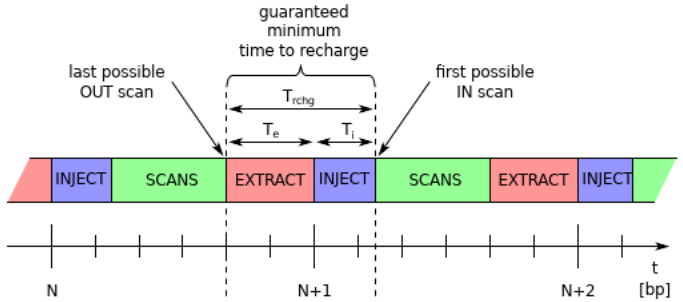
~400V - 60 Amps

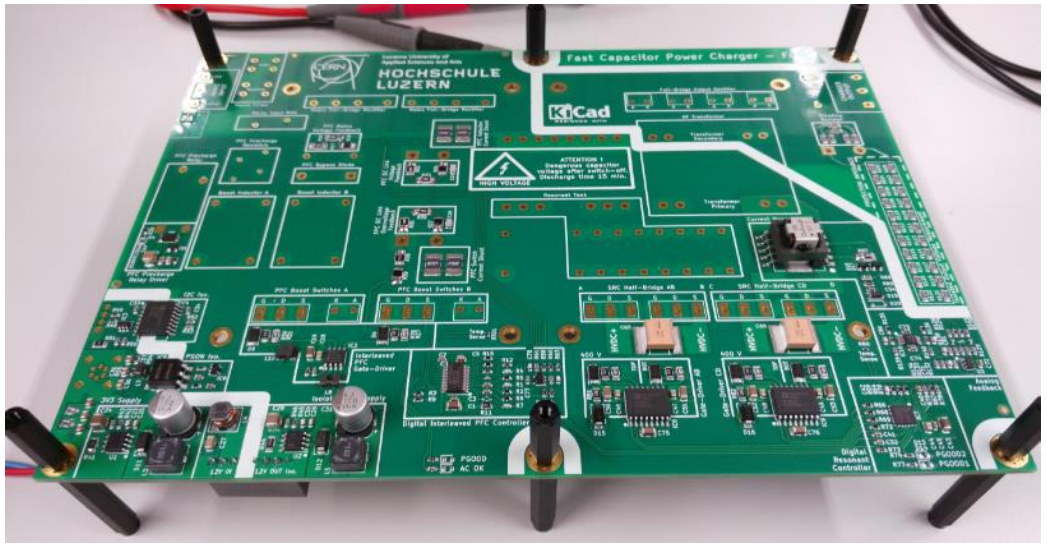


Hardware design and qualification - Control

- Redesign of the charger for future upgrade by (E. Mazlagic - Tech. Student mostly TW)
- Solution to increase repeatability rate
- "**Fast Capacity Power Charger**" using an efficient power stage topology
- Designed to replace existing charger (same mechanical and electrical interfaces)
- Prototype under test at Tech. University of Lucerne (CH)
- Plan to test inside an IDC drive at CERN before end of February 2021 (end of Master thesis)

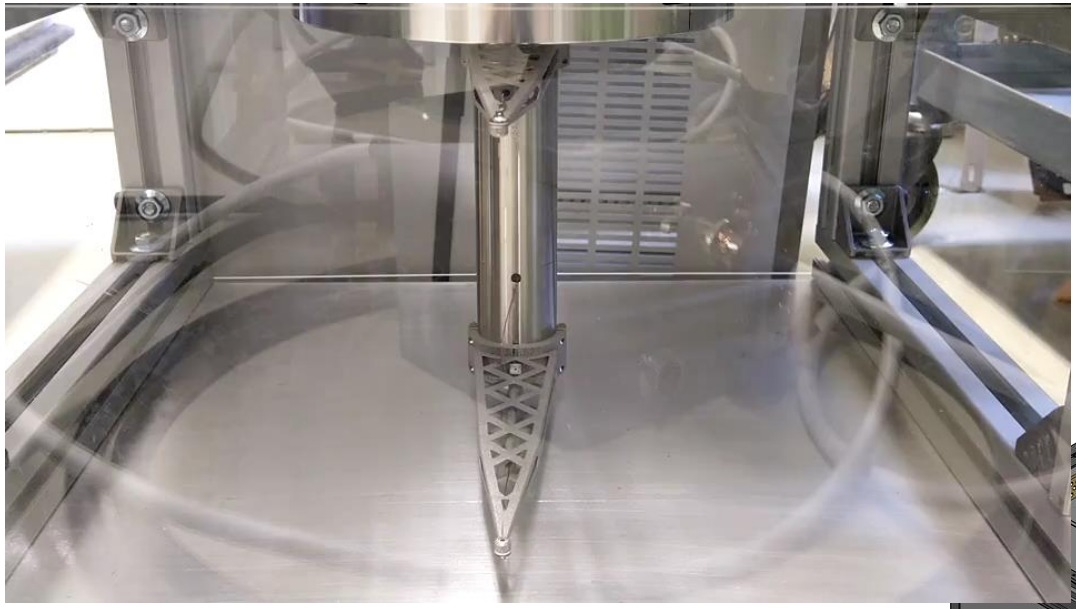
slot		value	unit
basic period	T_{bp}	1'200	ms
injection	T_i	275	ms
scan	T_s	670	ms
extraction	T_e	395	ms
recharge	T_{rchg}	670	ms

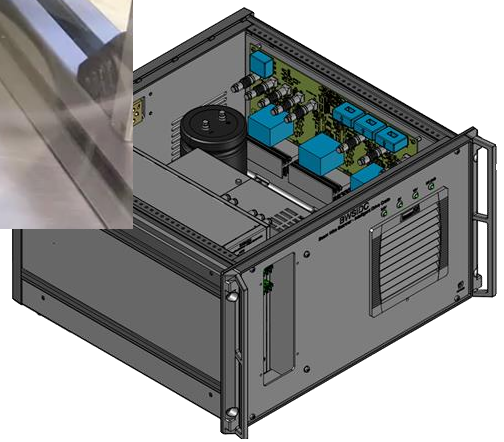




Hardware design and qualification - Control

- IDC drive extensive validation performed at CERN during lockdown
  24 April – 22 June – more than 13’000 scans at various temperature 23-55 [◦C]



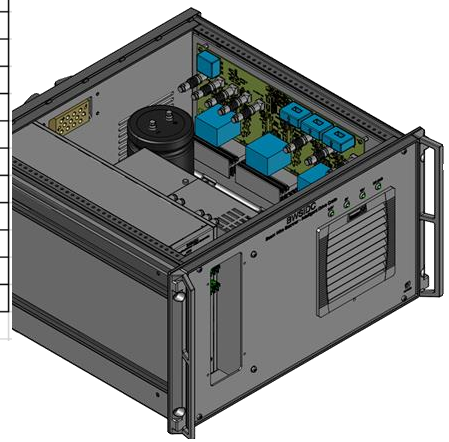


IDC drive inside the climatic chamber at top temperature of 55 [◦C], cables of 120 [m] and high repetition rate of 5 scans at 20 [m/s] every ~15s.

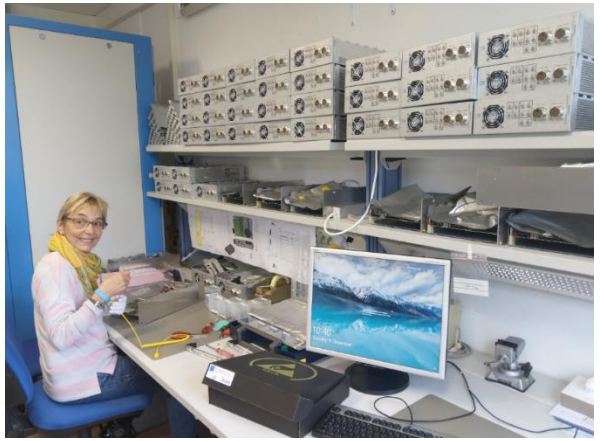
Hardware design and qualification - Control

- IDC drive extensive validation performed during lockdown
  24 April – 22 June – more than 13’000 scans at temperature between 23-55 [◦C]

date	location	SN IDC	SN scanner	duration (h)	temperature	scan per cycle	cycle duration	nbr cycles	nbr scans	charge-discharge cycles	remarques
7.05		IDC_01	ESS-CR014	2.113194444	25	1	8.5	895	895		
7.05		IDC_01	ESS-CR014	1.43	25	2	13	396	792		
8.05		IDC_01	ESS-CR014	1.843333333	25	3	14	474	1422		
8.05		IDC_01	ESS-CR014	0.237222222	25	3	14	61	183		
12.05		IDC_01	ESS-CR014	0.263888889	30	3	10	95	285		
12.05		IDC_01	ESS-CR014	0.91	40	5	12	273	1365		
13.05		IDC_01	ESS-CR014	0.725833333	40	5	13	201	1005		
13.05		IDC_01	ESS-CR014	1.216944444	50	5	13	337	1685		
14.05		IDC_01	ESS-CR014	1.144722222	55	5	13	317	1585		
15.05		IDC_01	ESS-CR014	2	55					50	
19.05		IDC_02	ESS-CR013	0.666	25					14	
20.05		IDC_02	ESS-CR013		25	1	6.5	29	29		
22.05		IDC_02	ESS-CR013	0.28	23	3	10.3	101	303		top speed reach 150 rad/s!
27.05	ClimCham	IDC_01	ESS-CR014		23	1	15s	202	202		
27.05	Wslab	IDC_02	ESS-CR013		23	1	15s	200	200		
28.05	Wslab	IDC_02	ESS-CR012		23	1	15s	175	175		rwire=4,27kOhm / isolation=open
29.05	Wslab	IDC_02	ESS-CR012		23	1	15s	330	330		rwire=4,27kOhm / isolation=open
3.06	Wslab	IDC_02	ESS-CR012	0.5	23	1	9	211	211		wire and isolation ok
3.06	Wslab	IDC_02	ESS-CR012	2.1	23	3	15	551	1653		wire and isolation fault
4.06	Wslab	IDC_02	ESS-CR011		23	3		104	312		wire and isolation after 1 scan
12.06	Wslab	IDC_02	ESS-CR011		23	1		80	80		full automated scripts / tests data into same hdf5 file
15.06	ClimCham	IDC_02	ESS-CR010		40	3	9	130	390		100m cable, use gui, DC_BUS stable at around 310V
17.06	ClimCham	IDC_02	ESS-CR010		55	1		100	100		100m cable, script, minimal data taking
17.06	ClimCham	IDC_02	ESS-CR010		55	1		10	10		100m cable, script, minimal data taking, better IOPS settings
22.06	867	IDC_01	ESS-CR009		25	1		20	20		220m cables, script, Gain current = 6 (was2), minimal data, noisy
22.06	867	IDC_01	ESS-CR009		25	1		20	20		220m cables, script, Gain current = 3 (was2), good behaviour, IOPS noise
total								5292	13232		



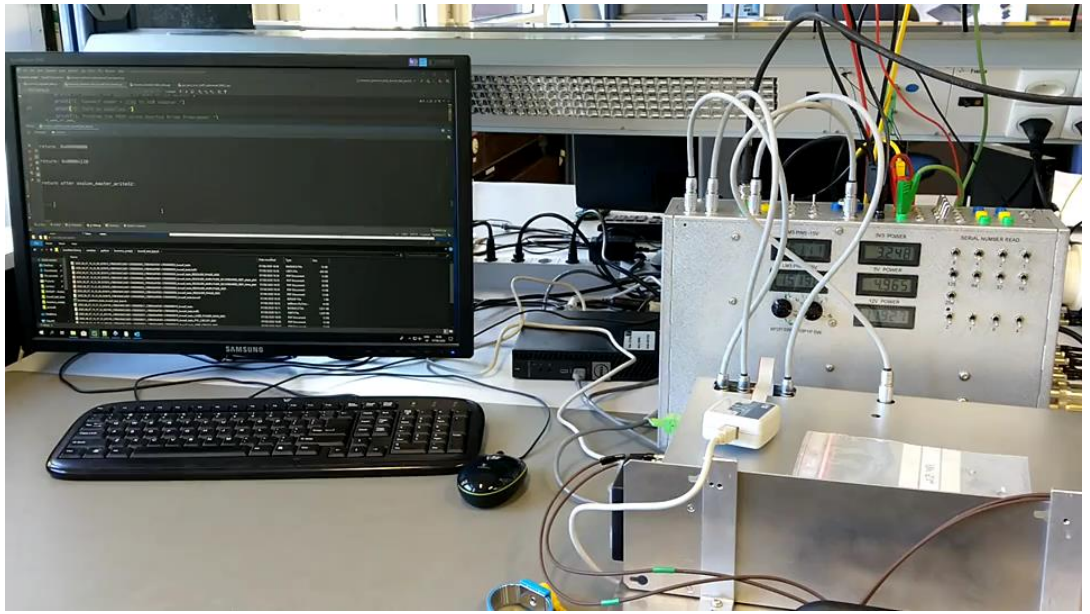
Production and test tools - Control



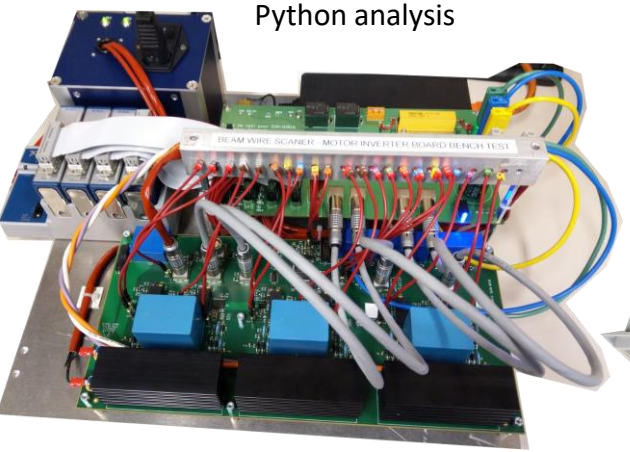
- Production & Test lab ready for the series before lock-down Christiane, Guillaume, Georges and Thasos (BL Greek team).
- Help from Miguel and Jose during the lock-down. Christiane back mid-June.
- 10 pcs pre-series done
- 27 pcs series assembly finished waiting for the electronics board
- Expecting start boards testing on the 21 September

Production and test tools - Control

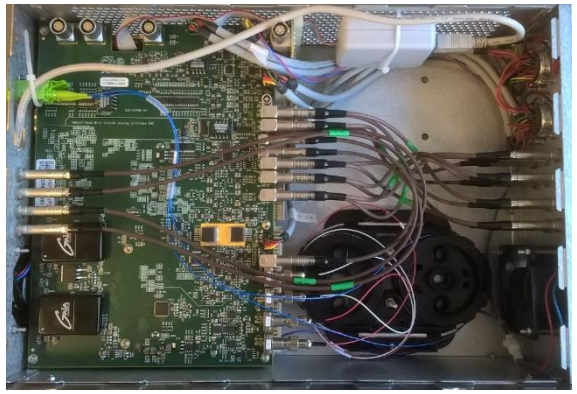
- Test bench for all boards, automated for the most complex
- Same scripts family used for the complete drive BWSIDC
- Enormous reduction in testing time at the cost of more developments
- Step 1: Resistive measurements & excel report
- Step 2: Automated tests & report generation per board
- Step 3: Data analysis of all boards results at ones



BWSMIB bench
(Jean/Guillaume/Jonathan)
Labview controlled
Python analysis



BWSIDC automated functional bench with scanner (Jonathan)
Python based script using JTAG
(soon IP-BUS)



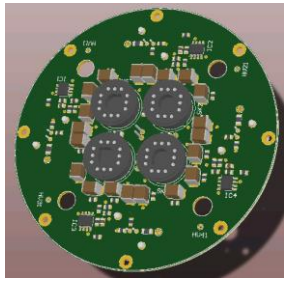
BWSAIF (Motor inverter) bench
(Guillaume/Jonathan)
Python based script using JTAG
(soon to be migrated to IP-BUS)

Design and validation - Hardware Acquisition

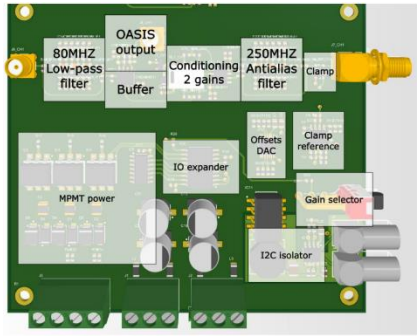
- MPMT assembly - Scintillator - PMT/PCB board:
  - Assembled and lab validated with laser source (Aurelie & BI-ML)
  - Series assembled for PSB and PS

- MPMT amplifier:
  - kick-off meeting 7 April (Miguel)
  - design review 5 June by William Vigano and al.
  - PCB version 2 tested & first crate assembled
  - Design drawing (electronics and mechanics) ready
  - Production will be handled by TE-MPE (to be started)

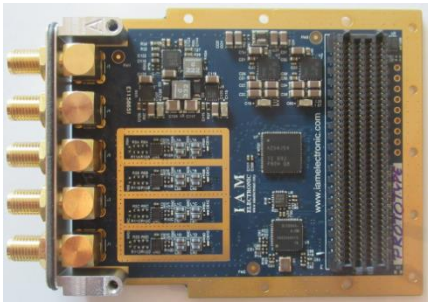
- Fast ADC module:
  - validation and go-ahead for production end of February (David)
  - First batch of 30pcs received beginning of June
  - all pieces tested (Jose & David) results under analysis (Federico)
  - Next batch to be launched soon



MPMT board for 4 PMT
EDA-03764



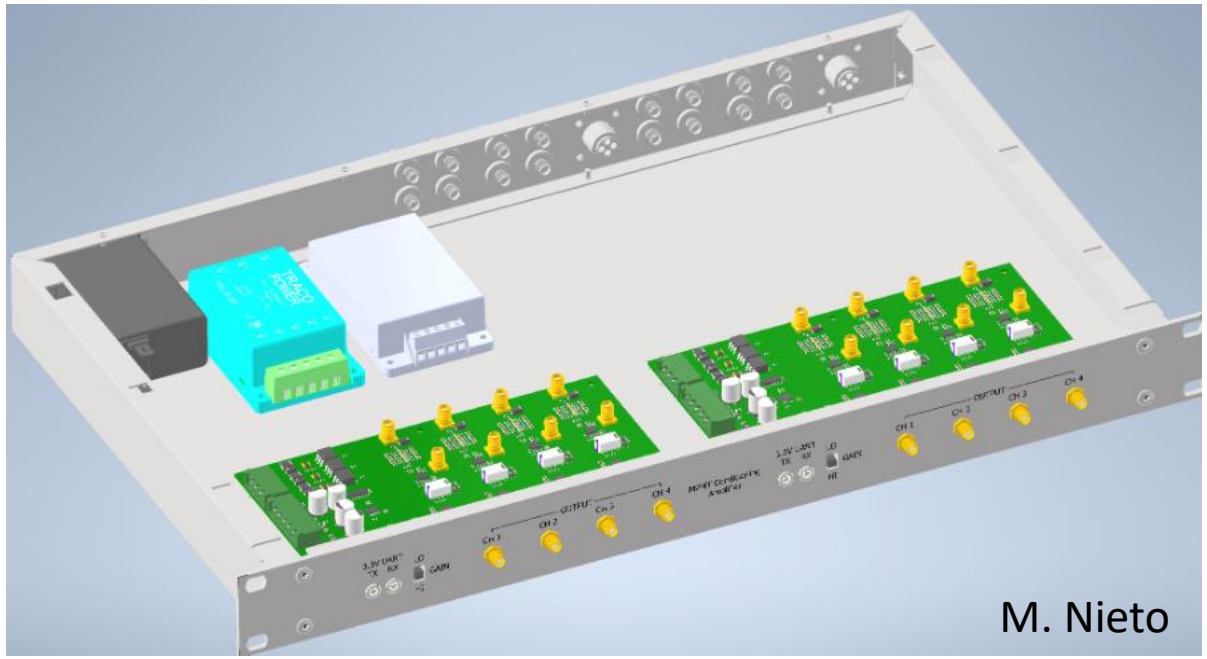
MPMT amplifier
EDA-xxxxxx

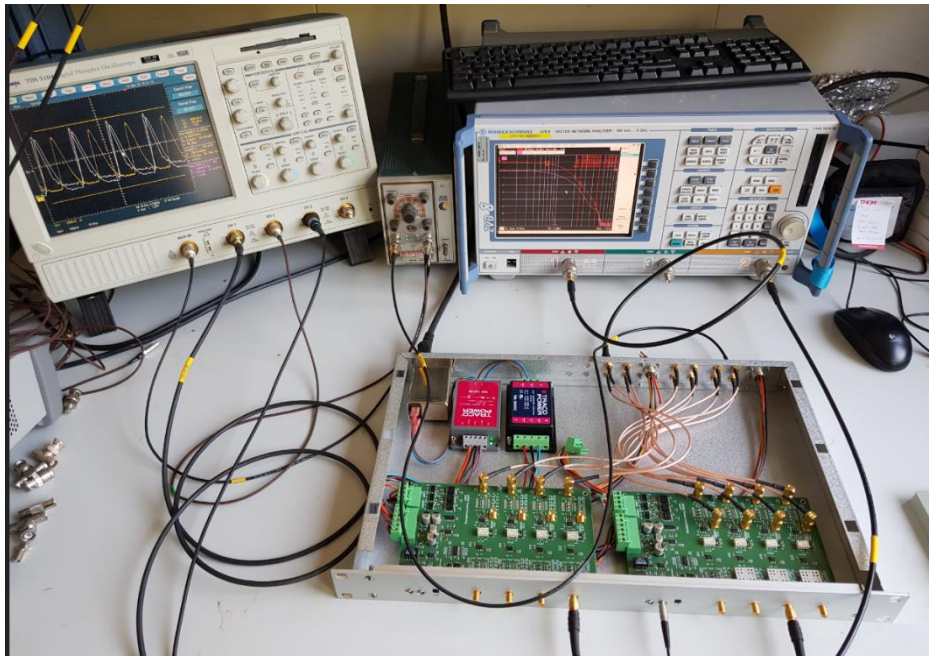


Commercial ADC 4x500MHz
14bits by I.A.M. Electronics

Design and validation - Hardware Acquisition

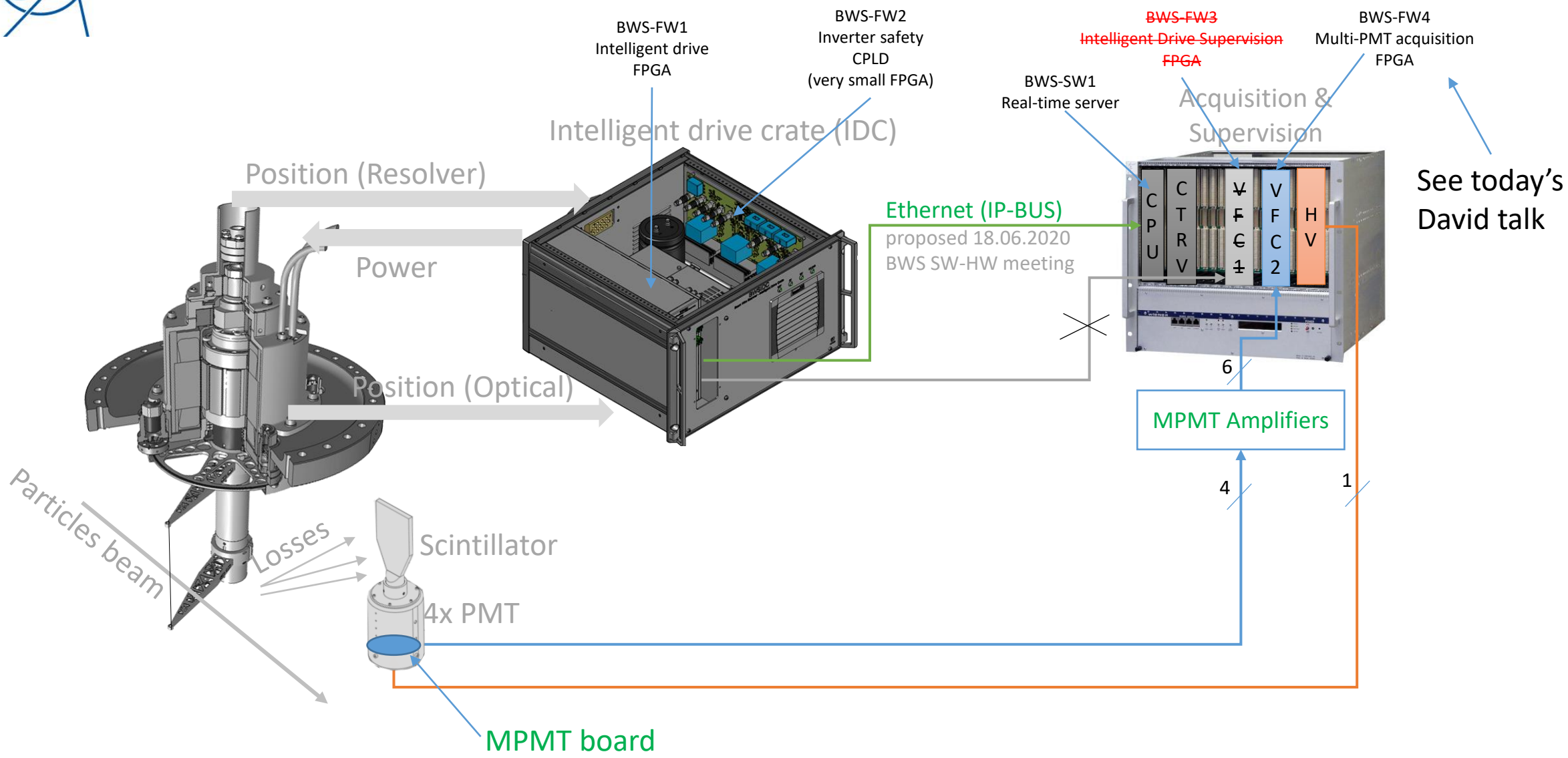
- MPMT amplifier:
  - Design drawing (electronics and mechanics) ready





Test setup of the MPMT amplifier V2

Firmware


BWS-FW1
Intelligent drive
FPGA
BWS-FW2
Inverter safety
CPLD
(very small FPGA)
~~BWS-FW3~~
~~Intelligent Drive Supervision~~
~~FPGA~~
BWS-FW4
Multi-PMT acquisition
FPGA
BWS-SW1
Real-time server
Acquisition &
Supervision
Intelligent drive crate (IDC)
Position (Resolver)
Power
Position (Optical)
Ethernet (IP-BUS)
proposed 18.06.2020
BWS SW-HW meeting
CPU
CTRV
~~VFC1~~
VFC2
HV
6
MPMT Amplifiers
4
1
See today's
David talk
Particles beam
Losses
Scintillator
4x PMT
MPMT board

Firmware status

- BWS-FW1 Intelligent drive FPGA
  Optical encoder pre-processing + timing closure optimization (done during lockdown)
  IP-BUS link to the CPU (ready since last week)
  Movement sequencer (working on it)
  Multi-speeds (next)
  DDR memory integration (future)

- BWS-FW2 Inverter safety CPLD (very small FPGA)
  Operational on V2 boards being produced now
  Good for operation at nominal speed

- BWS-FW3 Intelligent Drive Supervision FPGA
  Not needed anymore in the new architecture

- BWS-FW4 Multi-PMT acquisition FPGA
  See David's presentation

Firmware – BWS-FW1 - IP-BUS link to SW

- Now integrates IP-BUS link
- Board answering to ping (1st September)
- 1Gigabit copper link
- IP address generated from unique number of the VFC-HD board
- Low level python driver written (python) for simple read and write transactions
- Python DevExpert app migrated

- Successful control of 4 IDC drive in the PSB connected to the same Ethernet switch (using DevExpert app)
- Setup ready in the lab with MEN-A25 and Ethernet mezzanine for SW to start testing it.

Read chronogram of 64 words of 32bits with IP-BUS

(current implementation that can be optimized)

takes ~128 to be received + 256 clk to transfer from Avalon to IP-BUS then, unit 576 to be completely sent to the Ethernet mac => 704 clk for 64 (32bits)*4 bytes => 704 for 256bytes.

256/0.0000176 => ~14.5Mbyte/s (without CPU/driver induced delays)

Firmware – BWS-FW1 - IP-BUS link to SW

IPbus User's guide Developer's guide Admin (restricted)

Software and firmware that provide a reliable high-performance control link for particle physics electronics, by implementing a simple A32/D32 control protocol for reading and modifying memory-mapped resources within FPGA-based hardware devices.

Introduction to IPbus | User's guide

Firmware

Repository (GitHub): ipbus/ipbus-firmware
Version: v1.8

Latest updates:

- Firmware v1.8 released
  Thu, 30 Apr, 2020
- Firmware v1.7 released
  Mon, 3 Feb, 2020
- Firmware v1.6 released
  Tue, 22 Oct, 2019

Software

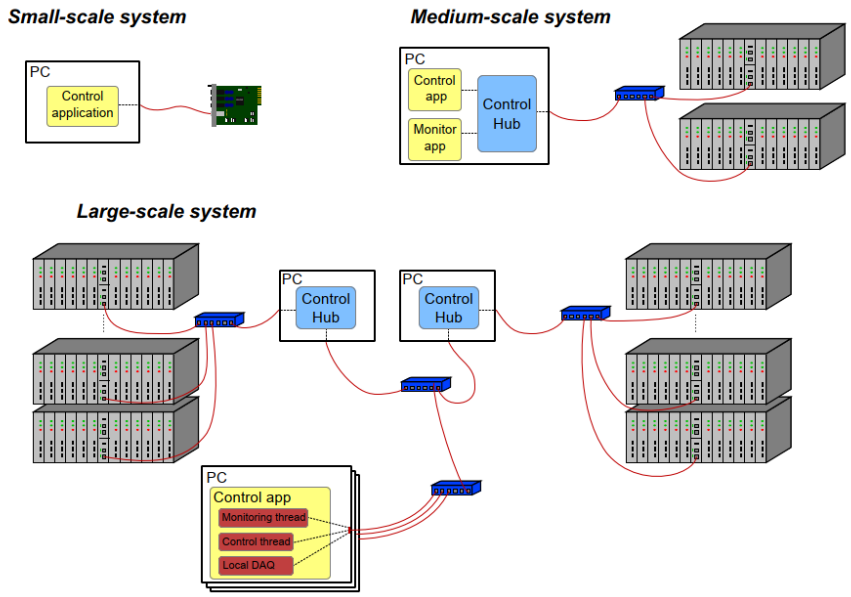
Repository (GitHub): ipbus/ipbus-software
Version: v2.7.5

Latest updates:

- Software v2.7.5 released
  Thu, 11 Jun, 2020
- Software v2.7.4 released
  Fri, 15 May, 2020
- Software v2.7.3 released
  Sat, 21 Mar, 2020

Publication

*C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea and T. Williams, "IPbus: a flexible Ethernet-based control system for xTCA hardware", JINST **10** (2015) no.02, C02019.* DOI: `10.1088/1748-0221/10/02/C02019`



1-to-1 block transfers. The block read/write latency and throughput for one μHAL client controlling one device via the ControlHub is shown in figure 2. The median single-word write/read latency is approximately 250 μs. Although this single-word latency is significantly larger than with VME/PCIe-based control, for multiple transactions or large block transfers this is compensated by concatenating multiple transactions into each packet, and by having multiple packets in flight around the system at any given time. Together, concatenation and multiple packets in flight increase throughput by a factor of approximately 20 to 2000, depending on transaction type. Hence, the 1-to-1 block read/write throughput for payloads larger than 1 MByte is above 0.5 Gbit/s.

http://ipbus.web.cern.ch/ipbus/

Firmware – Control – scan sequencer

- Implementation on-going of the scan sequencer to hide low level HW control from the SW
- Handling of the power stage of the electronics
- Generation of signal synchro for the acquisition electronics
- Time stamping scanner events for the SW

Additional slides

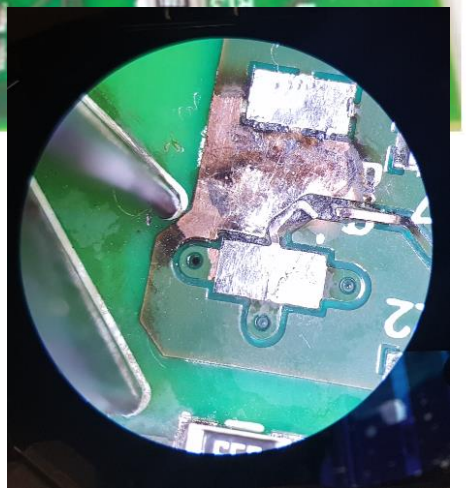
Boards status
BWSCPC – V4 issue – Feb. 2020

Problem:

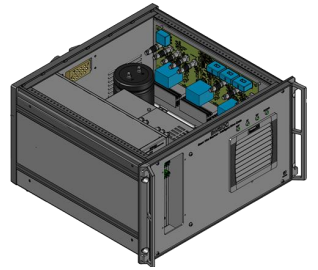
- Systematic components burning (at least 6 times)
  Flyback shunt, MOSFET and driver
- Happens after few seconds of operation
- Only when controlled by BWS-MIB

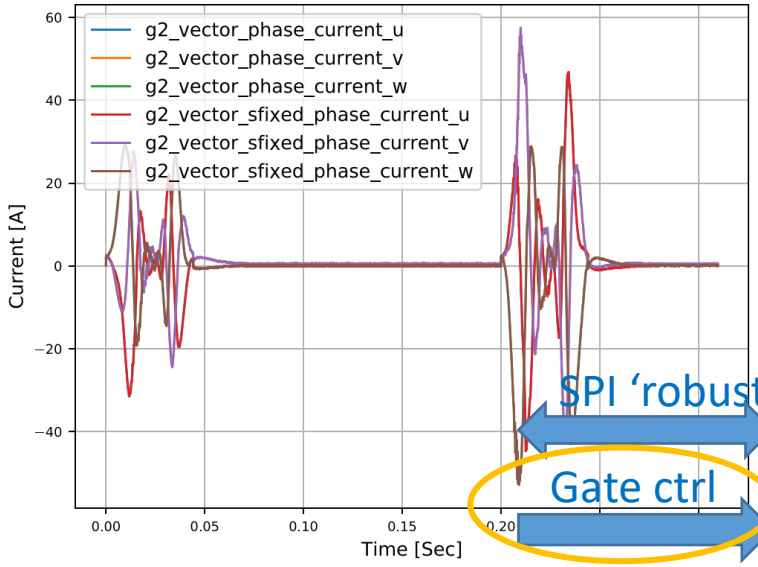
Actions:

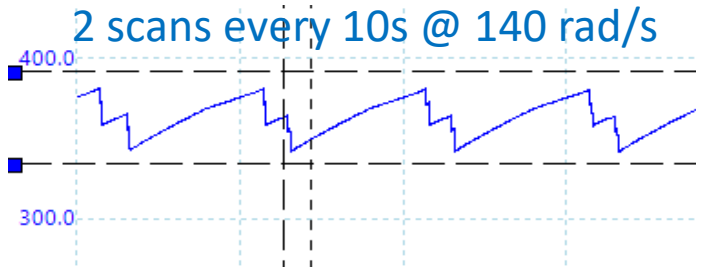
- CPC design dimensioning re-checked
- MOSFET switching characteristics extensively measured
- Multiples board modifications tested:
  - Better grounding – large ground bounces
  - Increasing shunt resistor – lowering charge current
  - Gate resistor to slow down - MOSFET slew rate
- Suspecting EMI inducing instabilities on the control signals
- Sum of design flaws are leads to this situation

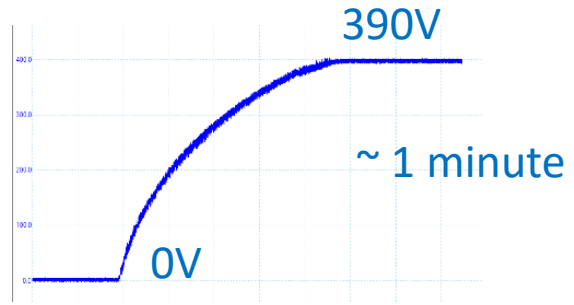


Power parts
BWS-IDC actuation power architecture









Motor Inverter Board (BWS-MIB)

Capacitor Power Charger (BWS-CPC)

SPI 'robust'

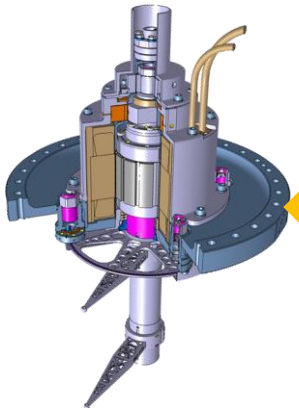
Gate ctrl

Analog
I - Ubus

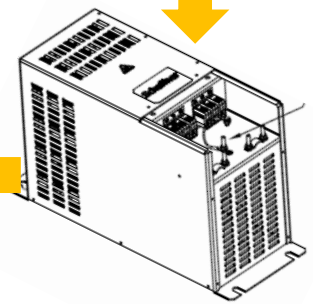
Ctrl lines

Opto-isolated
digital ON/OFF

Main AC
~230V



3 phases
~300V - 60 Amps



LC
Output
filter

390V DC-BUS

450V
16mF