







## **DESY Testbeam Results and More:**

Timing Measurements, ATLASpix Rotations, New Sensors

CLICdp Collaboration Meeting CERN, October 1st, 2020

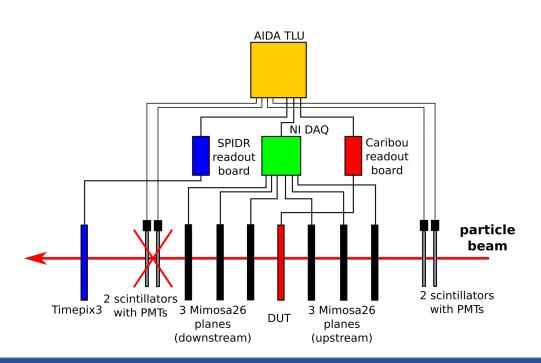
Jens Kröger Heidelberg University & CERN

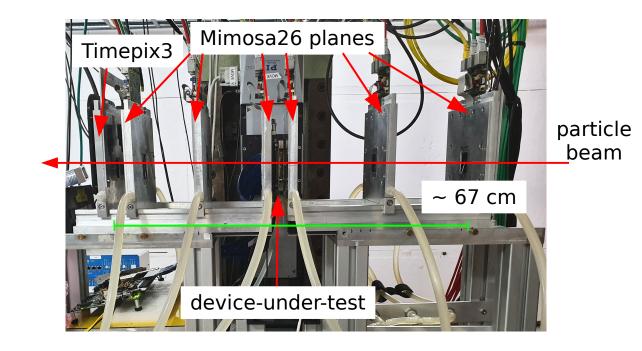


## **Test Beam Setup at DESY**

- AIDA TLU
- 2-3 scintillators + PMTs
- 6 Mimosa26 planes
- Timepix3
- DUT

- → provides global clock (time sync.)
- + triggers Mimosa Readout
- → input to TLU
- → good spatial resolution, "no" timing (2x 115µs bins rolling shutter)
- → nanosecond track timestamps
- → CLICpix2, ATLASpix, CLICTD





## **Reference Time Measurement**

### **AIDA TLU:**

- coincidence from 2-3 scintillators
  - coarse (25ns bins)
  - fine (780ps bins) for each scintillator
- "precise time = coarse + fine"
  - including measured delays (cables, TOF, ...)
- → 2 scintillators: 600 ps
- → 3 scintillators: 450 ps

#### Note:

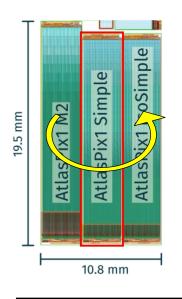
- scintillators not tuned (potential for more)!
- repeat analysis for all test-beams (different scint.)

### Timepix3:

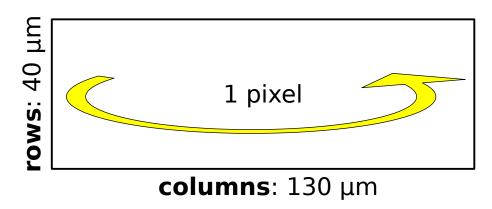
- applied lab calibration by Florian Pitters
  ⇒ see CLICdp-Pub-2019-001
- time resolution ~ 1.1 ns
  - unfolded TLU resolution
  - cross-validated analysis with SPS data (2015)
- → fully sufficient for all current DUTs
- + validate TLU performance
- → for highest timing resolution:
- use Timepix3 for track-by-track timestamp
- replace by nearest TLU timestamp

### sensor dimensions:

- 25 columns (130 μm pitch)
- (40 µm pitch) 400 rows

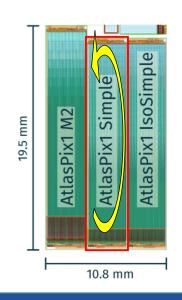


#### rotation in column direction

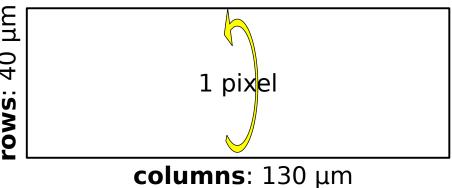


## **Use case in tracking detector:**

- rotation in column direction
  - forward tracks
- rotations in row direction
  - low p, tracks (more curled)



### rotation in row direction

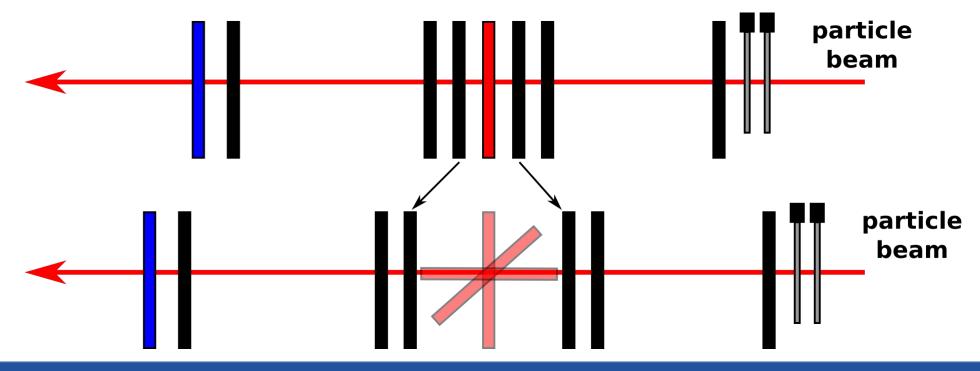


# **Rotation Analysis Objectives**

### has not been done before

- cluster formation
- depletion depth
- timing performance
- efficiency (?)

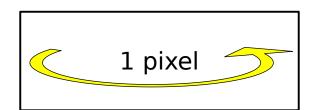
**But:** rotations require **larger** telescope spacing → **reduced** tracking precision

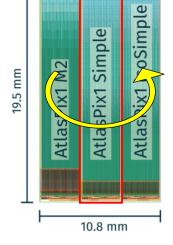


- rotation in column direction
- cluster width column
  → grows significantly
- cluster width row
  → grows slightly (angled tracks)

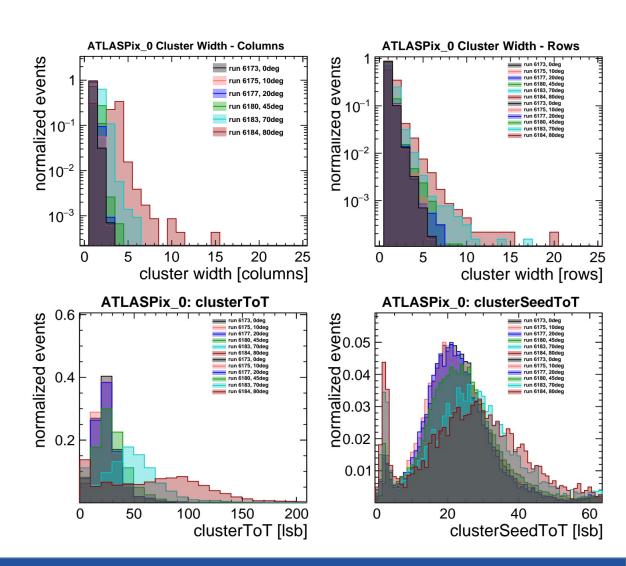
cluster ToT and seed pixel ToT

→ clear angle dependence





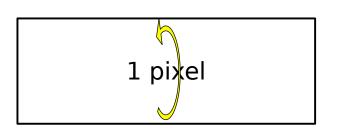
# no tracking yet! alignment work-in-progress

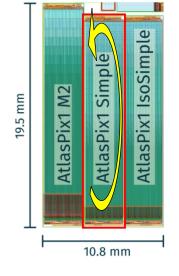


- rotation in row direction
- cluster width column
  → grows slightly (angled tracks)
- cluster width row
  → grows significantly

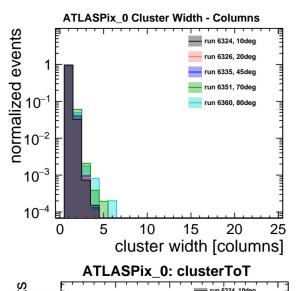
cluster ToT and seed pixel ToT

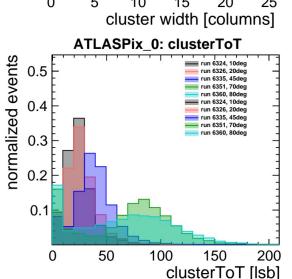
→ clear angle dependence

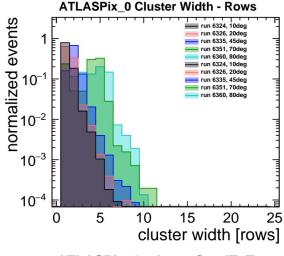


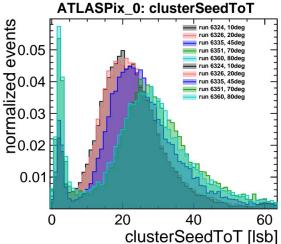


### no tracking yet! alignment work-in-progress

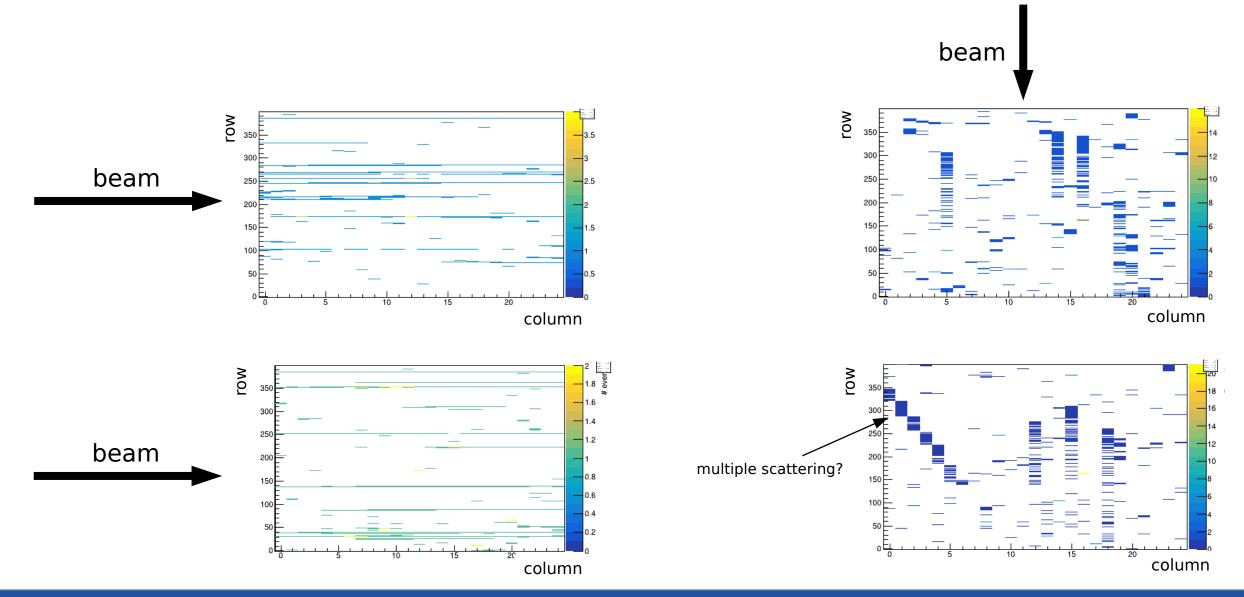








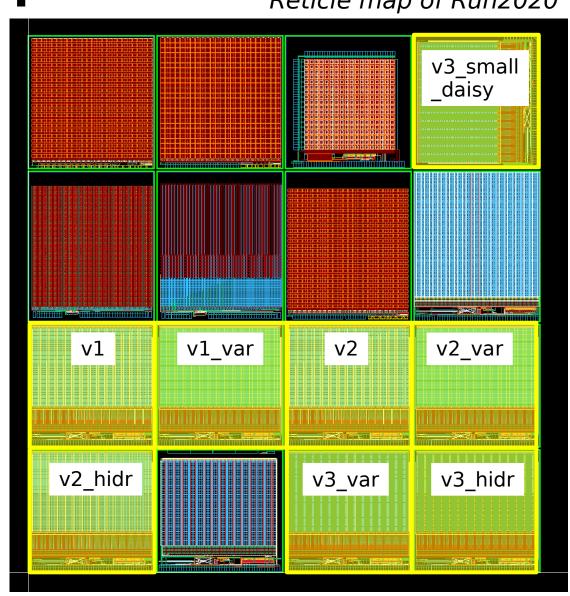
# **Event Displays at 90° Rotations**



## What's next after ATLASpix?

### Reticle map of Run2020

- TSI engineering run submitted in **May 2020** → called "Run2020"
- 8 new similar chips (+ 8 others)
  - for CLIC, LHCb, PANDA etc.
  - based on ATLASpix(3) design
- each sensor:
  - same size ( $\sim$ 5x5 mm<sup>2</sup>)
  - same periphery and readout
- → 1 readout system:
  - directly compare 8 sensors

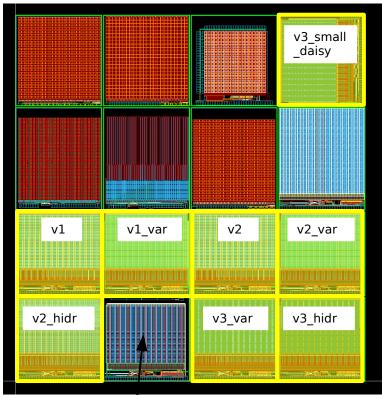


## **8 Similar Sensors**

- same: size, periphery, readout, pinout
- different: comparators, amplifiers
- v1: NMOS comparator
  - well-known (safe option)
- v2: CMOS comparator
  - better performance expected
  - but: manufacturing risk due to additional deep p-well
- v3: comparator in periphery
  - very fast (only for large pixels)
  - allows daisy-chain readout

- V\*:
  - 29 x 124 pixels
  - 25 x 165 μm<sup>2</sup>
- V\* Var: variable pixel size
  - $50 \times 165 \, \mu m^2$  and
  - 100 x 165 μm<sup>2</sup>
- \*\_hidr: high dynamic range
  - 2 comparators:
    - one fast for timestamp
    - one slow for ToT

### Reticle map of Run2020



### small pixel HV-MAPS:

- 25 x 35 μm<sup>2</sup>
- CLIC Vertex Detector?

## Which are relevant for CLIC?

# Reminder

### CLIC tracker requirements

- spatial resolution:
  - ~ 7 μm (transversal)
- max. granularity:
  - 1-10 mm pixel size (longitudinal)

**NMOS** 

comp.

**CMOS** 

comp.

distributed

comp.

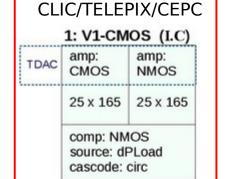
### ATLASpix: 40 x 130 μm<sup>2</sup>

- transversal: 40  $\mu$ m/ $\sqrt{12}$  ~ 11.5  $\mu$ m (binary resolution)
- longitudinal: 130 μm << 1 mm

New sensors: 25 x 165 μm<sup>2</sup>

- transversal: 25  $\mu$ m/ $\sqrt{12}$  ~ 7.2  $\mu$ m (binary resolution)
- longitudinal: 165 μm << 1 mm

### relevant for CLIC:



#### 3: V2-NMOS (II.N)

amp:

DAC	PMOS	NMOS	
	25 x 165	25 x 165	
	comp: CMOS source: dPLoad cascode: circ		

#### 5: V3-NMOS (III.NS)

DAC	amp: PMOS	amp: NMOS
8,000,010	25 x 165	25 x 165
	comp: dis	nt wires

#### LHCb "MightyPix"

#### 2: V1-VSIZE (I.V) 100 x 165 PMOS std 8u DS CC 50 x 165 PMOS std 8u DS CC

comp: NMOS

#### 4: V2-VSIZE (II.V)

100	x 16	5 PMC	os
std	8u	DS	СС
50	x 16	5 PMC	os
std	8u	DS	CC
com	ip: CN	/OS	

#### 6: V3-VSIZE (III.V)

100	x 16	5 PMC	os
std	8u	DS	CC
50	x 16	5 PMC	os
std	8u	DS	CC
com	p: dis	tribute	ed

#### LHCb/PANDA

Standard design:

4µ, single source, linear cascode

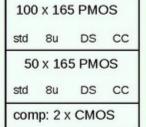
Legend:

std = standard

DS = double source

CC = circular cascode

#### 7: V2-VSIZE (II.H)



- 2 comparators:
- one slow one fast
- → high dyn. range (hidr)
- provides high energy & time resolution

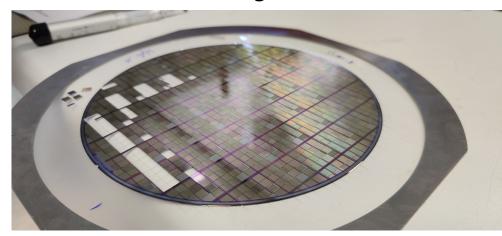
#### 8: V3-VSIZE (III.H)

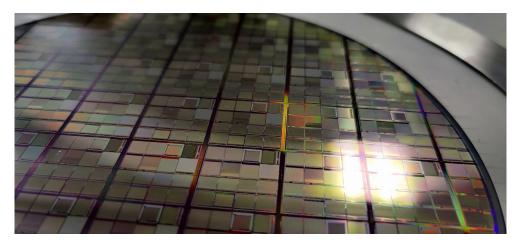
100 x 165 PMOS std 8u DS CC 50 x 165 PMOS std 8u DS CC comp: 2 x distributed

## **Timeline + Status**

- submission in May 2020
- wafers received in September 2020
- 1 unthinned wafer diced at KIT (Karlsruhe)
- started testing in Heidelberg
- other wafers:
  thinning + dicing at Optim (France)
  → delayed by COVID
- first LHCb test-beam at DESY in 3 weeks
  - support by Mu3e group (Heidelberg)
  - support by me for reconstruction (Corryvreckan)

### Wafer Picking in Karlsruhe





## **Summary:**

### **Reference Time**

quantified precisely now

- AIDA TLU: 450 – 600 ps

Timepix3: 1.1ns

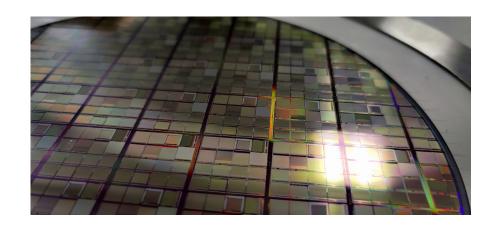
### **ATLASpix Rotation Scans**

- first sanity checks
  → good data quality
- analysis ongoing
  - → interesting physics results expected

## **Outlook:**

### **New Sensors**

- based on ATLASpix design
- produced by TSI, testing has begun in HD
- next: integration in Caribou



### **Acknowledgment:**

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

# Backup

in case there are some questions...

## Run2020: More details on the sensors

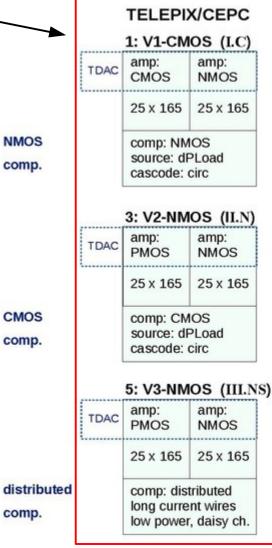
relevant for CLIC tracker: -

ATLASpix:  $40 \times 130 \mu m^2$ 

25 x 165 μm<sup>2</sup> now:

> NMOS comp.

- each pixel contains:
  - n-well (electrode)
  - charge-sensitive amplifier (CSA)
  - output transistor
  - TDAC (not all matrices), 3 tune + 1 enable
  - injection switch + capacitor



#### LHCb

#### 2: V1-VSIZE (I.V) 100 x 165 PMOS std 8u DS CC 50 x 165 PMOS std 8u DS CC comp: NMOS

#### 4: V2-VSIZE (II.V)

l	100 x 165 PMOS				
l	std	8u	DS	СС	
ſ	50 x 165 PMOS				
١	std	8u	DS	СС	
Ì	com	p: CN	IOS		

#### 6: V3-VSIZE (III.V)

100	x 165	РМС	S
std	8u	DS	СС
50 x 165 PMOS			
std	8u	DS	CC

#### LHCb/PANDA

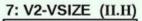
Standard design: 4µ, single source, linear cascode

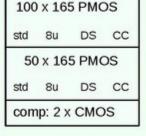
Legend:

std = standard

DS = double source

CC = circular cascode



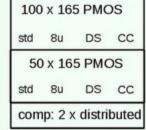


- one slow - one fast
- → high dyn. range (hidr)

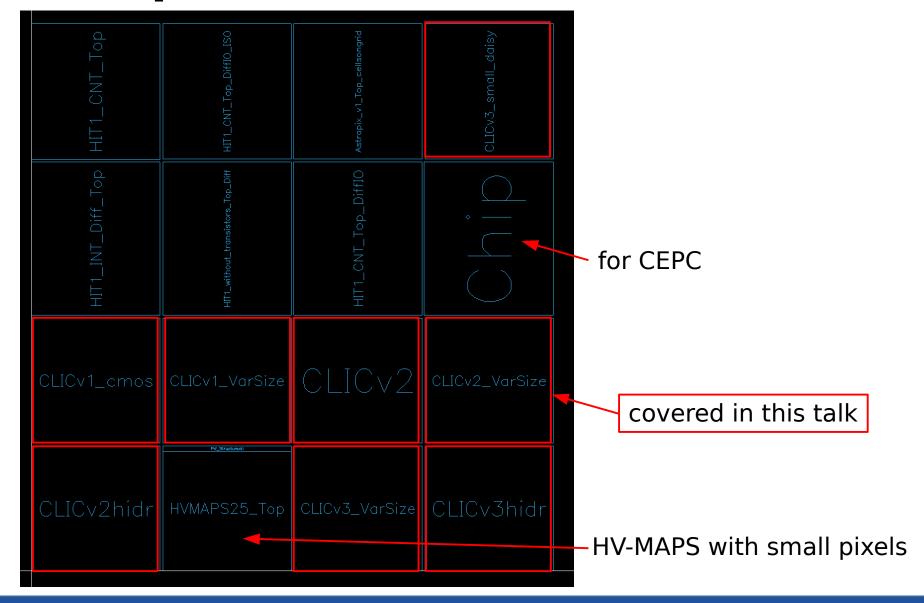
2 comparators:

provides high energy & time resolution

#### 8: V3-VSIZE (III.H)



## Run2020: all chips on the reticle



# **Pros and Cons of the Different Designs**

### **Comparators**

#### NMOS:

- + standard used so far
- high current consumption
- larger delay than CMOS
- additional 2.1V
- reduced output amplitude
- large area, large capacitance

#### • CMOS:

- + faster than NMOS at same current
- + smaller
- + more radiation tolerant (?)
- additional deep p-well (1st time for TSI) → some risk

#### distributed

- + very small capacitance in pixel
- + fast, low power
- + no additional p-well
- 2 lines per pixel → only feasible for larger pixels

### **Amplifiers**

#### PMOS:

- + lower noise at high current
- + smaller timewalk
- + more suitable for larger pixels (large capacitance)

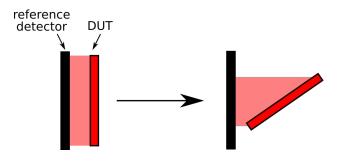
#### NMOS:

- + better timewalk at small currents
- + more suitable for smaller pixels (small capacitance)
- some risk: more flicker noise + less experience

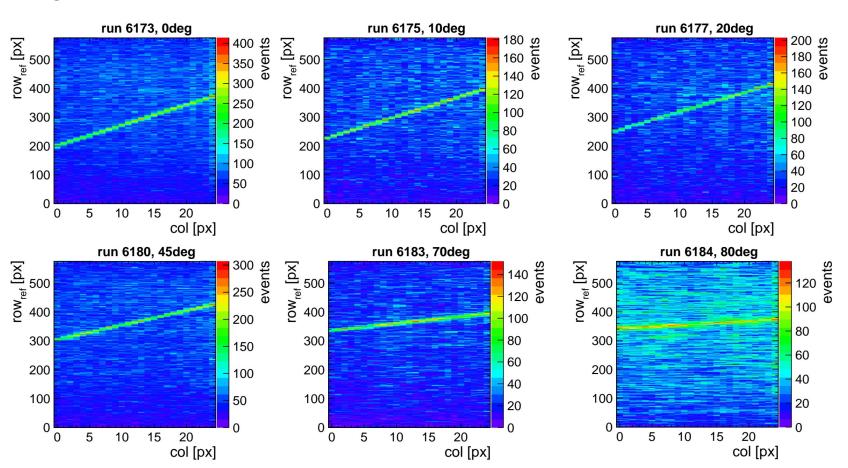
#### CMOS:

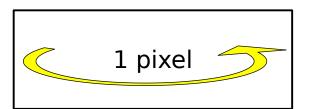
+ for very low bias current (like at CEPC)

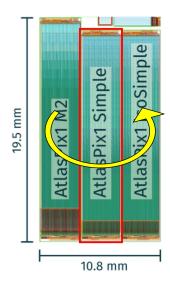




larger rotation → cover **all columns** on DUT with **fewer rows** of reference detector (rotated by 90°)

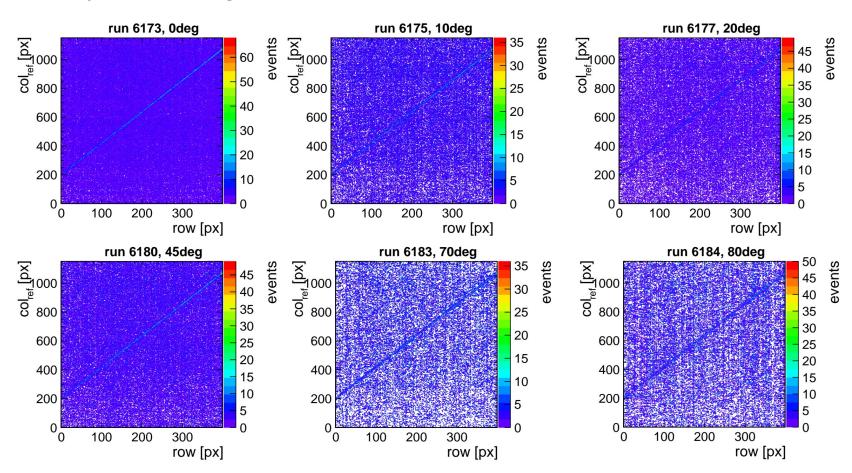


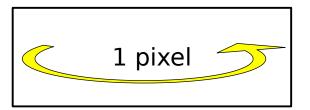


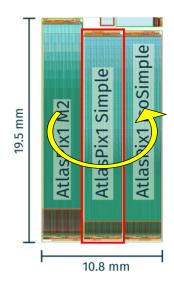


• 2D correlations for rotation in column direction

as expected: no significant effect for rows

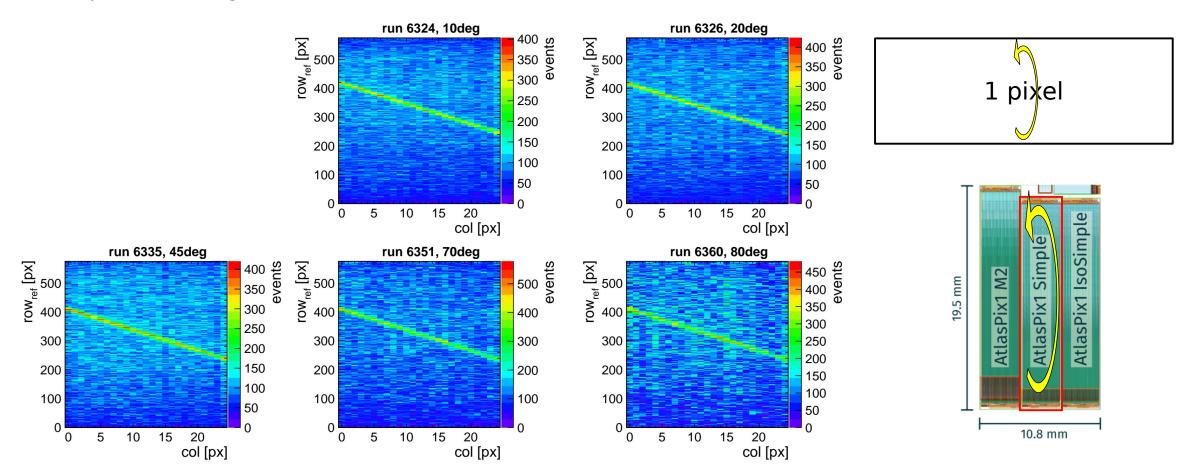




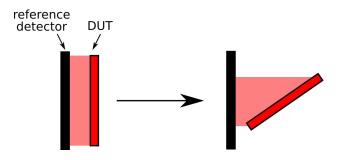


2D correlations for rotation in row direction

as expected: no significant effect for columns



2D correlations for rotation in row direction



larger rotation → cover all rows on DUT with fewer columns of reference detector (rotated by 90°)

