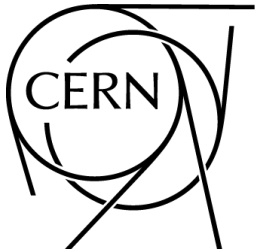
Lessons learned from simulation based 180nm small collection electrode CMOS technology optimization

M. Munker, D. Dannheim, W. Snoeys

CLICdp Workshop, October 2020



EP-DT
Detector Technologies

Outline

- Introduction
- Understanding of technology with 3D TCAD
- Optimization – concepts developed in 3D TCAD and implementation in prototype chips
- Summary & outlook

Introduction

Motivation – why do we need to optimize CMOS sensors?

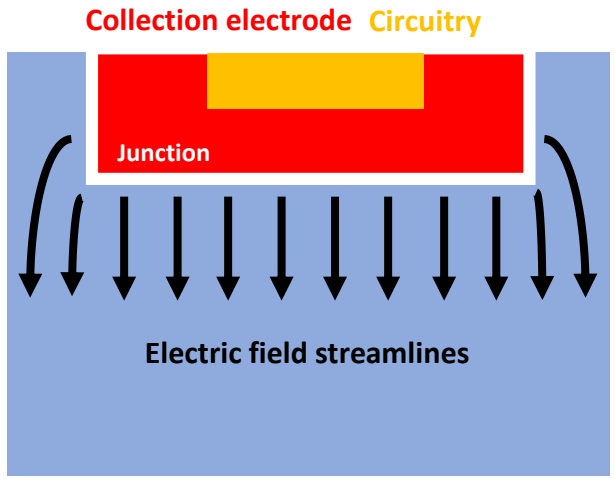
- **Aim = combination of:**
  - + Monolithic
  - + Small capacitance
  - + Fast charge collection

"Golden" set of parameters:

→ Reduce production effort, costs + material
→ Improve S/N → reduce power consumption + improve timing/spatial precision
→ Improve timing precision + radiation tolerance

- **Challenge:**
  - Difficult to maintain high & uniform field (precise time-stamping and radiation tolerance) with small collection electrode/capacitance

Large collection electrode:



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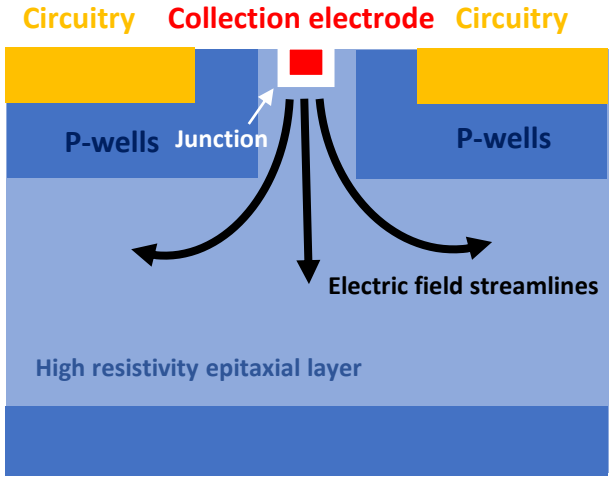

Relevant for & performed within:

- CLIC Vertex & Tracker R&D
- FASTPIX ATTRACT
- ATLAS Itk upgrade
- EP R&D, TJ 65nm
- …

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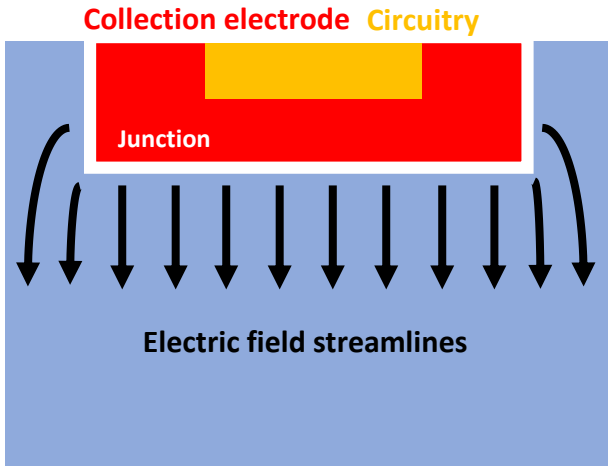

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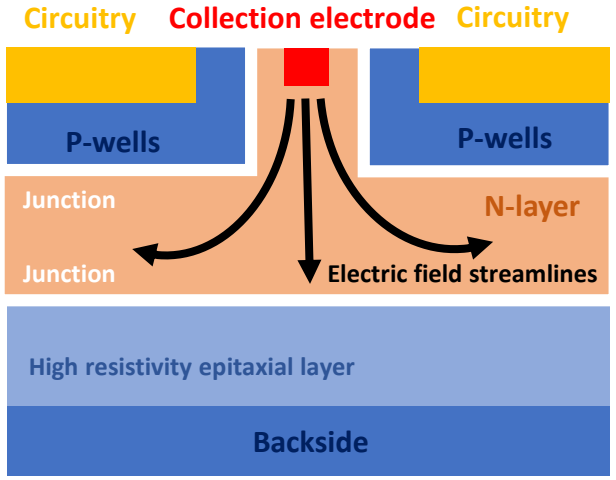

Cross section of 180nm TJ process, used for optimization.

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- CLIC Vertex & Tracker R&D
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- ATLAS Itk upgrade
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- …

W. Snoeys et. al: https://doi.org/10.1016/j.nima.2017.07.046

Monolithic CMOS sensor simulation basics

Monolithic CMOS = placement of circuitry in sensor:

→ Fundamental change of electrostatic situation

→ Essential change of charge collection

→ Major change of performance

1. Sensor simulation & optimization with finite element simulations:

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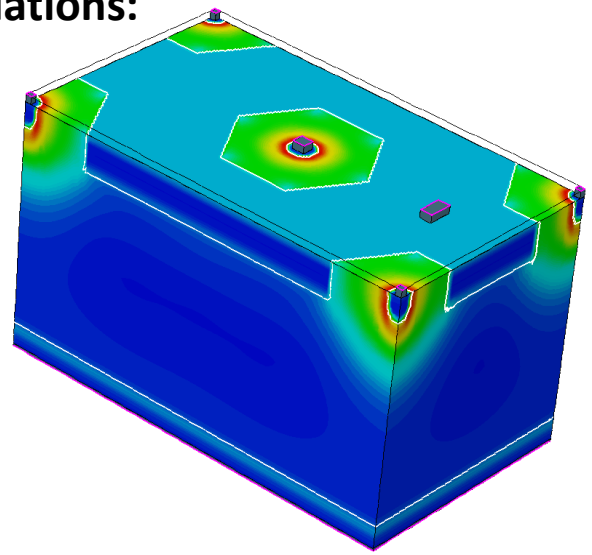
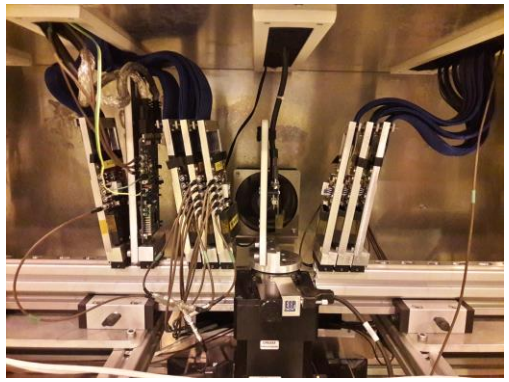


SILVACO SYNOPSYS® Silicon to Software™



2. Need to evaluate performance of optimized sensor:

- Transient TCAD (very computing intensive, but fully self consistent solution)
- Test-beam (usually large effort for development of test environment, complex convolution of sensor and readout effects, but: realistic)
- Transient Monte Carlo (Allpix^2, see Simon's talk, Garfield++) + electrostatic TCAD (fast, access of high statistics with high level of detail in-pixel & in-sensor resolved)

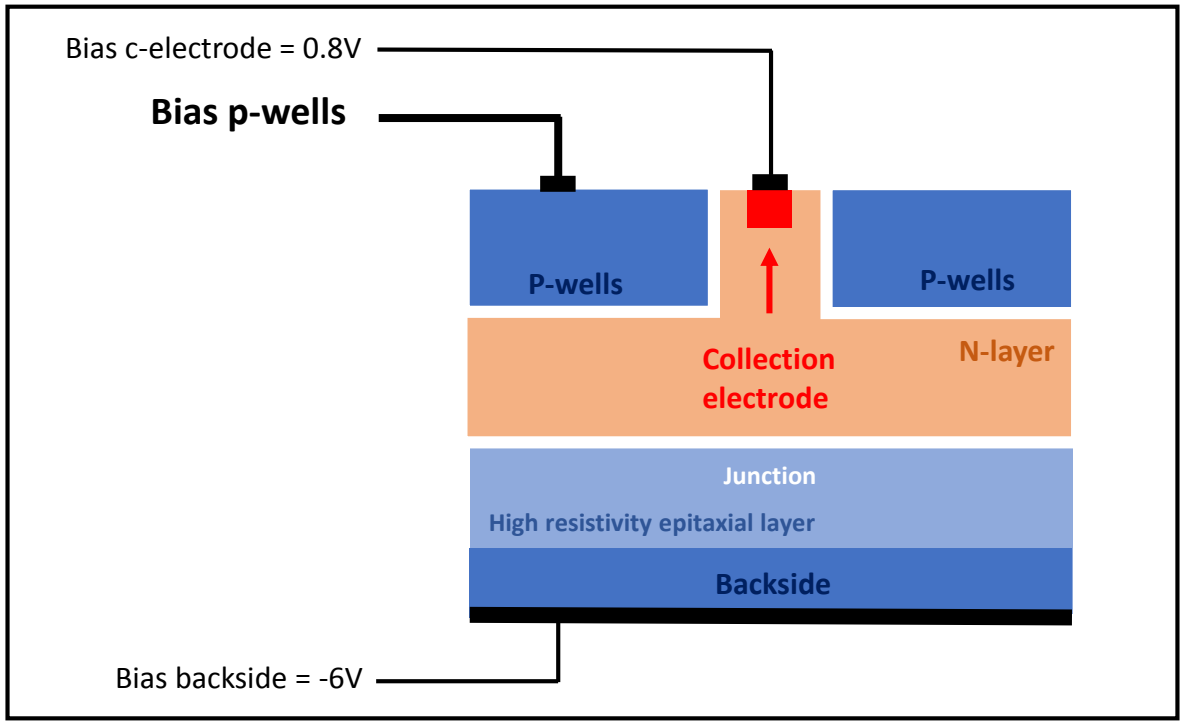
Understanding of technology with 3D TCAD

Depletion for different p-well voltage

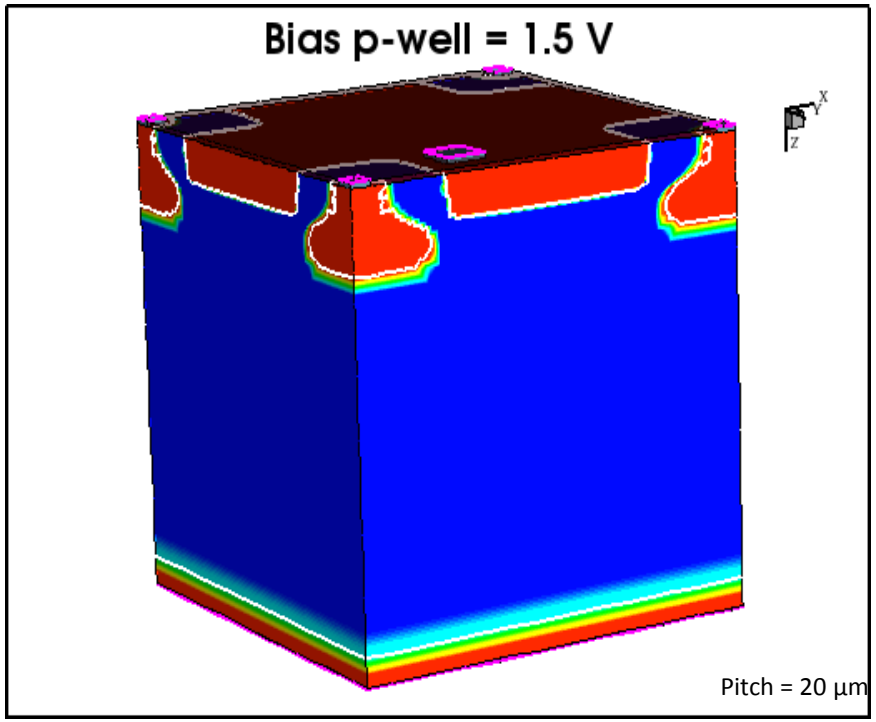
Motivation:

- Depletion around collection electrode ∝ sensor capacitance ∝ **noise and threshold**
- **Depletion in depth ∝ signal**

Sensor bias configuration:



Field in depth (color scale) for different p-well bias:



- Lesson learned:
  - Depth fully depleted by bias of backside and c-electrode
  - Bias p-wells important to deplete n-layer (capacitance) but constrained by circuitry (breakdown of NMOS)

Depletion for different p-well voltage

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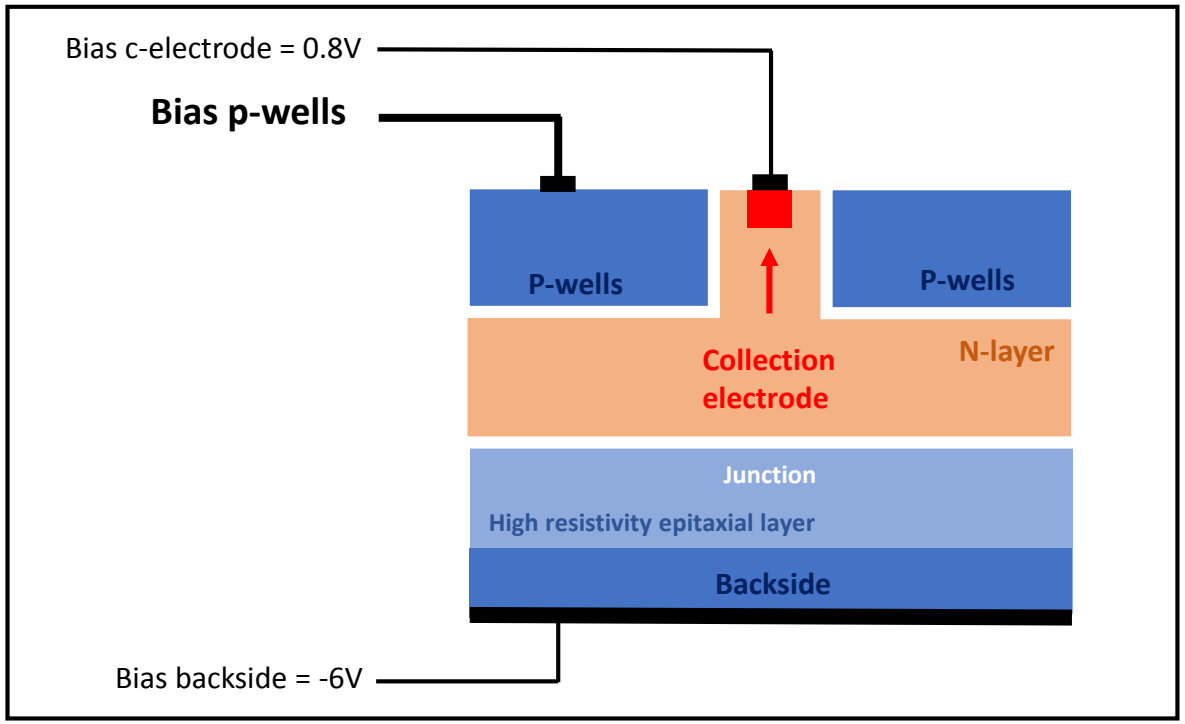
Sensor bias configuration:



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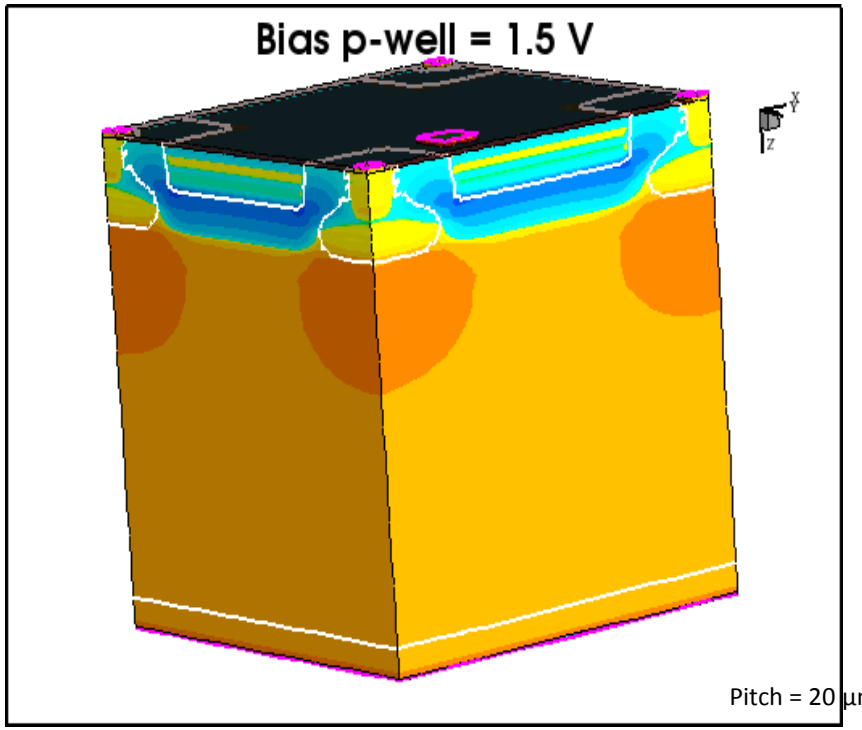


For higher p-well voltage:

- Higher field in depth around c-electrode (positive voltage terminal), lower in large rest part of sensor

Lesson learned:

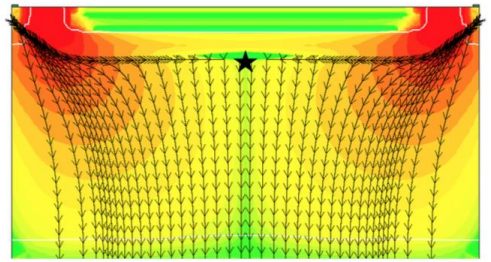
- Depletion backside reduces for higher p-well voltage because voltage gradient (electric field) between p-wells and backside is reduced!

→ Example of 'non-standard performance' and need of 3D TCAD to understand technology performance

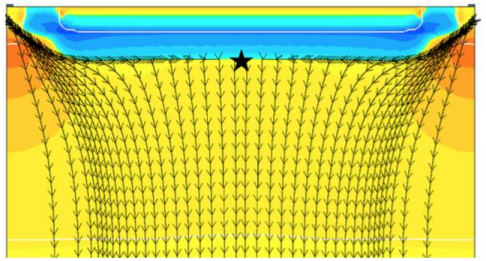
Electric field minimum

Electric field minimum (star symbol) and electric field streamlines (arrow-lines):

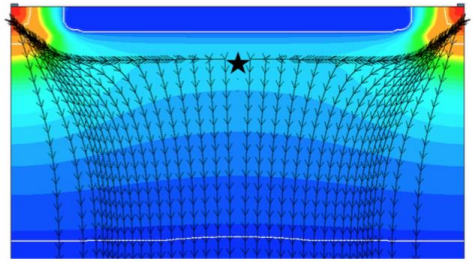
Lateral field:



Field in depth:



Electrostatic potential:



Pitch = 36.4 µm

Lessons learned:

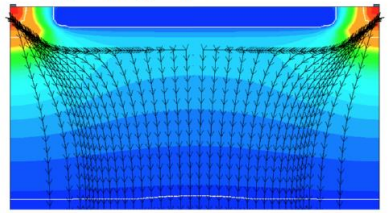
Electric field minimum at pixel borders comes from placing the p-wells (circuitry) in the sensor (can not be removed)

→ Have to minimize/mitigate the pixel edge regions

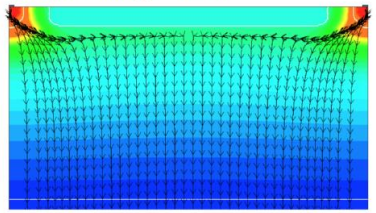
Example for implication of electric field minimum:

Field in depth (color scale) and electric field streamlines (arrow-lines):

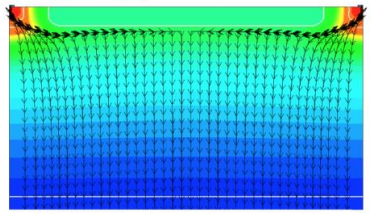
Backside voltage −6 V:



Backside voltage −15 V:

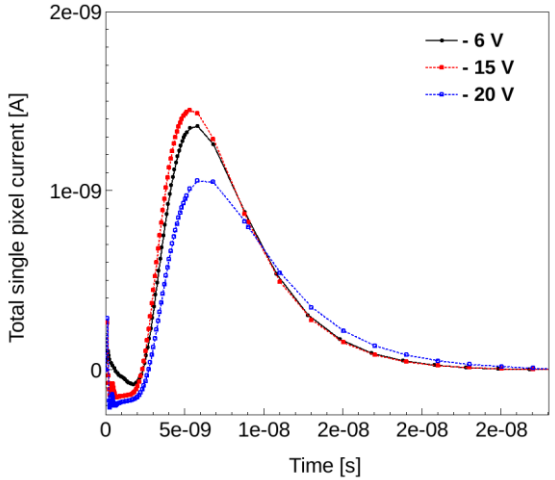


Backside voltage −20 V:



Pitch = 36.4 µm

Current pulse for MIP traversing pixel corner
for different backside bias after irradiation:



Lesson learned:

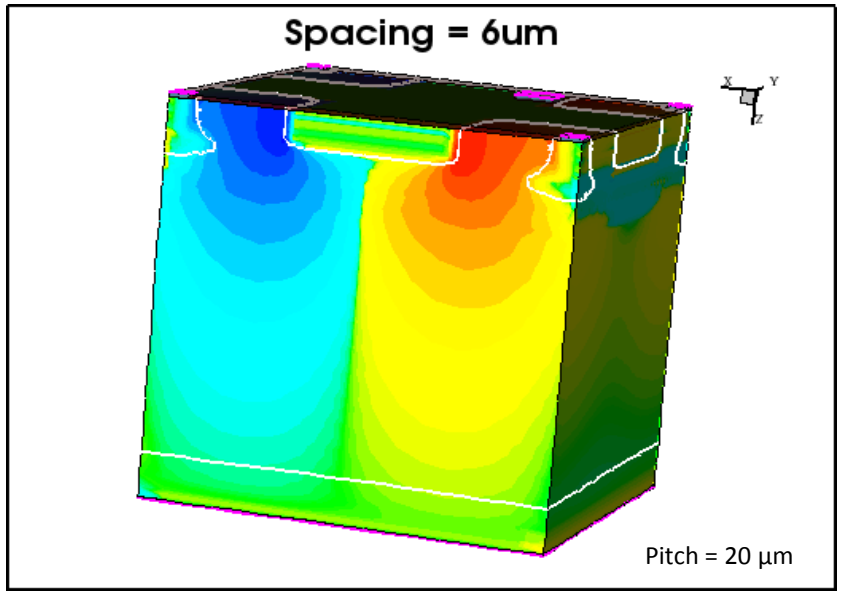
Because of the small c-electrode and the electric field minimum, the difference between lateral field and field in depth is important for the charge collection

→ Higher absolute field does not always result in a faster charge collection & improved radiation tolerance!

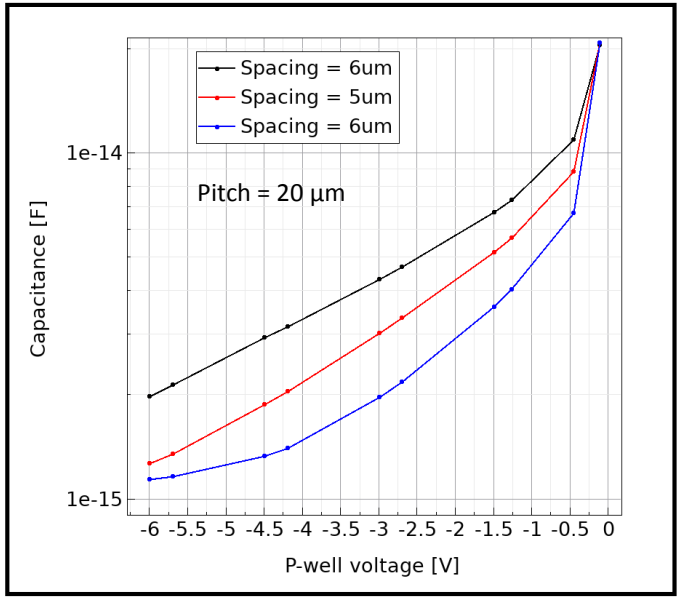
Trade-off between capacitance and lateral field

Spacing = distance between c-electrode and p-wells

Lateral field (color scale) and depletion (white lines) for different spacings:



Capacitance vs. p-well bias for different spacings**:**



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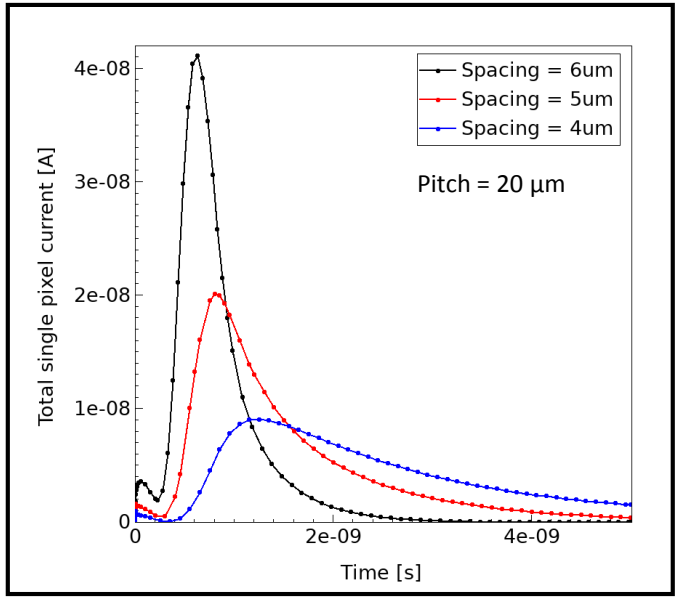


1. Depletion around collection electrode reduces for smaller spacings → Smaller capacitance for smaller spacing
2. Lateral field reduced for smaller spacing → Slower charge collection for smaller spacing

Lesson learned:

→ Trade-off between lateral field (speed of charge collection) and capacitance (noise, threshold)

→ Note also large performance variations for only small change (1 µm different spacing)! → complex optimization.

Summary of main lessons learned for understanding of technology

We can not use the concepts from standard planar sensors for this technology, for example:

- Higher sensor bias can result in less depletion
- Higher sensor bias can result in slower charge collection

→ Need to perform 3D TCAD to develop understanding for this technology.

Parameters are highly correlated and very sensitive to small changes, for example:

- A small change of 1 µm different spacing changes significantly the speed of charge collection and sensor capacitance and space available for circuitry!

→ Dedicated optimization in 3D TCAD for each geometry needed

Performance limited by electric field minimum:

→ Need to maximize the lateral field

→ Need to break trade-off between small capacitance and high field

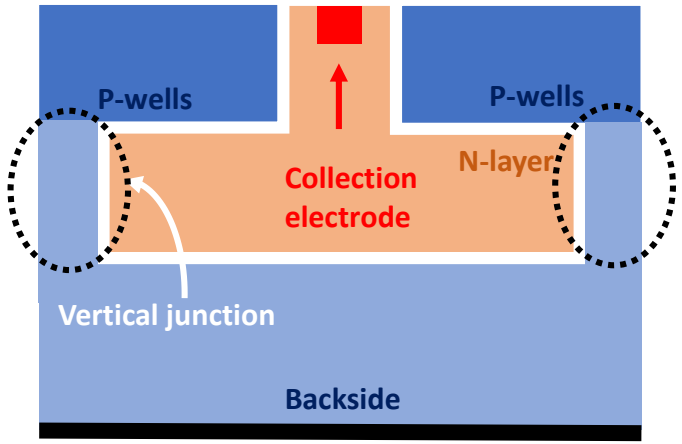
→ Need to reduce the edge regions

Optimization –
concepts developed in 3D TCAD and implementation in prototype chips

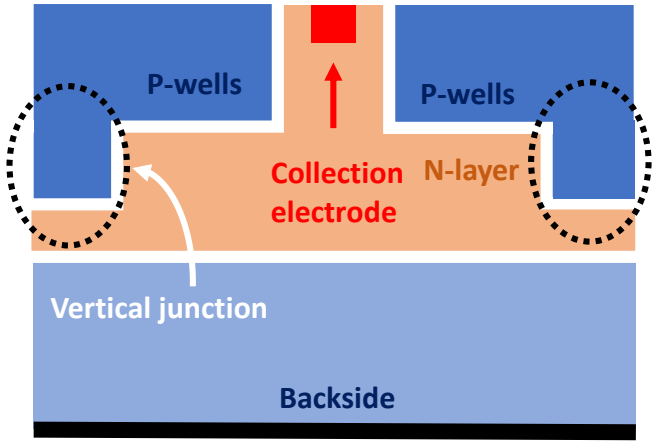
Gap in n-layer and additional p-implant – modifications to maximize the lateral field

M. Munker et. al: doi:10.1088/1748-0221/14/05/c05013

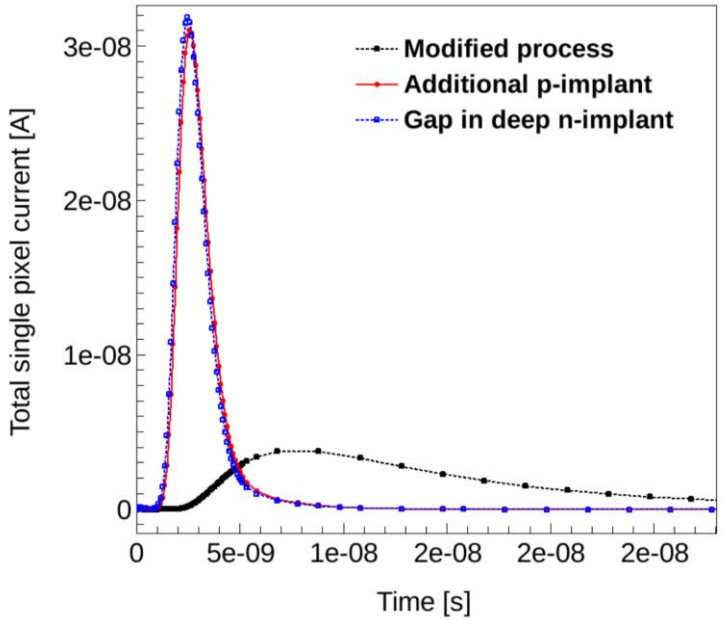
Gap in N-implant (in dashed ellipse):



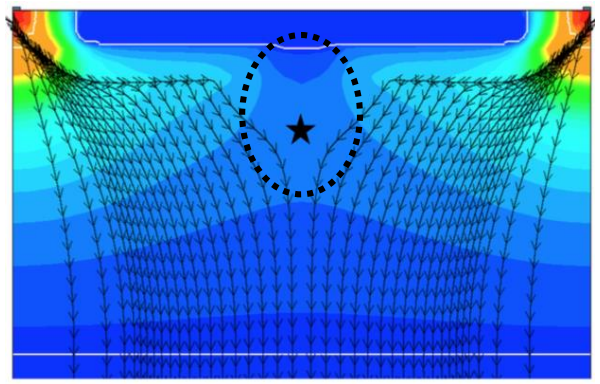
Additional p-implant (in dashed ellipse):



Current pulse for MIP traversing pixel corner for different process variants:

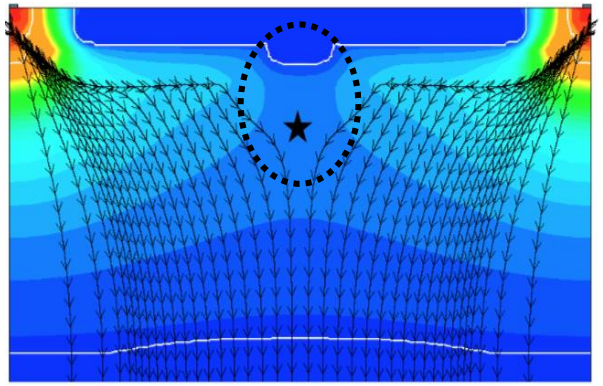


E-static potential, gap in layer:



Pitch = 36.6 µm

E-static potential, additional p-implant:



Lesson learned:

Significant speed up of charge collection, results in:

1. Increased radiation tolerance (HL-LHC, future proton colliders)
2. Improve temporal precision (future colliders, e.g. CLIC)
3. Reduce charge sharing (improved energy resolution, medical applications, high efficiency for thin sensors)

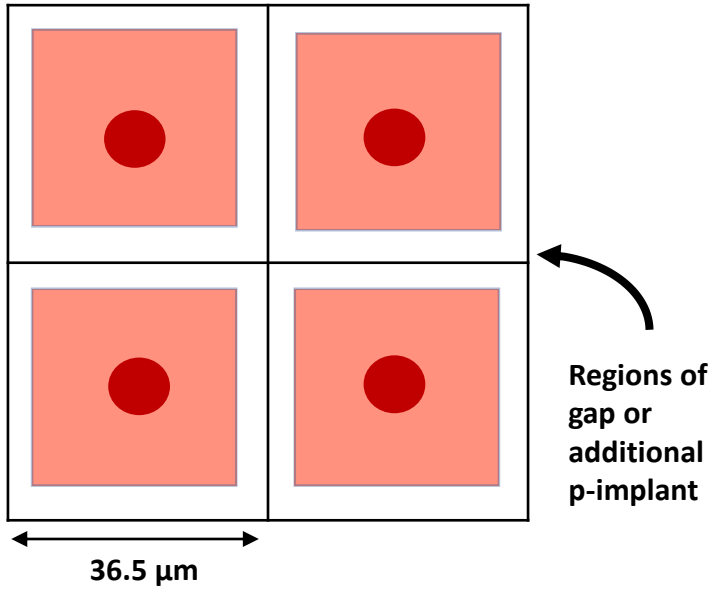
Note: lateral field maximized while not changing capacitance!

Example test-beam results - validation of simulations

M. Dyndal et al.: https://doi.org/10.1088\%2F1748-0221\%2F15\%2F02\%2Fp02005

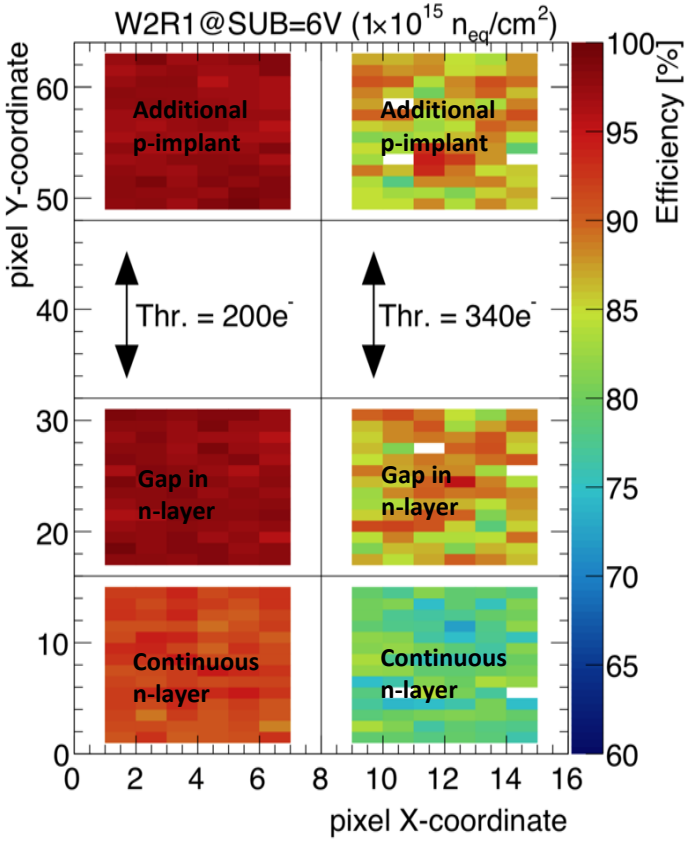
MALTA - an asynchronous readout CMOS monolithic pixel detector for the ATLAS High-Luminosity upgrade:

Mini-Malta pixel layout:



Regions of gap or additional p-implant

Mini-Malta efficiency after irradiation for different process variants:



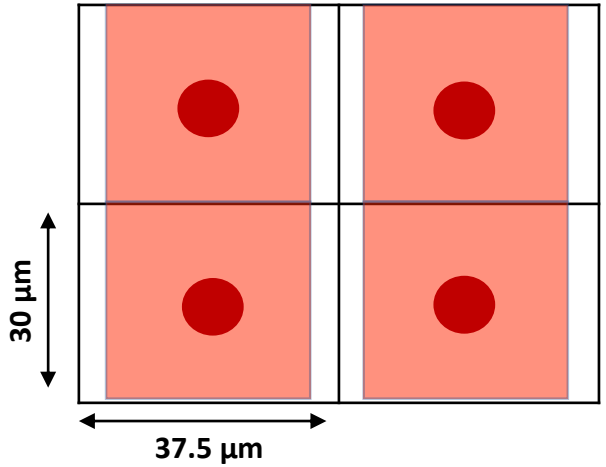
Lesson learned:

→ Increased charge collection time results in increased radiation tolerance

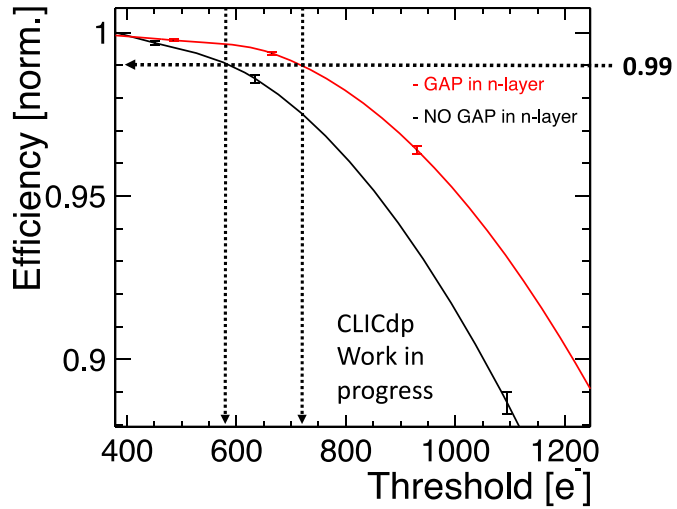
→ Radiation hard small c-electrode design achieved with modifications

CLIC tracker chip CLICTD – see Katharina's talk:

CLICTD sub-pixel layout:



CLICTD efficiency for different process variants:



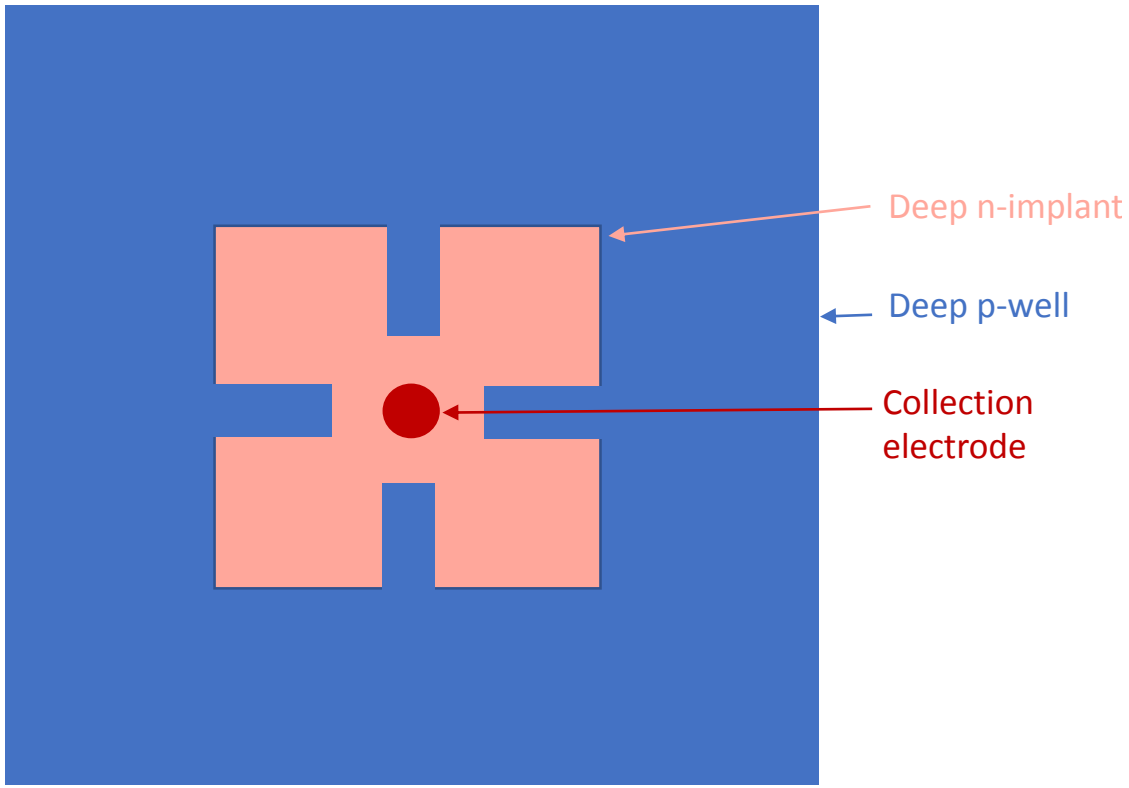
Lesson learned:

→ Reduced charge sharing for process with gap results in larger efficient operation window

→ Relevant for thin epi layers in 65nm TJ process!

P-well fingers - modifications to break trade off between capacitance and lateral field

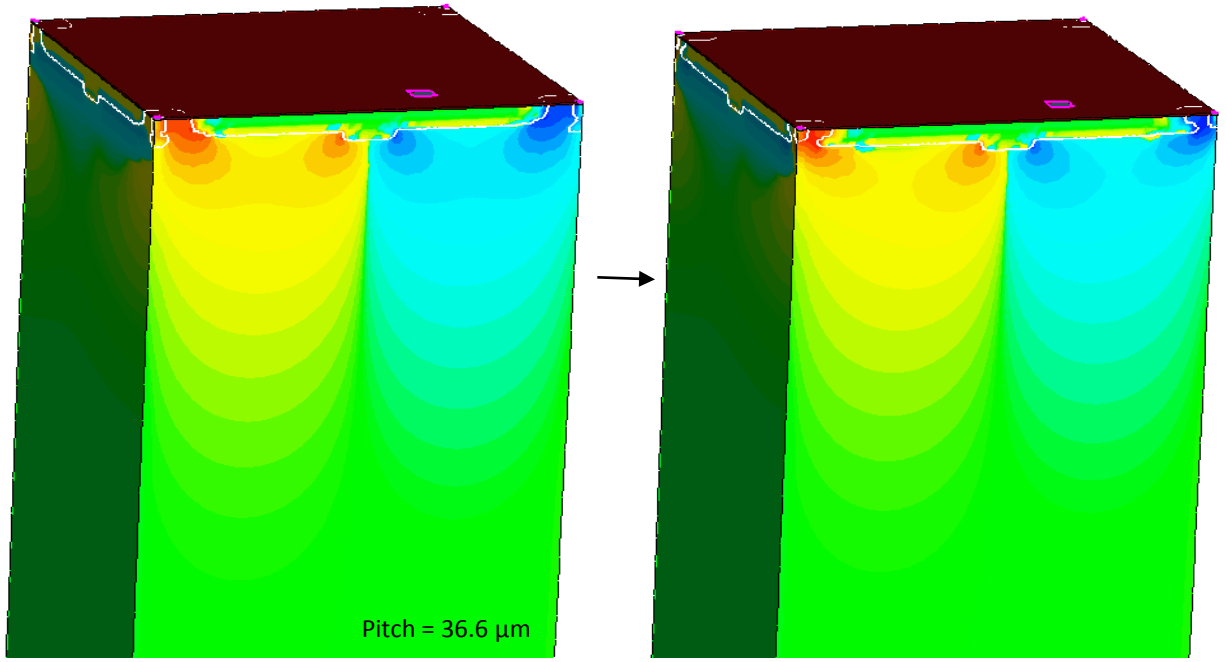
Top view on pixel cell:



Lateral field (color scale):

Standard opening:

Modified opening with p-well fingers:



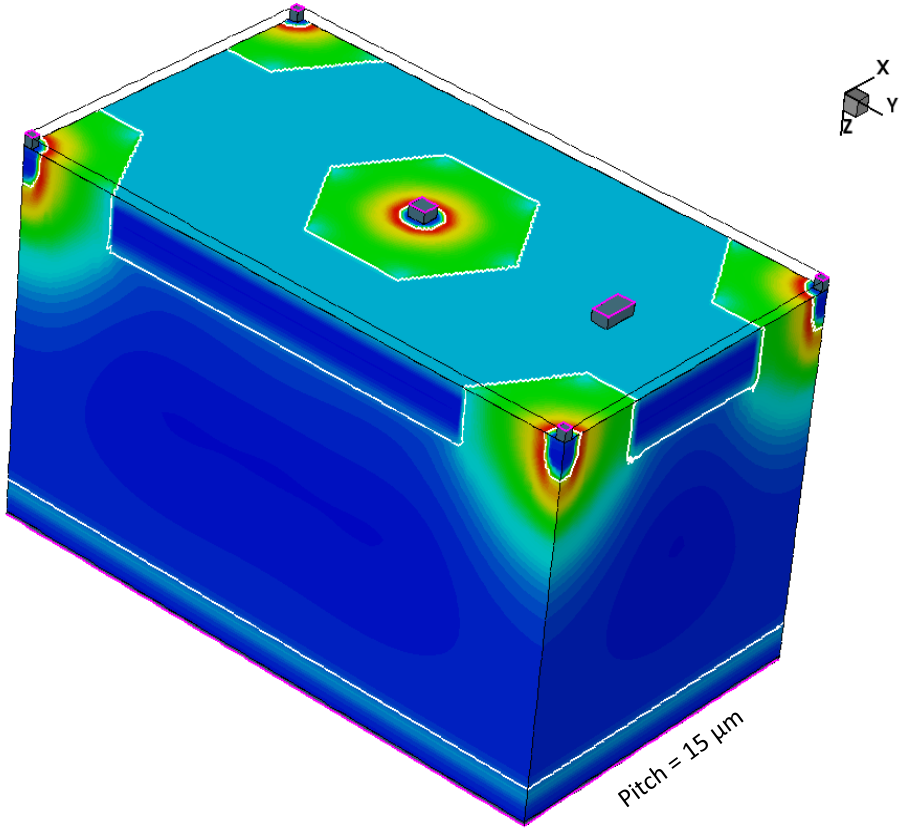
Lesson learned:

→ Capacitance reduced (in this case by factor of 2)

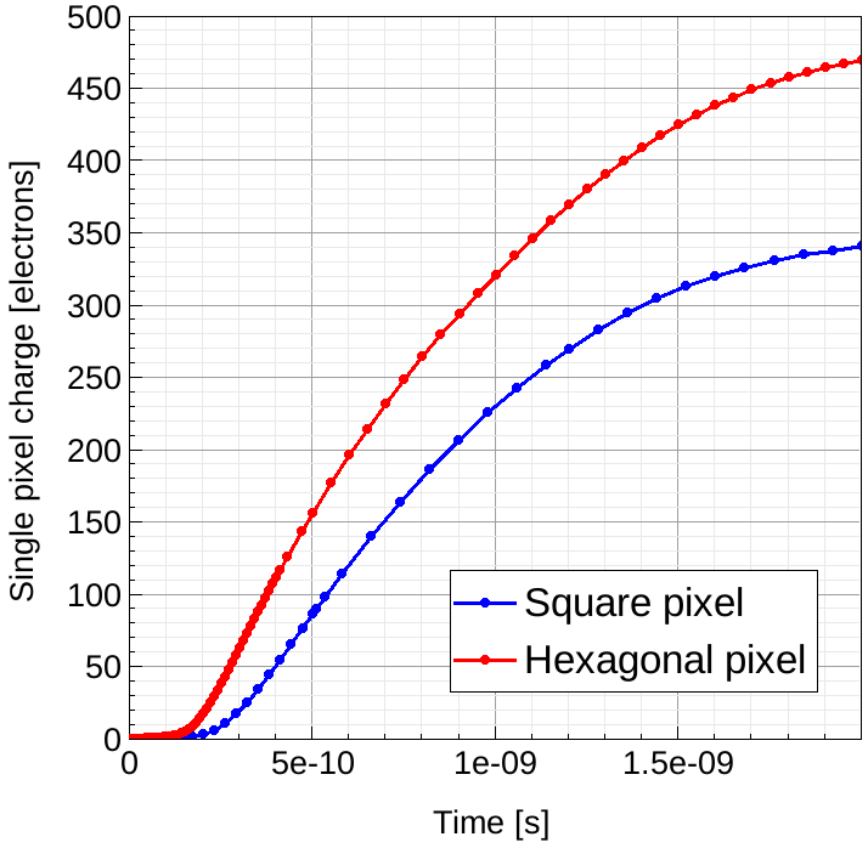
→ Impact on lateral field (charge collection) small since deep p-well is only extended in small 'fingers'

Hexagonal pixels - modification to minimize the edge regions

Simulated hexagonal unit cell – electrostatic potential:



Comparison hexagonal to square pixel cell charge vs. time for MIP incident at pixel corner:



Lessons learned:

→ Hexagonal design reduces the number of neighbors and charge sharing → higher single pixel signal → **higher efficiency for thin sensors (65nm TJ)**

→ Hexagonal design minimizes the edge regions → **faster charge collection**

Czochralski - modified starting material to increase signal

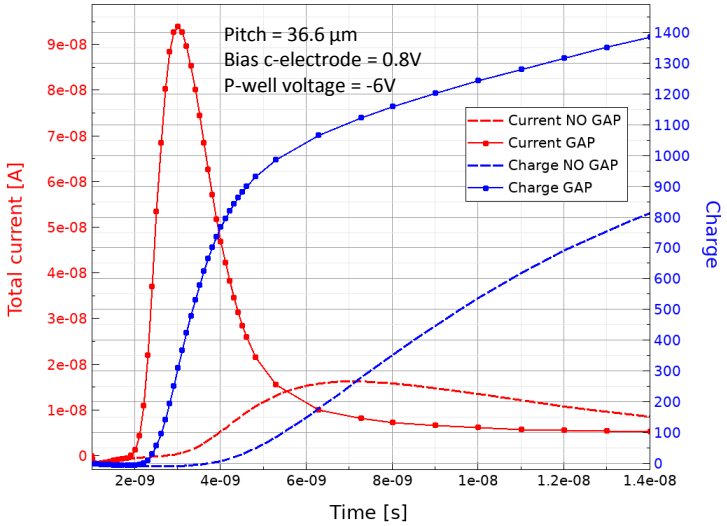
Epi layer thickness limited → use High Resistivity Czochralski wafers as starting material to increase depleted sensor region and signal

H. Pernegger et. al., Hiroshima conference 2019

Some example questions/studies:

Do modifications still improve speed of charge collection for thick sensors?:

Current pulse with and without gap in n-layer for 50µm thickness and -6V on backside: :

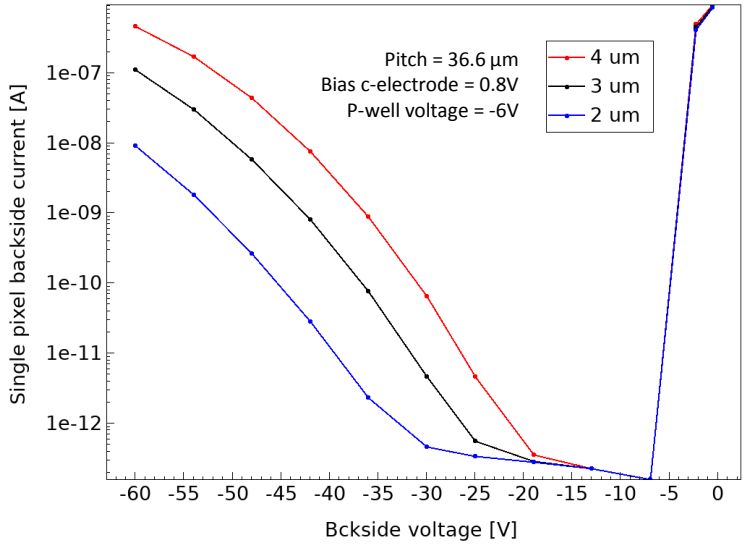


Lesson learned:

Modifications improve charge collection speed even for thick sensors (weighting field)

Can we achieve a sizable depletion even with the modifications?

Punch through current between p-wells and backside for different sizes of the additional p-implant:

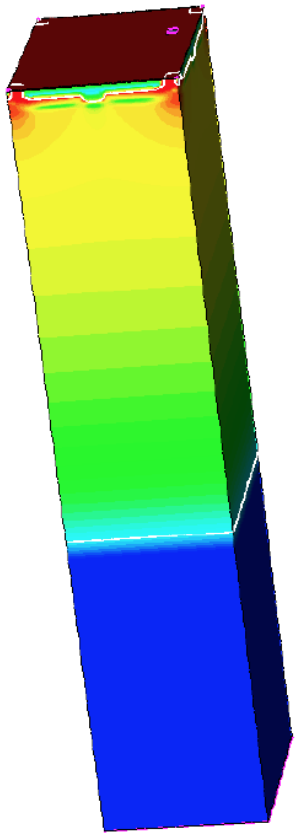


Lesson learned:

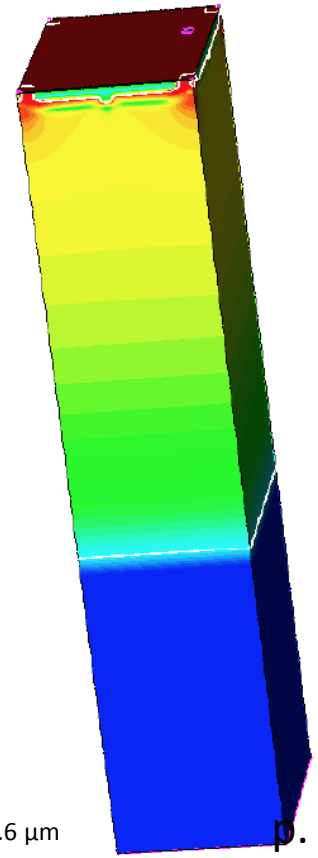
Better depletion (less punch through) for smaller p-implant while not impacting lateral field & charge collection

Lateral field (color scale) for 150µm thickness and -30V on backside:

P-implant = 4 µm:



P-implant = 2 µm:



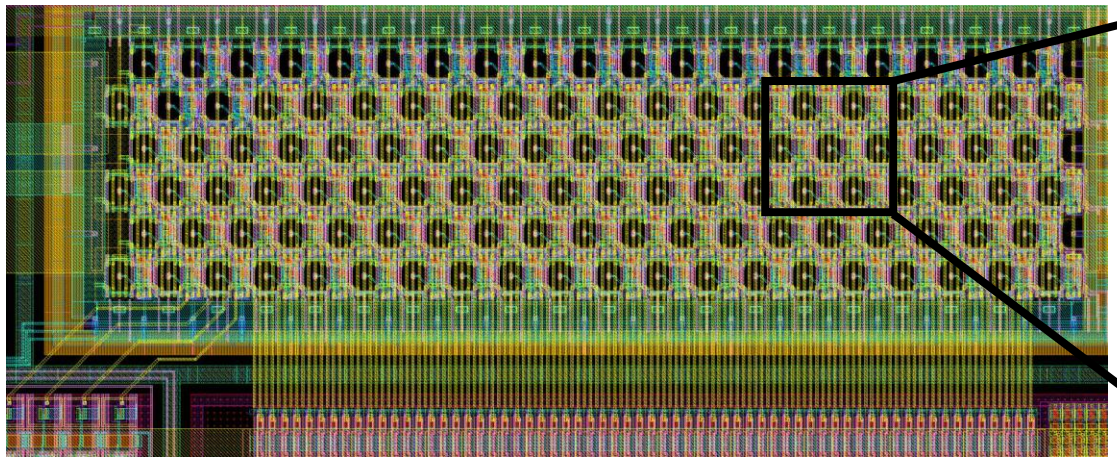
Pitch = 36.6 µm

ATTRACT FASTPIX - sub-nanosecond radiation tolerant CMOS pixel sensors

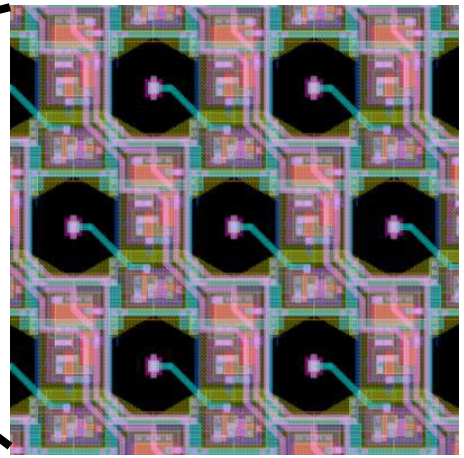
T. Kugathasan et al., https://doi.org/10.1016/j.nima.2020.164461

- Further order of magnitude improvement of charge collection time down to < 100 ps by combination of modifications
- Design of 32 hexagonal sub-matrixes: combination of gap and p-implant, retracted deep p-well, p-well fingers,…

Pixel matrix layout on hexagonal grid:



ZOOM:



- Test-chip to optimize small pixel (down to 8.66µm) sensor design
- Circuitry (180nm) placed in periphery
- 1 LVDS for test-pulse
- 1 LVDS for fast OR of pixel signals
- 2 LVDS for delay lines for pixel position encoding

Status:

- Tests are starting now (Tomas designed boards, Eric already tested them and worked on SW/FW, chips are at CERN)

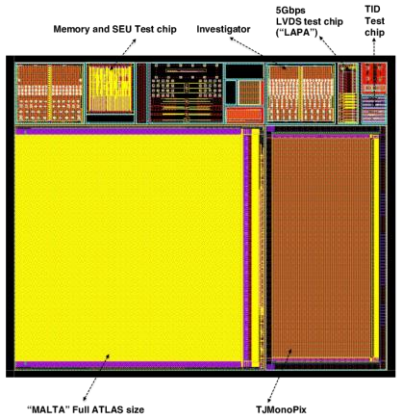
Relevance:

- Optimized small pixel design will be used for TJ 65nm, EP-R&D
- Developed test-setup for such chips (small active area, fast timing) will be used for 65nm TJ prototypes

Summary of chips using developed modifications

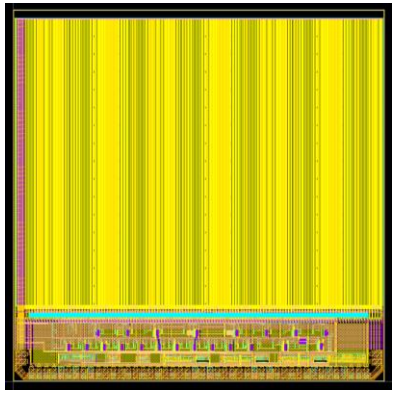
Developed new pixel design solutions implemented in various TowerJazz 180nm chips for different experimental environments:

MALTA/Monopix:



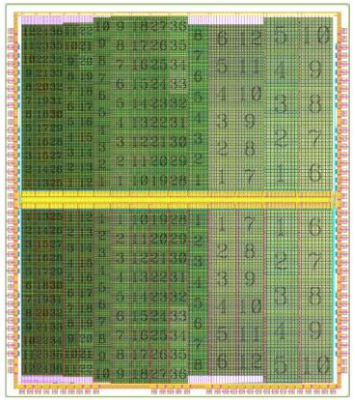
<u>HL-LHC and future pp-colliders:</u>
Increased sensor radiation tolerance

CLICTD:



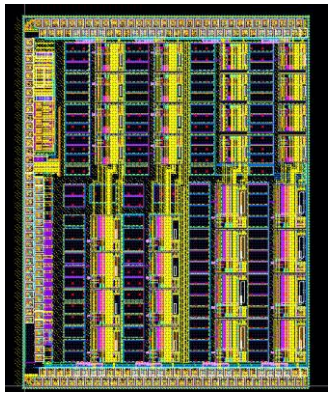
<u>Future e^+e^- colliders:</u>
Improved timing precision and high efficiency for thin sensors

INVESTIGATOR:



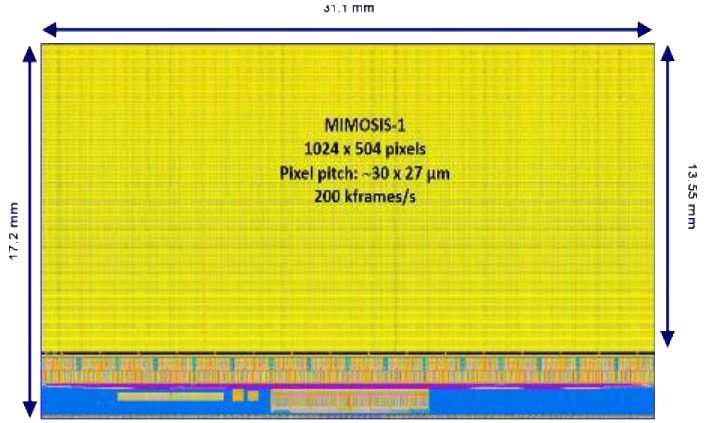
<u>R&D:</u>
Investigation of analogue response

ATTRACT FASTPIX:



<u>Single photon counting (LIDAR):</u>
Improved timing precision

MIMOSIS:



<u>Antiproton and ion research:</u>
Increased sensor radiation tolerance and high efficiency for thin sensors

Summary

We need to modify the concepts from standard planar sensors for this technology:

→ Need to perform 3D finite element electrostatic simulations to develop new concepts for this technology

Parameters are highly correlated and very sensitive to small changes:

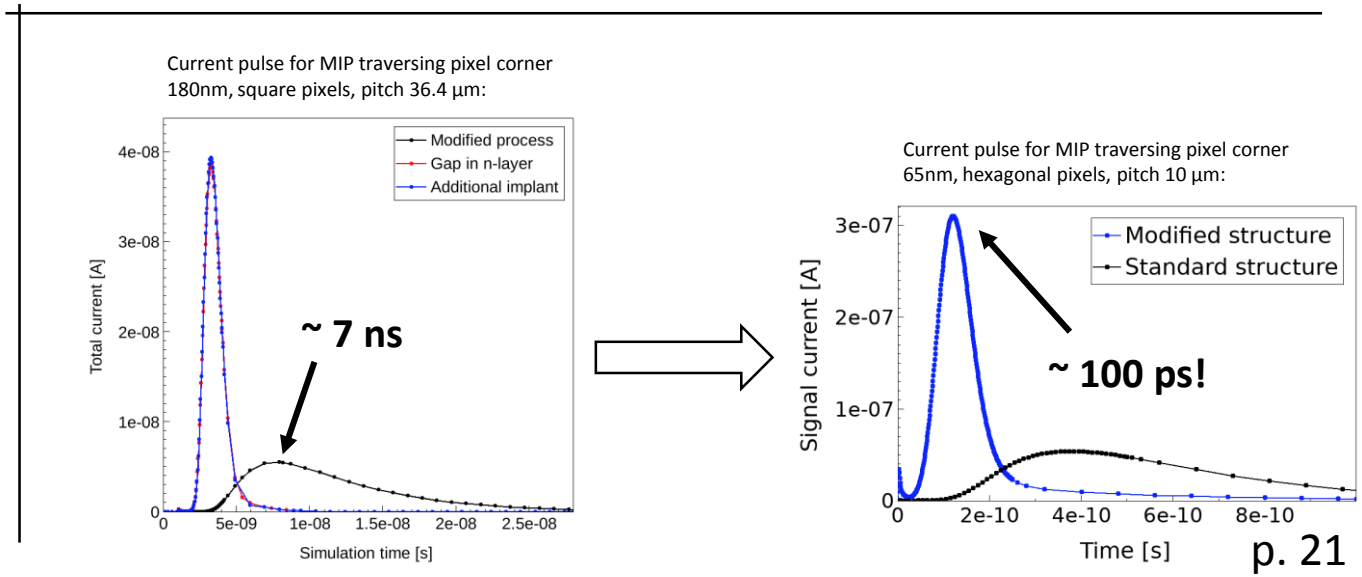
→ Dedicated optimization in 3D TCAD for each geometry needed (very time consuming due to large parameter space)

Modifications developed to increase radiation tolerance, increase efficiency for thin sensors and achieve a more precise time stamping capability:

→ Implemented in various prototypes chips

→ Test results confirm improved performance

Modifications have improved charge collection speed by 2 orders of magnitude.



Outlook

- Summary of main lesson learned in paper (very early stage)

- ATTRACT FASTPIX testing:
  - Validation of simulation
  - Preparation for 65nm TJ

- Testing 180nm CLICTD Cz chips:
  - Expected in beginning of next year

- Evaluation of optimized design with MC Tools:
  - Allpix2 – next talk from Simon
  - Garfield ++

- 65nm TJ pixel design optimizations

Lessons learned from 180nm small collection electrode CMOS technology optimization

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[a]CERN, Geneva, Switzerland

Abstract

Combining the advantages of a monolithic technology with a small sensor capacitance allows for a low detection threshold, precise spatial resolutions, low power consumption, low material budget and reduced production effort and costs. However, the resulting small collection electrode design suffers from reduced speed of charge collection that results in reduced radiation tolerance and limited timing precision. Motivated by this, a design effort based on 3D TCAD simulations was performed, to optimise CMOS sensors with a small collection electrode and increase their charge collection CMOS sensors are developed, aiming to meet all challenging requirements at future

Wishlist for next year's test-beams:

Assembly	Availability	Target beam-time
ACF	Now	10.2020
MightyPix	End 2020	02.2021
FASTPIX	*End 2020*	*02.2021*
CLICTD Cz	*Early 2021*	*04.2021*
Timepix3/CLICpix2 thin FBC active edge	Early 2021	04.2021
EP R&D 65nm test-chip	*Mid 2021 (?)*	*06.2021*
Timepix3 ELAD	Mid 2021 (?)	06.2021

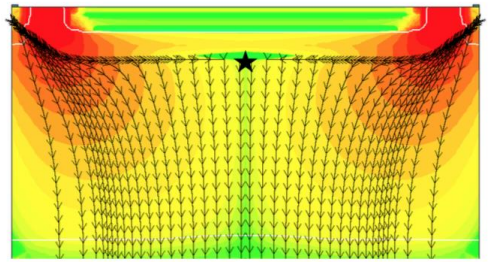

Thanks!

Backup

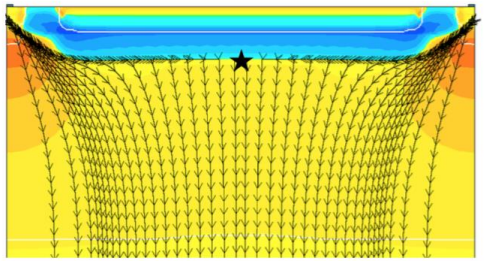
Electric field minimum

Electric field minimum (star symbol) and electric field streamlines (arrow-lines):

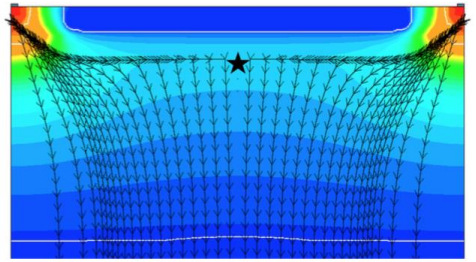
Lateral field:



Field in depth:



Electrostatic potential:



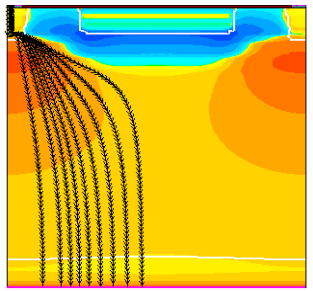
Lessons learned:

Electric field minimum at pixel borders comes from placing the p-wells (circuitry) in the sensor (can not be removed)

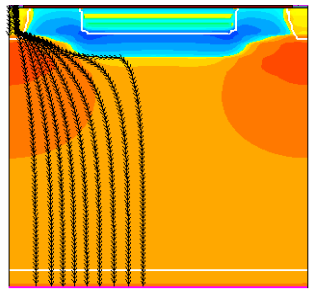
→ Have to minimize/mitigate the pixel edge regions

Example for implication of electric field minimum:

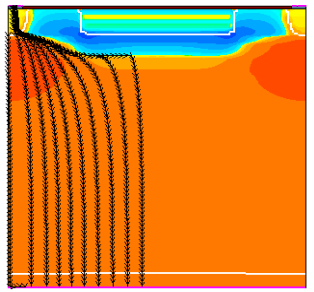
Field in depth (color scale) and electric field streamlines (arrow-lines):



Backside bias = -6V

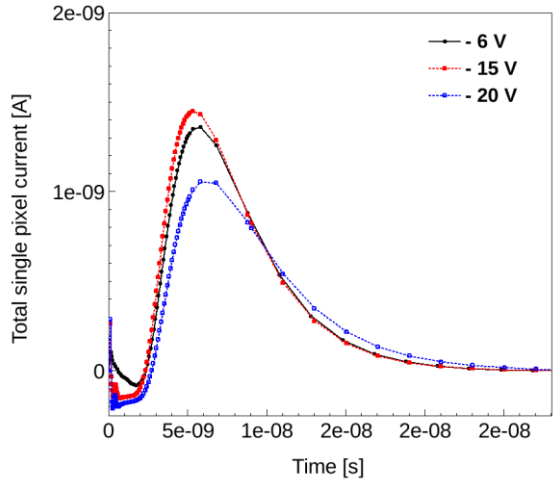


Backside bias = -10V



Backside bias = -14V

Current pulse for MIP traversing pixel corner
for different backside bias after irradiation:



Lesson learned:

Because of the small c-electrode and the electric field minimum, the difference between lateral field and field in depth is important for the charge collection

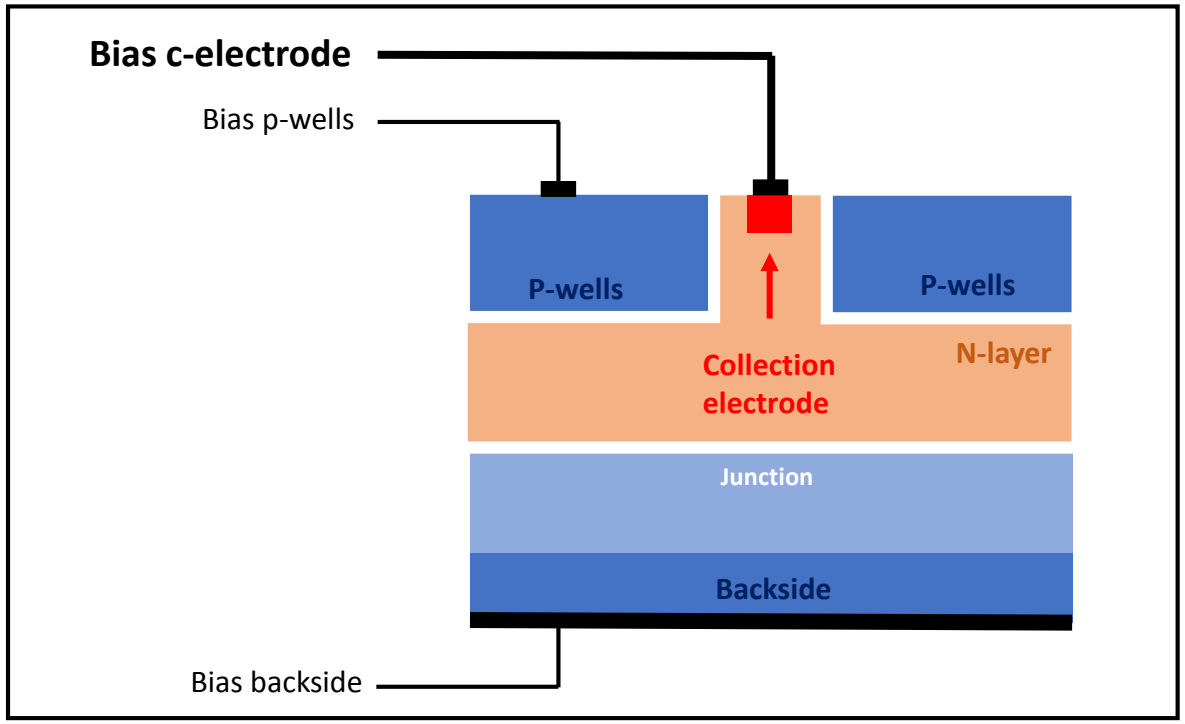
→ Higher absolute field does not always result in a faster charge collection!

Depletion for different c-electrode voltage

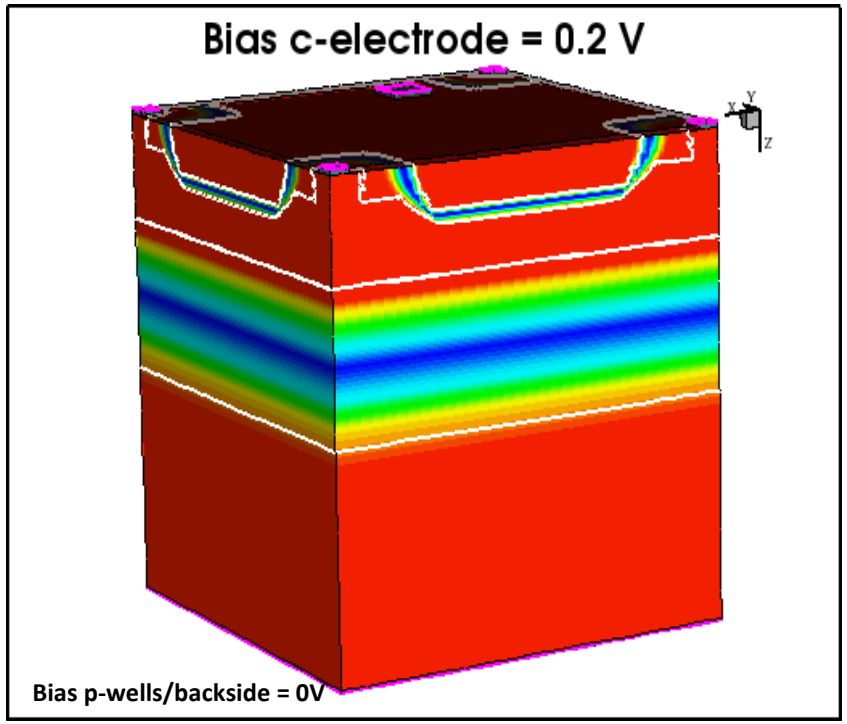
Motivation:

- Depletion around collection electrode ∝ sensor capacitance **∝ noise and threshold**
- **Depletion in depth ∝ signal**

Sensor bias configuration:



Field in depth (color scale) for different p-well bias:



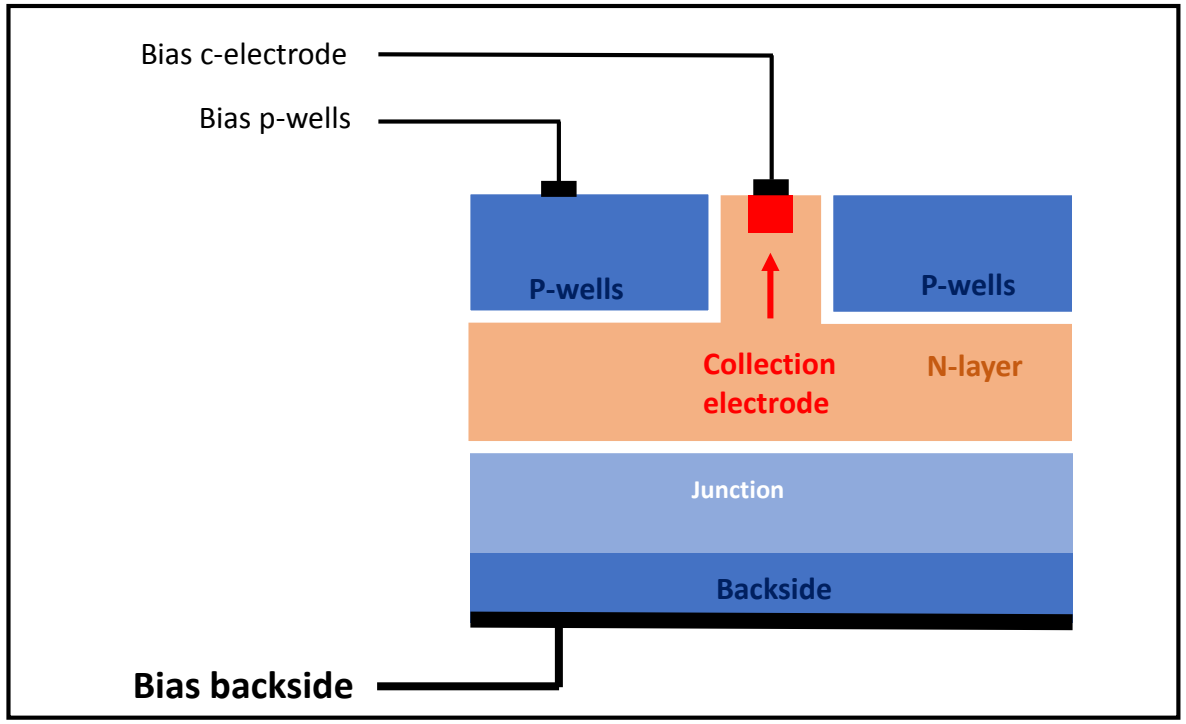
- Max. 0.8V, given by direct coupling to circuitry
- Lesson learned:
  - Bias c-electrode depletes n-layer from p-wells (capacitance) and epi layer from deep planar junction (signal)

Depletion for different backside voltage

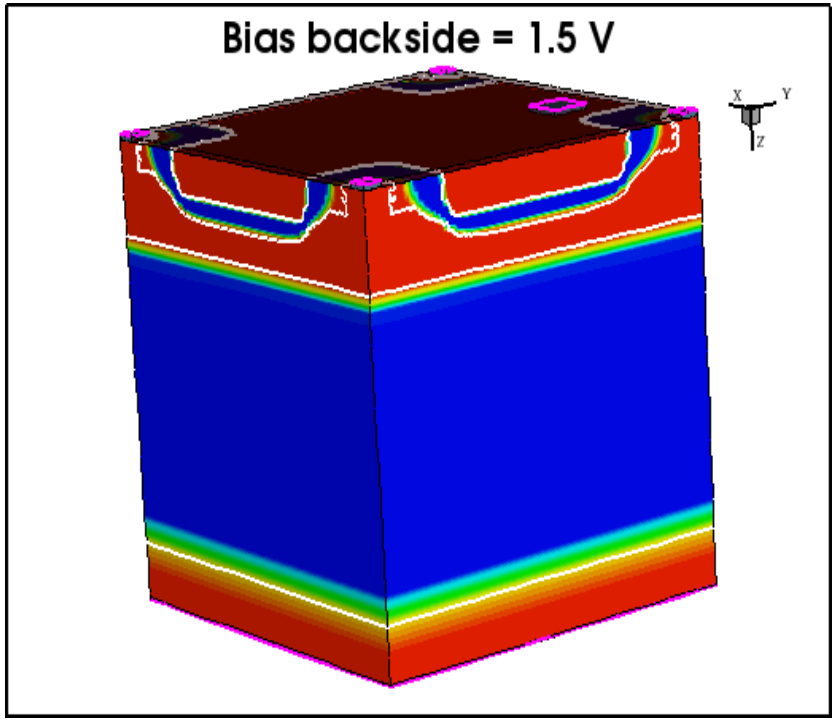
Motivation:

- Depletion around collection electrode ∝ sensor capacitance ∝ **noise and threshold**
- **Depletion in depth ∝ signal**

Sensor bias configuration:



Field in depth (color scale) for different p-well bias:



- Lesson learned:
  - Bias backside depletes n-layer (capacitance) but mostly the epi layer from deep planar junction (signal)