# Highlights from 10 years of CLICdp pixel-detector R&D

Mathieu Benoit

on behalf of all the collaborators over the years







**BROOKHAVEN SCIENCE ASSOCIATES** 

## **Outline**

- Early years
  - Conceptual Design Report studies
  - First experimentation with Timepix
- Towards a detector model
  - Cooling simulation
  - Powering and power pulsing
  - · Petals and whirlwinds!
- First prototypes: Towards thin pixel sensors
  - Timepix prototypes with thin sensors
  - The CLICpix ASIC
  - Simulation studies





## **Outline**

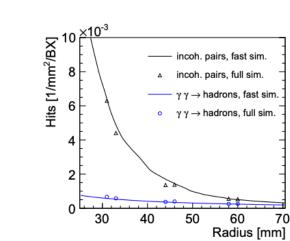
- Pixel detectors : The next generation
  - Active-edge prototypes with Timepix3
  - First CLICPix prototypes
  - TSV studies
  - CLICpix2
- Developing tools
  - Allpix<sup>2</sup>
  - CaRIBOu, peary
  - The Timepix3 Telescope
- Beyond bump bonding
  - CCPD prototyping
  - Monolithic sensors: SOIPix, ATLASpix and CLICTD

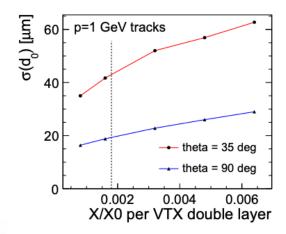




## Early years: The Conceptual Design Report

- Elaborated in 2010-2011, the <u>CLIC Detector and</u>
   <u>Physics Conceptual Design Report</u> set the course for the CLIC Vertex and Tracker detector R&D
  - The primary technological challenges to be addressed are in the power delivery, readout, interconnect, and low-mass mechanical construction.
  - Sensor thinning and ultra low-mass material construction will be necessary to stay within the material budget constraints implied by the physics goals outlined
  - Interconnect technologies and pixel connectivity must be studied and optimised.
  - we note the ongoing R&D on CMOS MAPS technologies, where several approaches are being pursued
  - The need for timing information implies a high-resistivity sensitive medium and full depletion, with advanced readout functionality for the individual pixels in the array. (...) one can think of several developmental roadmaps that can lead to a pixel detector technology for CLIC.





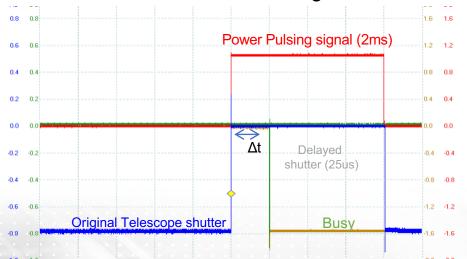
(b) Material in barrel pixel layers



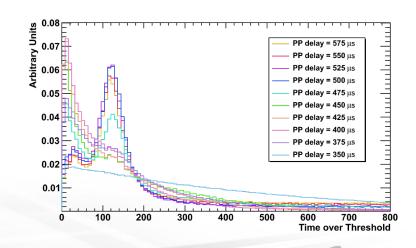


## First experimentation with Timepix (2011-2012)

- Initial effort to start the experimental side of R&D focused on Timepix, the ASIC available at the time
- With a scope, an assembly and a source, we demonstrate proof-of-concept of power pulsing the assembly
- We later hook up to the Timepix LHCb telescope to demonstrate that with tracking



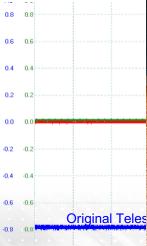






# First e

- Initial effort to selection for the selection for the
- With a scope, and demonstrate period
  the assembly
- We later hook to demonstrate

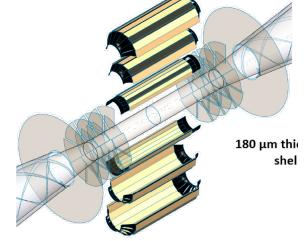


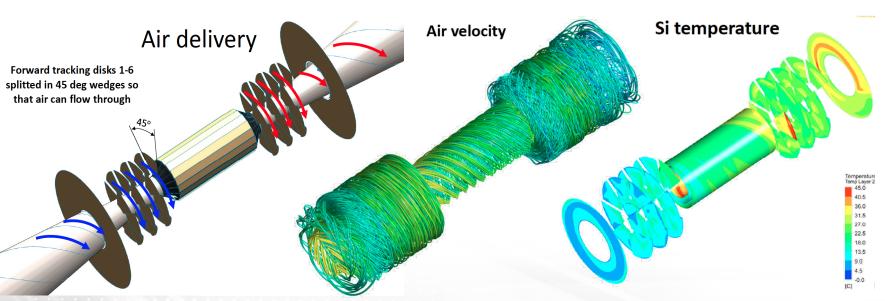


## Mechanical and Cooling simulation

From the insight of the CDR, study of mechanical integration of air cooling in the vertex detector were started to evaluate how to evacuate the dissipated energy from the tracking volume





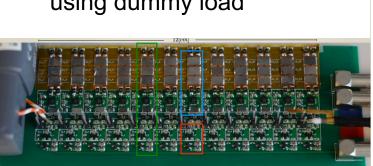


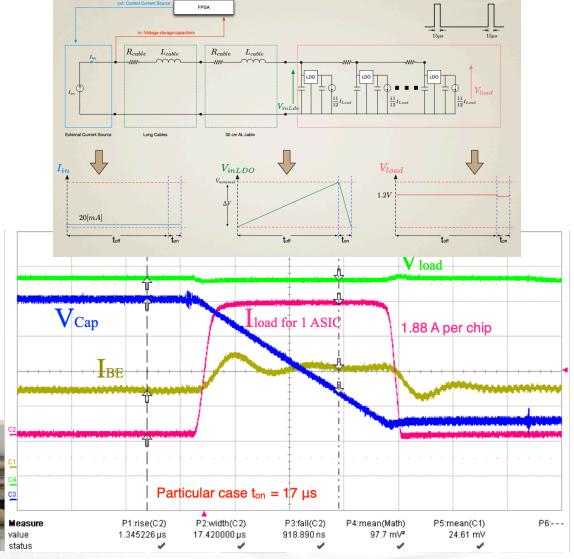


## Powering and power pulsing

To deliver pulse power in a a pulsed detector floating in a strong magnetic field, a new powering scheme based on LDO and super capacitors was studies to demonstrate the feasibility of our concept

- Local storage of energy required for data acquisition in super-capacitor
- Low steady current in powering line
- Demonstrated in laboratory using dummy load



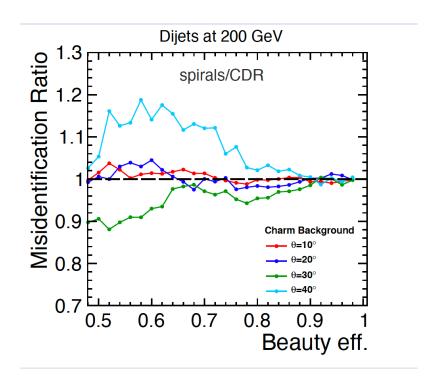






## Petals and whirlwinds!

## CLIC\_SiD\_spirals Allows airflow cooling with the same barrel as the CDR geometry. Material Budget [X/X] 0.05 0.04 0.03 0.00 CLIC\_SID\_CDR CLIC SiD spirals



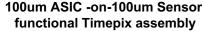
CLIC specific condition lead to the modification of existing detectors and optimize them. This was first steps towards a detector model specific to CLIC



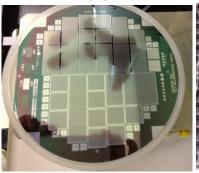


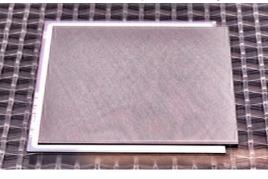
## First pixel sensor prototypes: Timepix sensors

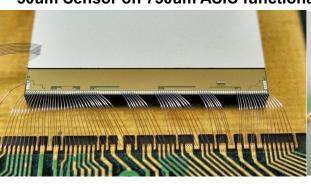
100 um thick Sensor wafer

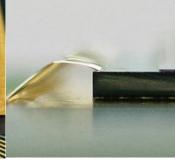


50um Sensor on 750um ASIC functional Timepix assembly





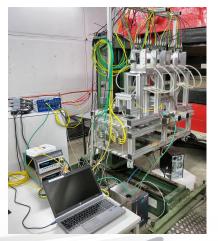




Thin Planar sensors were one of the goals of the Vertex detector R&D. Our efforts lead to the production of very thin assemblies with sensors from Advacam, Micron Semiconductor with sensor thickness down to 50 um

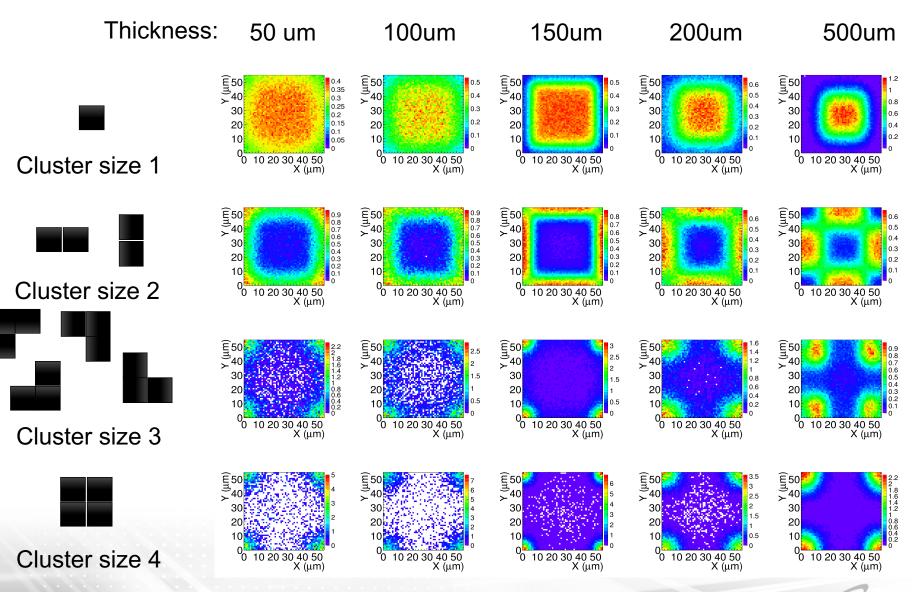
We produced the first 100um on 100um Timepix assemblies, a record at the time! We then extensively characterize the sensors at DESY using the EUDET Telescope







## Test beam !!







### A newcomer ...

Meanwhile... A certain I. Peric in Mannheim was playing with a new kind of sensor called **CCPD in HV-CMOS technology**. He agreed to add 1 row of pixels matching Timepix footprint on the CCPDv2 prototype

After designing a custom board, we had one assembly glued ...

It was connected, and we could see the pixels firing when we brought the Sr90 source.

We took a video and went for coffee...

The sample never worked again. It is nice nicely displayed on my office desk ©

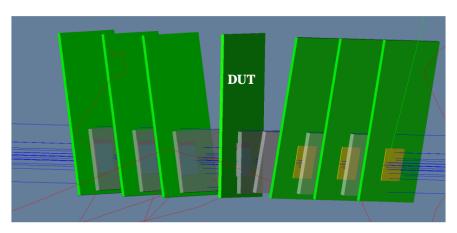


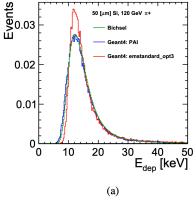




## Simulation studies

 After a successful first round of production of thin sensor prototype, with large amount of data on disk, A lot of work was done on optimizing simulation models using Allpix and TCAD simulation to project performance to smaller pixels





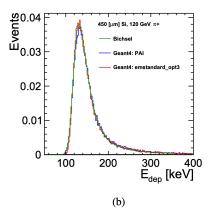


Figure 5.1: Energy-loss distribution in (a) 50  $\mu$ m and (b) 450  $\mu$ m thick silicon sensors due to the passing of 120 GeV pions ( $\pi^+$ ) comparing the Bichsel model and GEANT4 using the PAI and the emstandard\_opt3 physics lists.





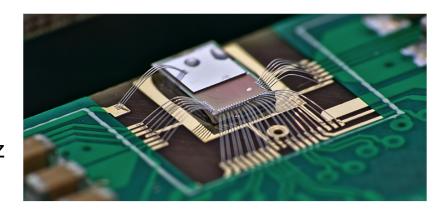
## **ASIC Development : CLICpix**

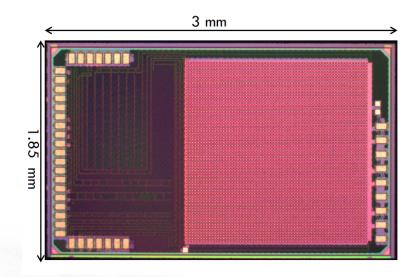
#### Main features:

- Small pixel pitch (25 μm),
- Simultaneous TOA (4 bits) &TOT (4 bits) measurements
- 100MHz measurement clock and 320 MHz readout clock
- Power pulsing
- Data compression
- Both pulse polarities can be handled

#### **Demonstrator CHIP:**

- commercial 65 nm CMOS technology
- array of 64x64 pixels
- The Krummenacher architecture, with a single ended preamp, a two stage discriminator and a 4-bit DAC









## The next generation: Timepix3

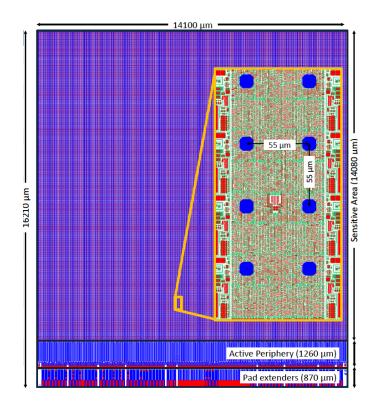
Timepix3 ASIC was received at CERN beginning of 2014. it represents a revolution w.r.t. the previous generation:

- ~10 ms readout time -> Data driven @ 10Gb/s
- TOT or TOA -> TOT(10bits) + TOA
- Proprietary DAQ -> DAQ developed by NIKHEF and CERN, full control of hardware + software

A Multi-Project Wafer common to ATLAS, UNIGe and CLIC to investigate further thin active-edge assemblies was produced with Advacam

15 wafers iproduced: 5x 50um, 5x100um, 5x200um Timepix3 and CLICpix compatible sensors with 20 and 50um active-edges

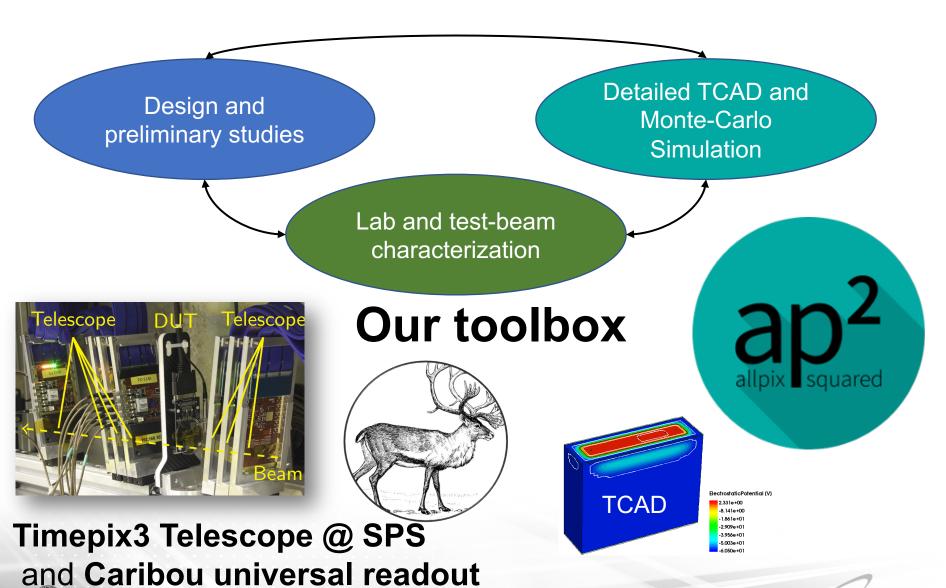
Possibility to flip-chip to 50um thin ASIC with TSV from a parallel project with LETI using Timepix3





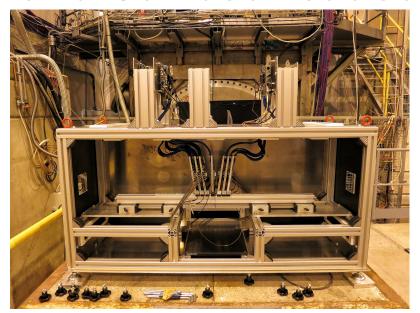


## Vertex and tracking R&D cycles



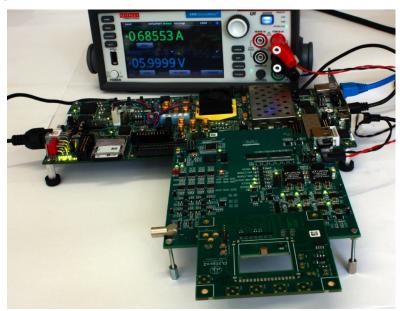
ENERGY

## Tools: The CLICdp Timepix3 Telescope and Caribou readout





- 7 x Timepix3 telescope planes
- Continuous readout
- ~1.2ns time resolution on tracks
- ~2 µm resolution at the DUT
- Flexible mechanics with rotation stages for angle study



### The CaRIBOu universal readout framework

- Multi-chip modular r/o framework
- Stand-alone system based on Zynq SoC running YOCTO Linux
- Peary generic DAQ software
- Generic CaR board for powering and monitoring of DUT
- Implementation for CLICPix, CCPDs, ATLASPix, FEI4, H35DEMO and more



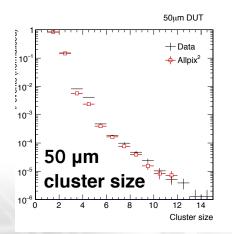
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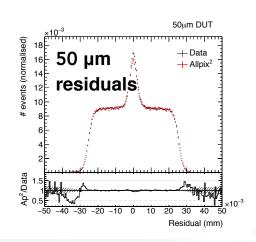
## Tools: Allpix<sup>2</sup>

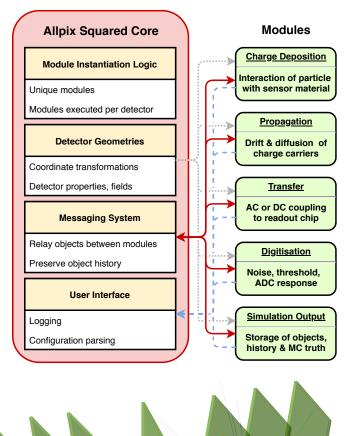
CERN.CH/allpix-squared

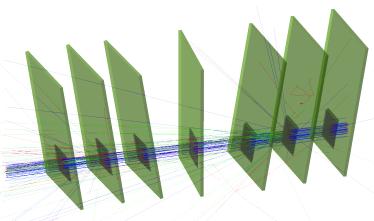


- A Modular, Generic Simulation Framework for pixelated Detectors
  - Generic simulation of pixel, strip detectors
  - Simple text base description of the geometry, simulation parameters
  - Charge transport and TCAD Electric Field import facilities
  - Visualisation and digitisation
  - Output in popular formats (EUDET,PROTEUS, Corryvreckan, etc..)







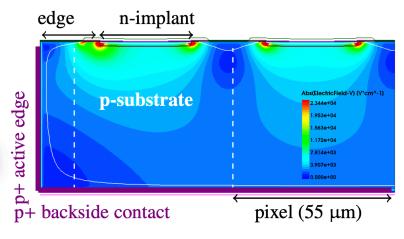


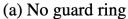


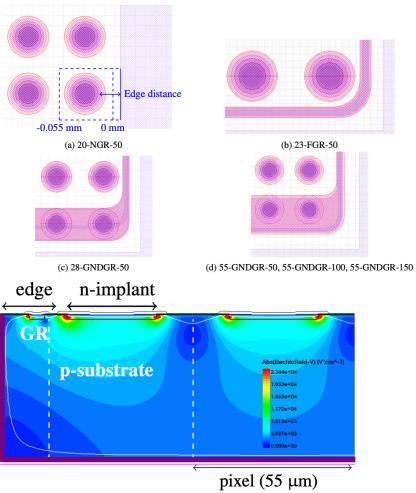


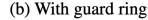
## Active-edge planar sensors with Timepix3

In view of the new sensor production, extensive TCAD simulation studies were also performed to optimize the submitted designs



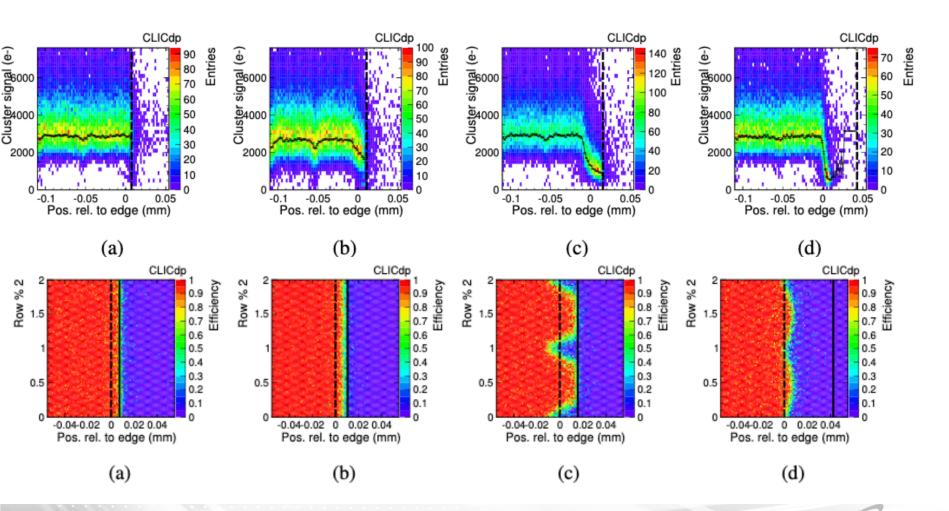








## Timepix3 Active-edge measurements





## First results with 25um pitch

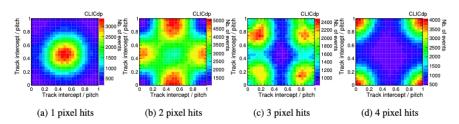


Figure 3.33: Track intercept within the pixel cell of the 200 µm planar CLICpix assembly for different cluster sizes.

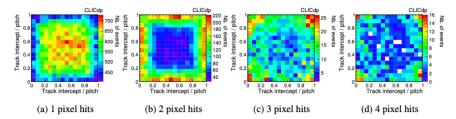
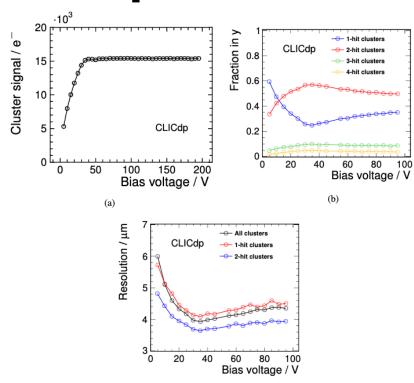
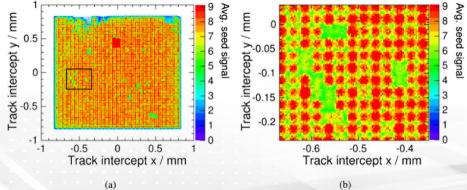


Figure 3.34: Track intercept within the pixel cell of the 50 µm planar CLICpix assembly for different cluster sizes.



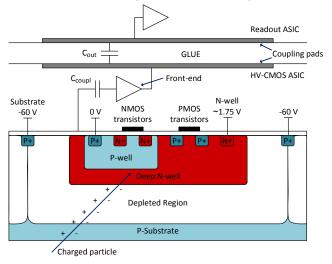




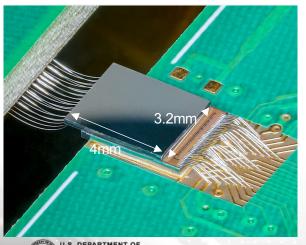
### Capacitively-Coupled Pixel Detectors (CCPD)

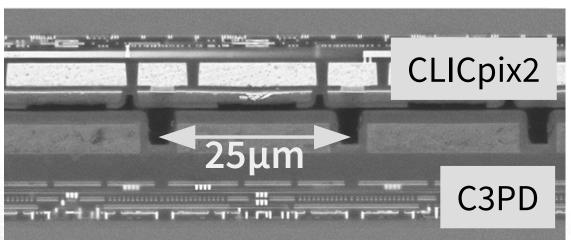
### (CCPDv3)C3PD+CLICPix(1)2

- 2 sensors, CCPDv3 and CLIC CCPD (C3PD) were designed in ams aH18 HV-CMOS technology
  - (64x64) 128x128, 25x25 μm<sup>2</sup> pixels
  - Substrate resistivity from 20 to 200 Ωcm
- First amplification layers integrated in sensors to provide large signal at output
- I<sup>2</sup>C 2-wire slow-control interface (C3PD)
- Coupling with ASIC done through a very thin layer of glue forming a capacitor (Low mass!)
  - Glueing method developed to using flip-chip assembly to acheive down to 100 nm glue layers
  - Fast prototyping method wrt planar sensors



Nucl. Instrum. Methods Phys. Res., A 823 (2016) 1-8 PhD Thesis M. Buckland CERN-THESIS-2018-114 I. Kremastiotis 2017 JINST 12 C12030 M Vicente et al., CLICdp-Note-2017-003

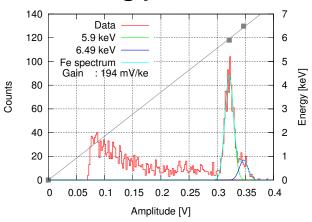


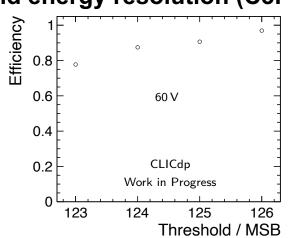


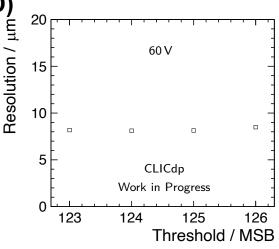


### Capacitively-Coupled Pixel Detectors (CCPD)

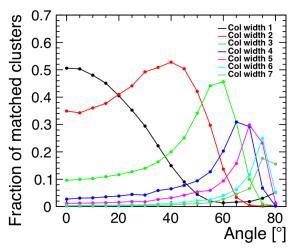
### Tracking performance and energy resolution (C3PD)

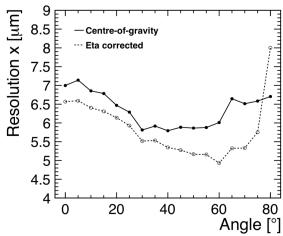


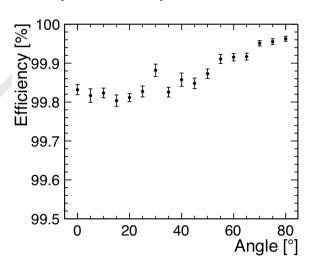




### Tracking performance versus track angle of incidence (CCPDv3)









**CERN-THESIS-2018-114** 

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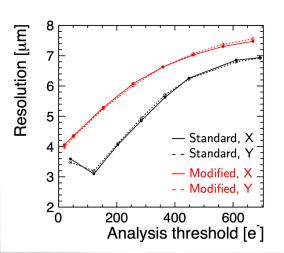
### **Small-Fill factor CMOS sensors**

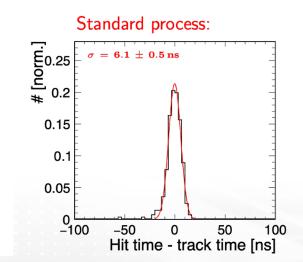
CMOS electronics integrated in **p-well separated** from collection electrode:

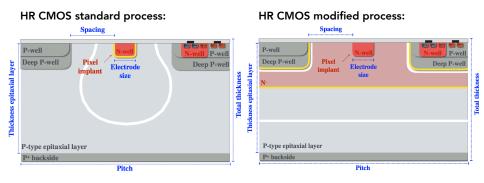
- Minimisation of diode size
- Minimisation of sensor capacitance down to ~ fF (large S/N)
- Process modifications to achieve full lateral depletion (W. Snoeys et. al)
- Further modifications proposed to improve timing and radiation hardness, see <u>Monday</u> presentation by M. Munker

### Investigator analogue test-chip:

 Various pixel layouts implemented in different pixel layouts, electrode to pwell spacings

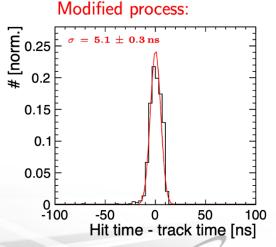






#### Test-beam results for both process variants:

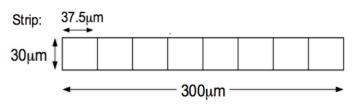
- Spatial resolution ~ 7 μm for threshold values of ~400e
- Fully efficient operation to threshold values below ~400e
- Timing resolution ~ 6 ns (limited by readout)





### Small-Fill factor CMOS sensors: CLICTD

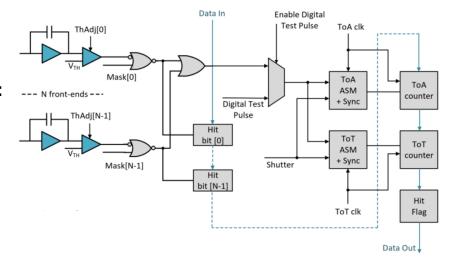
Promising results of 180 nm HR CMOS imaging process trigger design of fully monolithic CLIC tracker chip:



- Super-pixel segmented in high granular collection diodes to maintain fast - - charge collection while reducing digital logic
- Super pixel size of 30 μm x 300 μm
- Diode size of 30 μm x 37.5 μm

#### Diode discriminator outputs combined in 'OR' gate:

- 8-bit ToA and 5-bit ToT measurements
- Storage of hit-pattern
- 100 MHz clock for 10 ns time binning



#### Different operation modes:

- 8 bits time stamping information (ToA) + 5 bits energy information (ToT)
- 13 bits time stamping information (ToA)
- 13 bits photon counting (number hits that are above threshold)

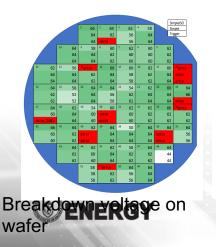


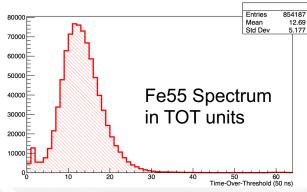


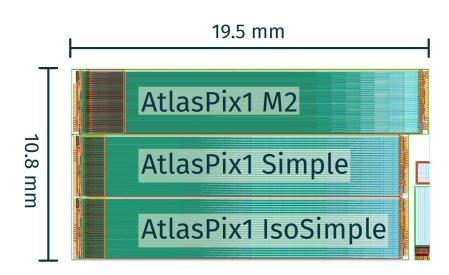
## Large Fill-Factor CMOS sensors

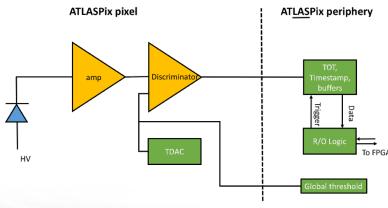
Implementation of fully **monolithic** sensors in ams aH18 process using high-resistivity wafers

- 180nm HV-CMOS Engineering run on 20-200 Ω cm substrate
- Thinned down to 60 μm
- 130x40 μm² pixels, 25x400 pixels
- 6 bit TOT and 10 bit TOA (up to 16 ns)
- Uniform breakdown across wafers at 60-85V
- Threshold down to 600e, 120e dispersion
- Full length column sensor (1.9cm)
- Trigger-less readout
- Serializer, PLL, High-Speed data transmission (1.25Gbps, aurora 8b/10b)
- Initially design for ATLAS, Radiation hard up to >1x10<sup>15</sup>n<sub>eq</sub>/cm<sup>2</sup>, 100MRad
- Close to CLIC Requirements









I. Peric et al., A high-voltage pixel sensor for the ATLAS upgrade, Nucl. Instrum. Meth. (2018), in press, DOI: 10.1016/j.nima.2018.06.060.

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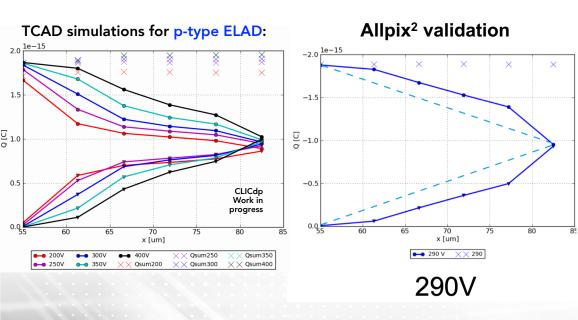
## **Enhanced Lateral Drift sensors (ELAD)**

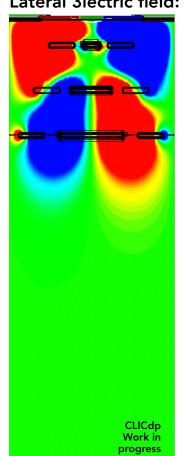


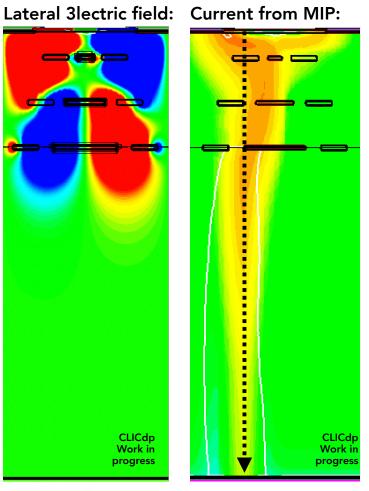


Concept to improve spatial resolution for thin sensors, H. Jansen (DESY/PIER):

- Deep implants to shape electric field lines in sensor
- Suggestive epitaxial layer grow and implantation
- Increased "linearised" charge sharing









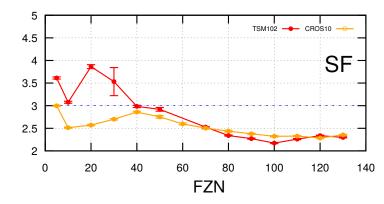
Patent DE102015116270B4

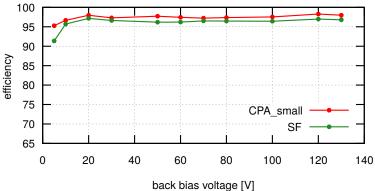
## **SOI** sensors

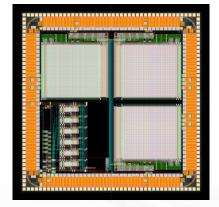
- Monolithic integration with sensor electronics separated from high-resistivity substrate by Oxide layers
- Cracow SOI test chip in 200nm LAPIS SOI process, differ parameters:
  - >=  $30 \times 30 \mu m^2$  pixels
  - · single-SOI and double-SOI wafers
  - · different readout schemes implemented
- First test beam results for 500 µm thickness
  - SOI HR-CMOS:  $30x30 \mu m^2$  pitch, **Efficiency > 97%**,  $\sigma_{SP}$  =  $2\mu m$

#### **CLIPS: CLICPixel SOI in production**

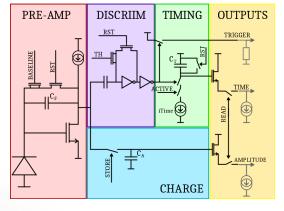
- 4.4 × 4.4 mm (previous 2.9 mm)
- Targets
  - spatial resolution <3 μm</li>
  - time resolution <10 ns</li>
- Analog charge and time information in storage capacitors in each pixel
   --> no need for fast clock distribution into matrix
- Snapshot analog readout between bunch trains with external ADC
- Timing reference base on tuned current source







esolution Y [um]















A lot of great collaborators!

## Conclusion

- Work for the CLICdp vertex and tracking R&D over the last 10 years has been tremendous, thanks to the work of our brilliant collaborators
- Collaboration with Medipix/Timepix Collaboration has been key to achieve our objectives
  - Timepix studies
  - Timepix3 Telescope
  - CLICpix,CLICpix2, C3PD, CLICTD
- Tools developed by the collaboration will be used for many more years
  - Allpix2, CaRIBOu and Peary, Coryveckran etc ...
- I want to thank everyone involved for such a great work and for your company over the last 10 years



