Birmingham Instrumentation Laboratory for Particle physics and Applications
BILPA

Towards a Reconfigurable CMOS Sensor suitable for Outer Tracking, Pre-shower and Digital EM Calorimetry at Future Facilities

UNIVERSITY OF BIRMINGHAM

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(CERN, 9/10/2020)

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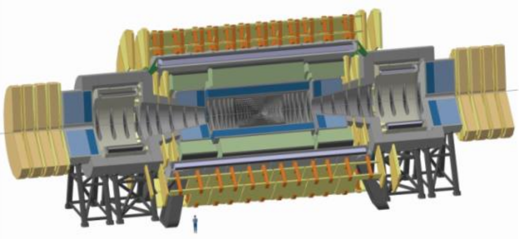
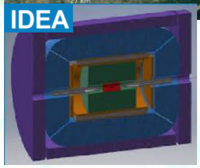
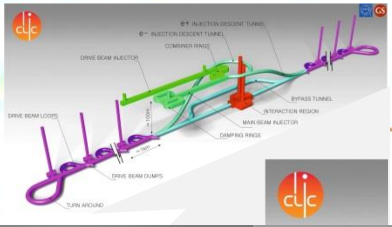
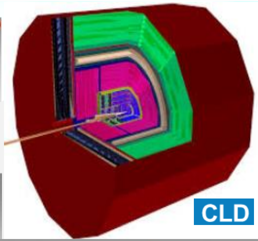
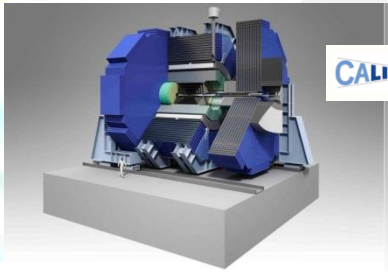
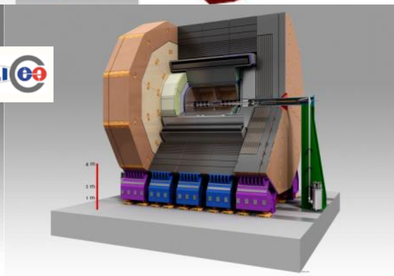


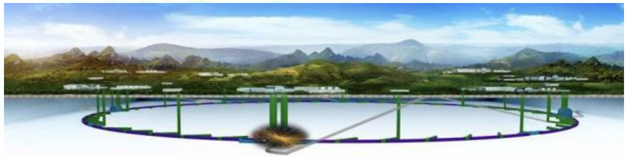


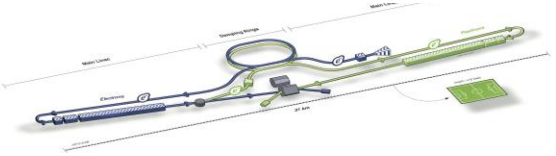


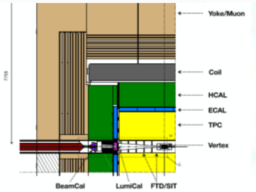










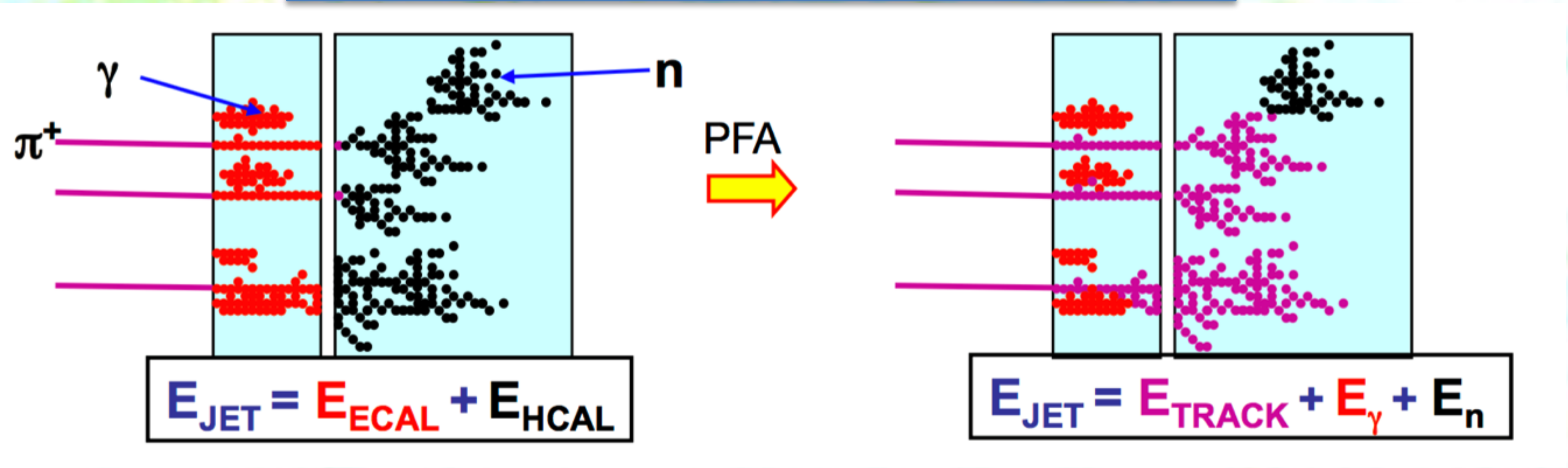


Introduction: Particle Flow

- **High granularity calorimetry offers the possibility of using Particle Flow techniques to make best use of all detectors to measure jet energies**
- **Use of a very compact EM calorimeter (particularly if intended before the solenoid) also reduces the volume (and therefore cost) of all detector systems outside it.**

Idea: for each individual particle in a jet, use detector with best energy/momentum resolution

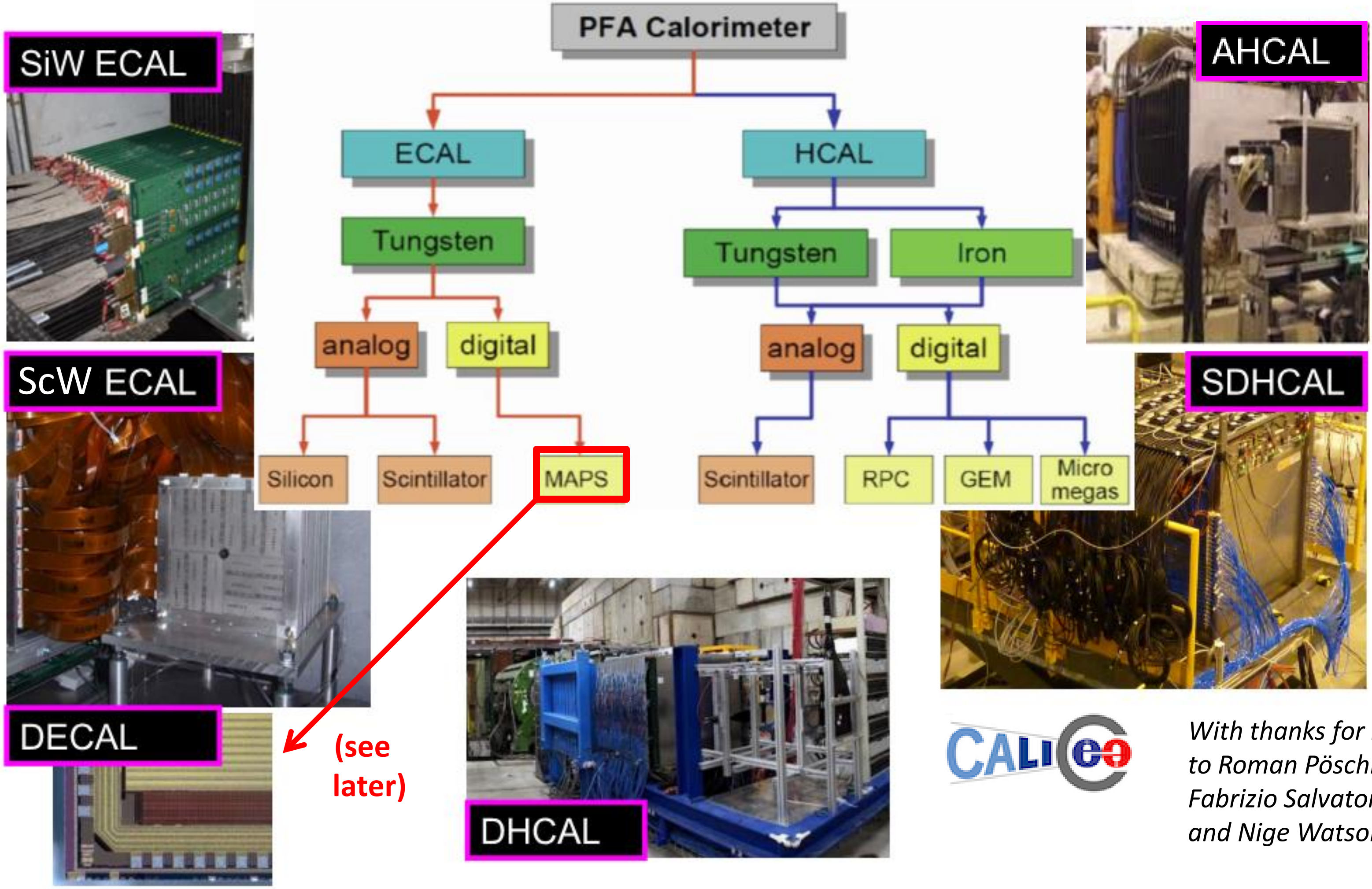
Charged tracks = Tracker
e/photons = ECAL
Neutral hadrons (only 10%) = HCAL



D. Barney, https://indico.cern.ch/event/718124/

Introduction: CALICE

- **The concept of SiW calorimetry has long been under consideration as a possible option within the CALICE collaboration as offering unprecedented granularity for PFA and is the focus of extensive prototyping and test beam activities**



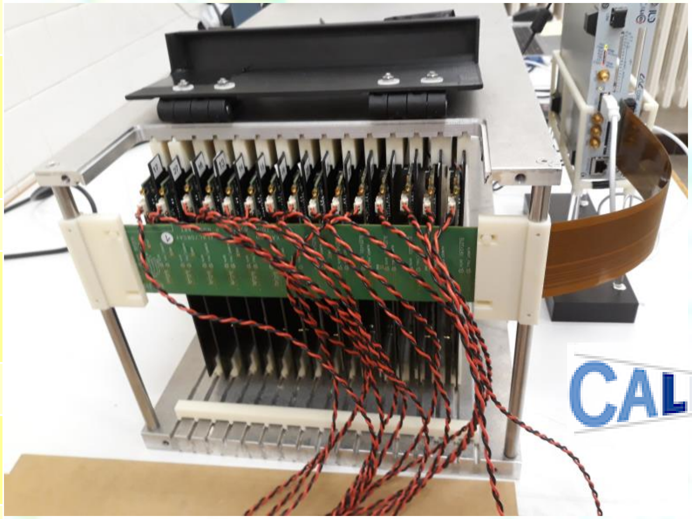
With thanks for help to Roman Pöschl, Fabrizio Salvatore and Nige Watson

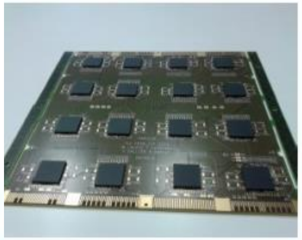
CALICE: SiW EM Calorimetry

Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV11	7 units	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 $(12)_{Trig.}$ 6–8 % masked
1st technological ECAL	2018	SLABvFEV11 & FEV13 SK2a+ Compact stack Long Slab	SK2 & SK2a (⊃timing) 8 ASUs	Improved S/N Timing...
1st working COB	2019	FEV-COB	2×1/4 ASUs	

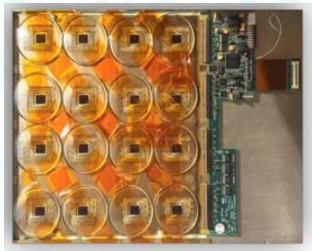
CALICE SiW ECAL Test Beam

- culmination of 10 years of prototyping
- Integrated front-end and digital electronics
- 15 layers with 15360 channels





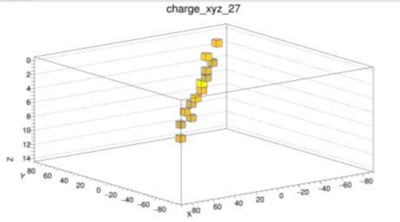
FEV10-12



FEV_COB

FEV13

Image of cosmic track



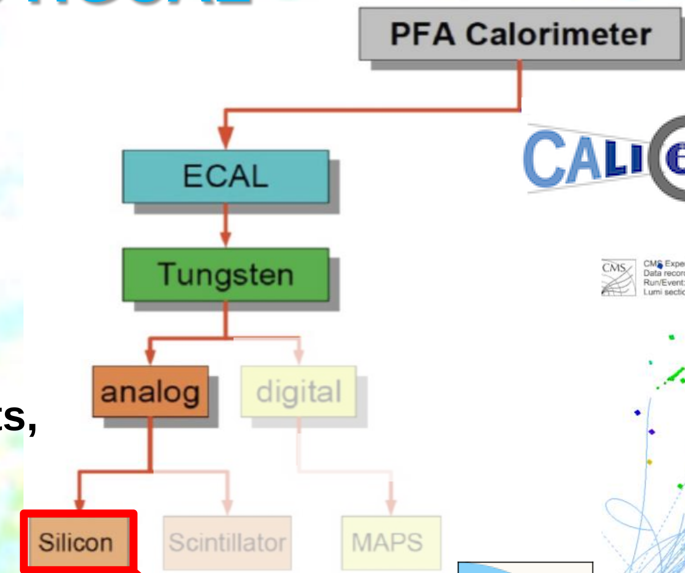
DESY Test Beam later this year

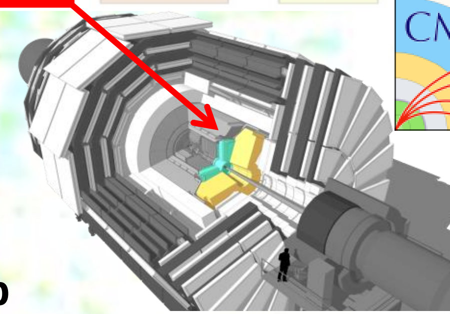
CMS HGCAL

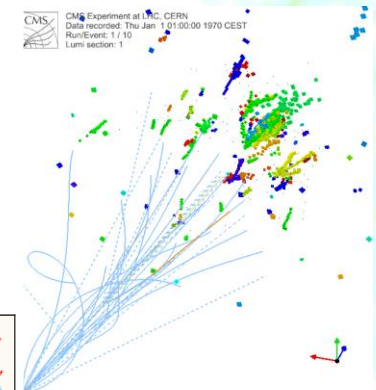
- **The activities being discussed here grew out of ideas within CALICE, but initially with a view to FCC-hh, inspired also by developments within CMS for Phase-II**
- **Given the very high radiation environments, CMS is building the High Granularity Calorimeter (HGCAL) as the upgrade path for their forward calorimetry at HL-LHC**
- **The HGCAL will have ~600m² of silicon sensors (~500m² of scintillators) with 6M Si channels, 0.5 or 1.1 cm cell size and overall ~27000 silicon modules**
- **The ECAL has 28 layers with Si + Cu/CuW/Pb absorbers giving 26 X_0 and ~1.7λ**

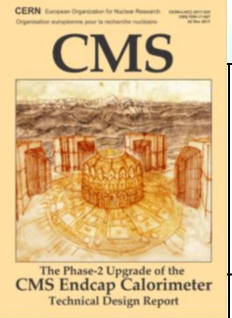
1.3, 1.4	Silicon sensors and modules	26 514
	GRAND TOTAL	67 153

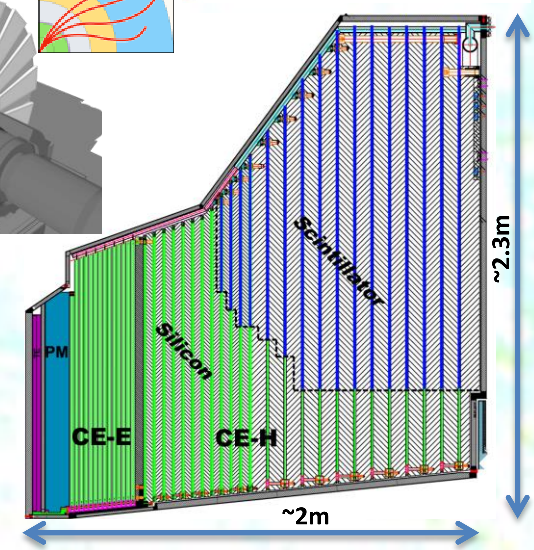
- **Silicon module costs ~4CHF/cm²**







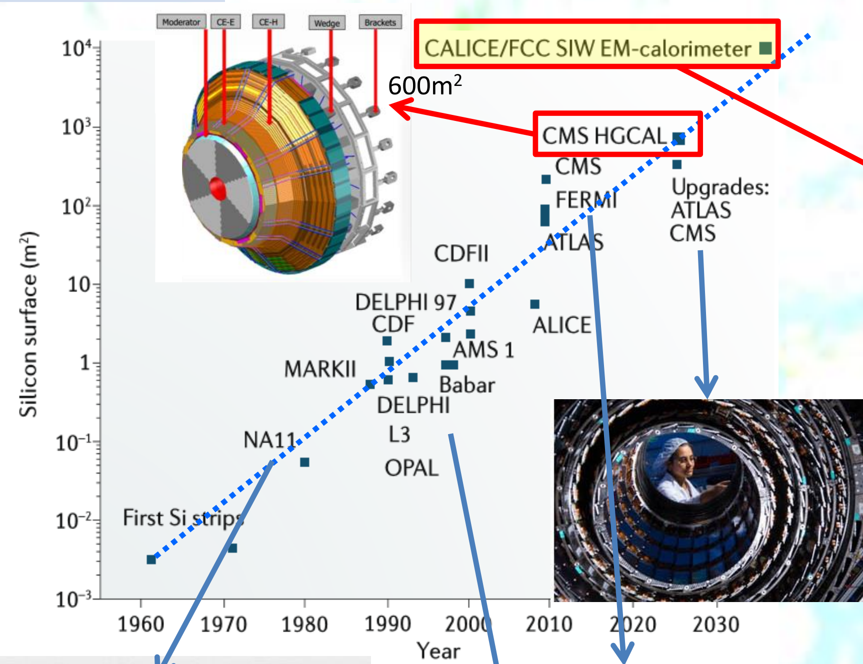


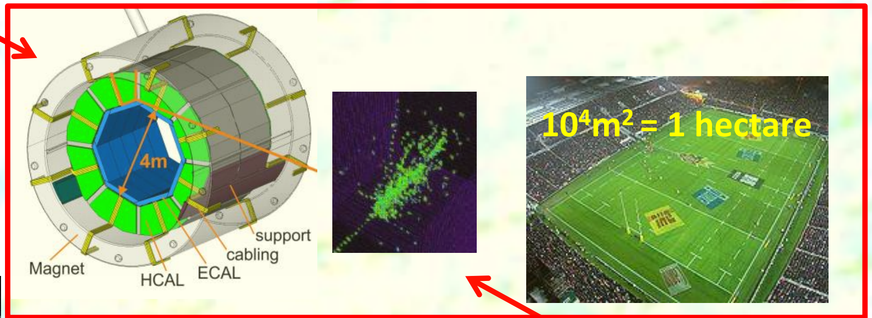


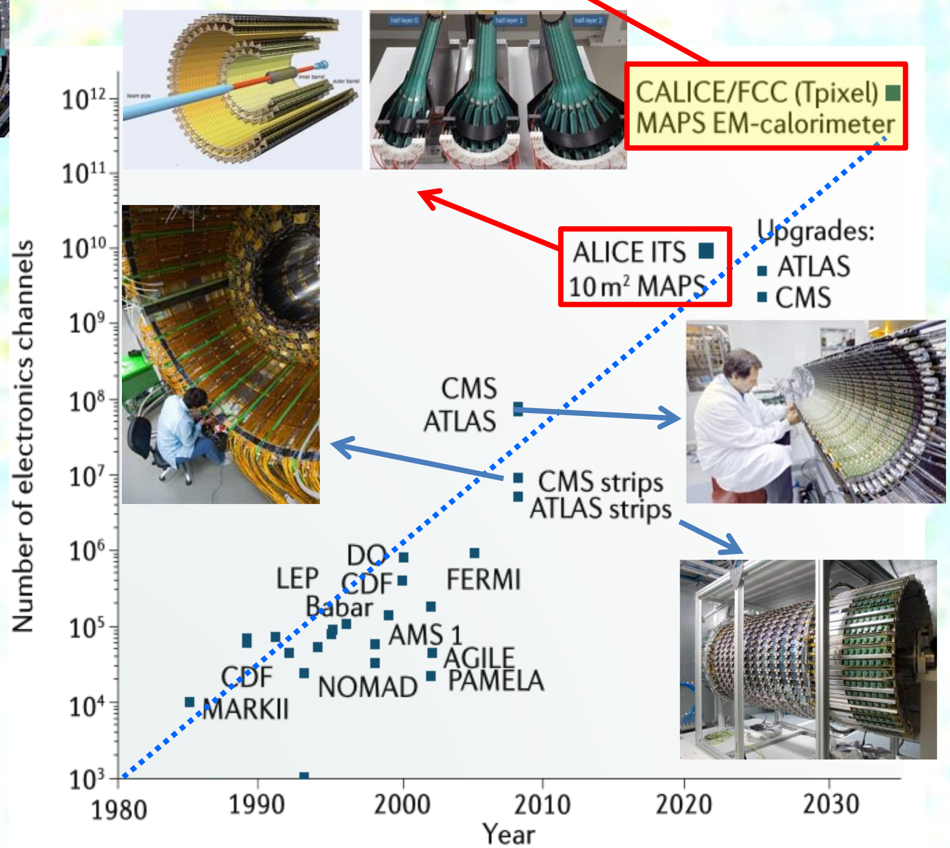
CE-E: 1.7λ Cu/CuW/Pb absorbers

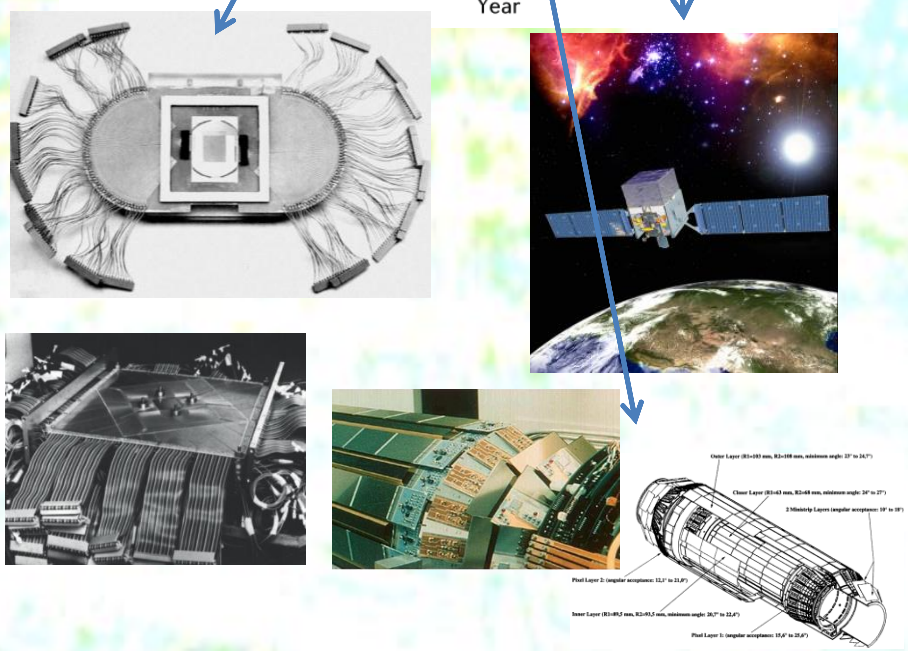
D. Barney, https://indico.cern.ch/event/718124/

Historical Development of Silicon Sensor Arrays



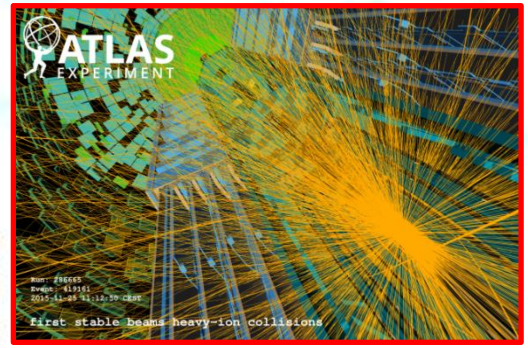


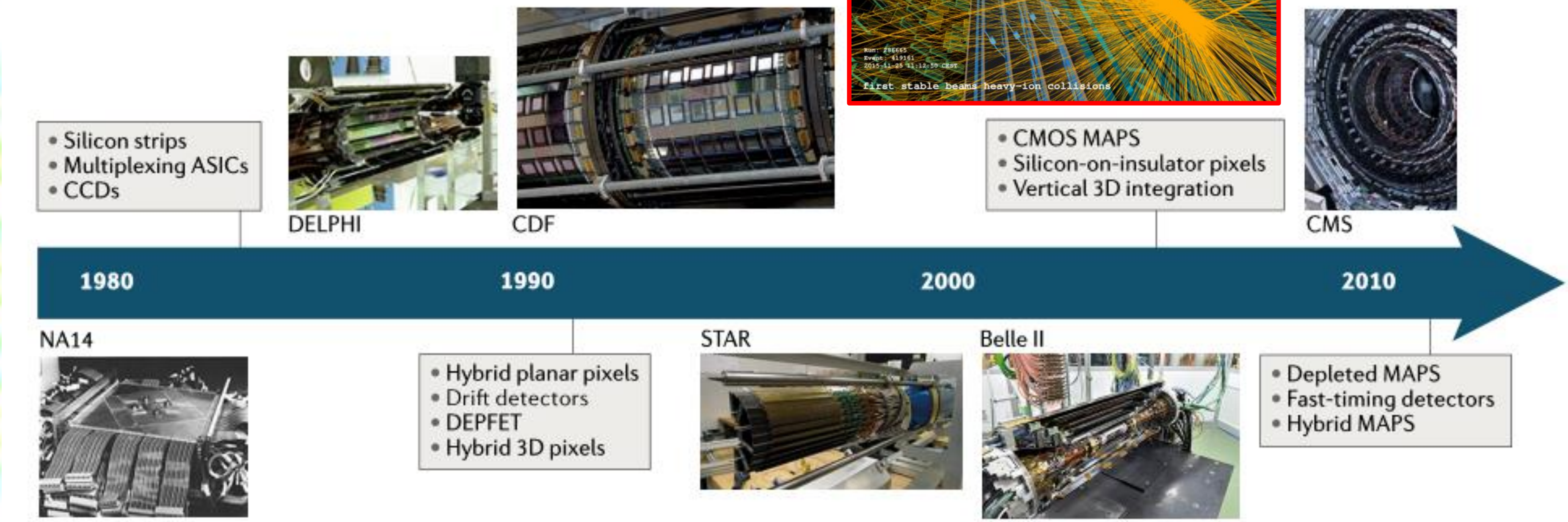




Silicon Sensor Technology Developments

Many different silicon detector technologies for particle tracking have been developed over the last four decades.





Applications of silicon strip and pixel-based particle tracking detectors - Nature Reviews Physics - https://doi.org/10.1038/s42254-019-0081-z Allport2019ER

What is remarkable is that <u>every decade</u> the instrumented areas have increased by a factor of 10 while the numbers of channels in the largest arrays have increased by a factor of 100.

This despite other specifications for readout speed, spatial resolution, reduced multiple scattering (minimal total material including cooling and services) and radiation hardness also becoming much more demanding

Commercial Microelectronics Evolution

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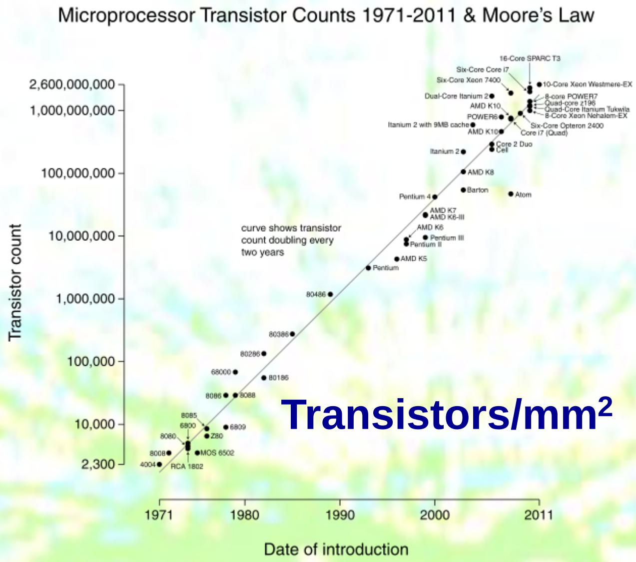
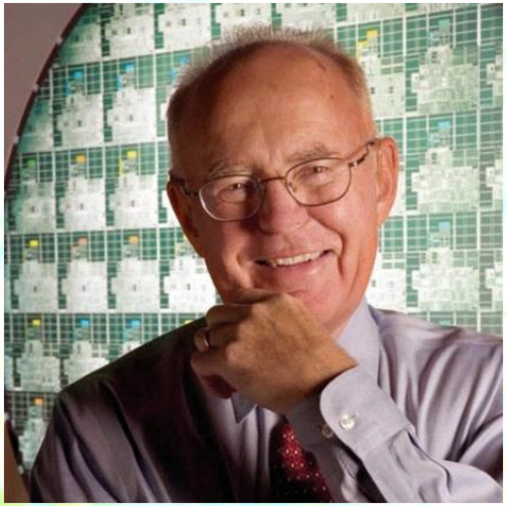
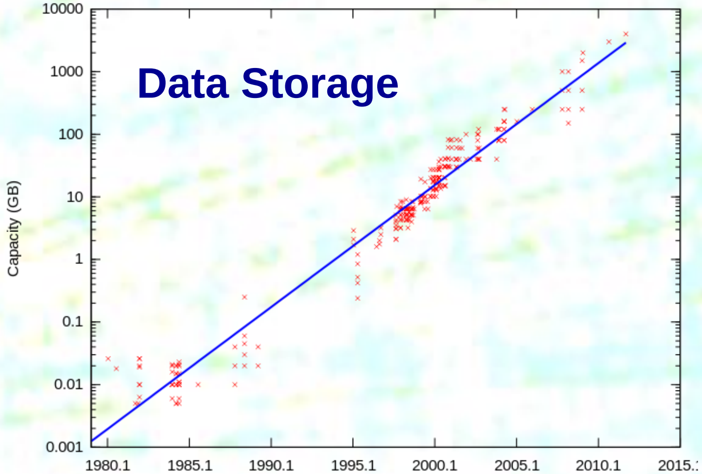
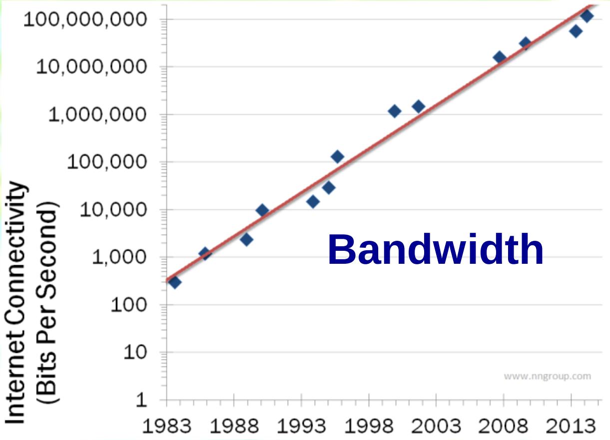
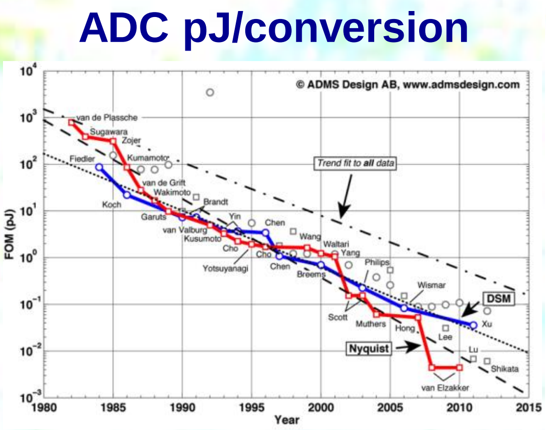
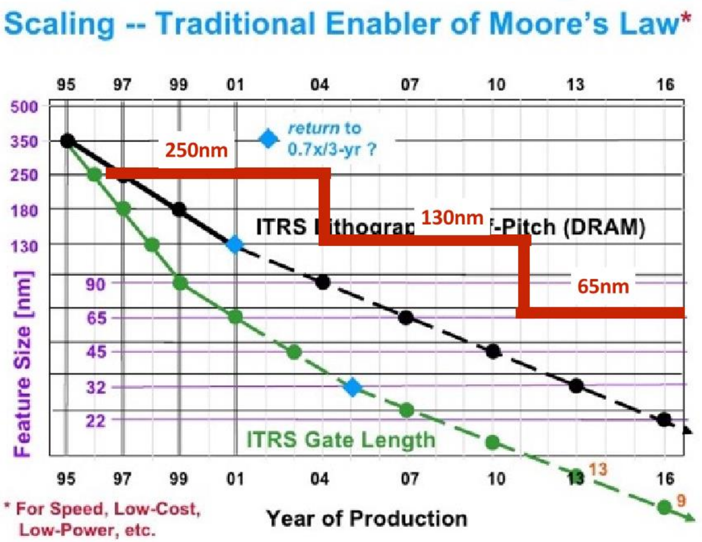












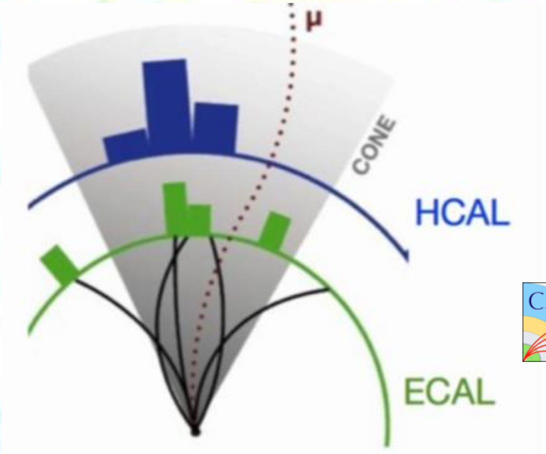
F Faccio: https://indico.cern.ch/event/468486

Historically showed doubling times of < 2 years but now slowing.

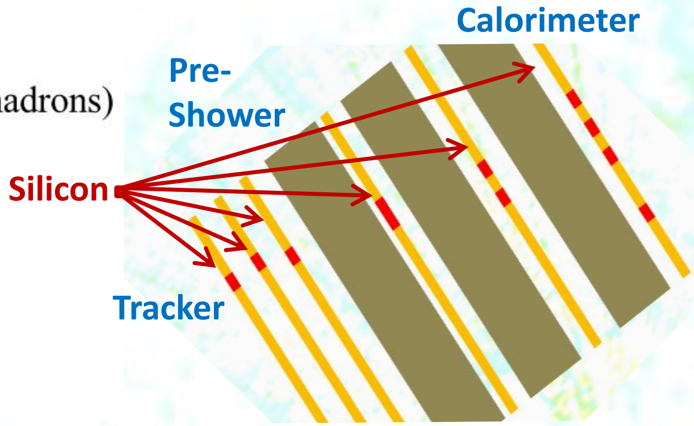
However, particle physics lags significantly behind commerical state-of-the-art because of additional constrants

Particle Flow Considerations

- In addition to vertexing, silicon detectors are widely assumed to be an important option for outer tracking either for a fully silicon "compact" tracker (often with high field) or outside a gaseous tracking volume (as "silicon wrapper" see for example Attilio Andreazza: https://indico.cern.ch/event/838435/contributions/3672992/attachments/1970363/3277344/LargeSiliconSystems_v2.pdf at 3rd FCC Workshop).
- Silicon detectors also technology of choice where high radiation, high speed or high granularity requirements; either in collider or fixed target experiments.
- The PFA concept requires excellent extrapolation of charged tracks into the calorimeter layers as well as high spatial resolution on EM showers (including resolving photons from high energy π^0 decays) and the start of hadron showers.
- Silicon layers (with tungsten or lead absorber) are also a leading candidate for such high granularity calorimeters, at least as far as the technology can be cost effective.



"Typical" jet:
~62% charged particles (mainly hadrons)
~27% photons
~10% neutral hadrons
~1% neutrinos



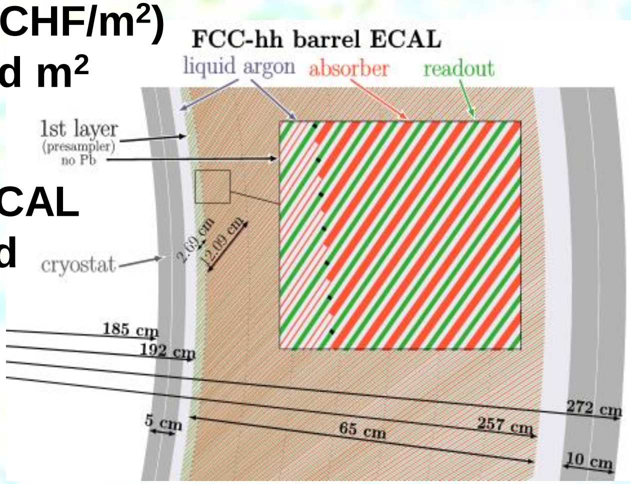
SiW ECAL CMOS MAPS Motivation

- **Current hybrid strip and pixel costs are still a major consideration (ATLAS Upgrade costs from Attilio Andreazza "*Large Silicon Systems*" at 3rd FCC Workshop, CERN January 2020, *referenced above*)**

	Strip	Pixels
Area	165 m²	13 m²
Power density	43 mW/cm²	700 mW/cm²
Module cost (TDR)	36900 kCHF	25067 kCHF
	224 kCHF/m²	1900 kCHF/m²

- **Even CMS HGCAL silicon module costs ~4CHF/cm² (40kCHF/m²) would still need to come down further for many thousand m² (» 10⁷cm²) array to become affordable**

➢ ***NB* partially mitigated by cost savings from reducing ECAL thickness (eg for FCC-hh) to < 20cm and removing need for cryostat with respect to LAr. (Depending in inner radius, could reduces total cost of HCAL, magnet system and muon spectrometer by up to factor of 2)**



11th FCC - ee Workshop — M. Aleksa

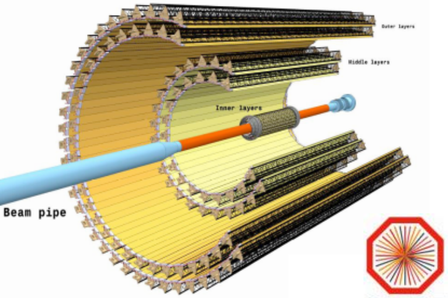
- **Excellent PFA capabilities but difficult to match LAr for cost, radiation-hardness and EM energy resolution**

- **For a hybrid silicon system (such as the CMS HGCAL), at some stage the price of polished high- ρ wafers could set a lower limit to what overall costs might be possible with separate thick depleted silicon substrate (although other options may exist)**

- **For both vertexing and outer tracking, thinking for silicon technology at future colliders is moving towards the use of CMOS Monolithic Active Pixel Sensors**

SiW ECAL CMOS MAPS Motivation

- **Currently, CMOS Imaging Sensors represent a ~20B$ business internationally (https://www.marketsandmarkets.com/Market-Reports/cmos-image-sensor-market-252212367.html) and market expected to continue growing rapidly driving down prices for such detectors**
- **Although existing CMOS sensor array (such as for ALICE ITS Monolithic Active Pixel Sensor) cost estimates can typically be ~5-10 times* those for CMS HGCAL, expect prices could be significantly lower for much larger orders and as a function of time, while integration of electronics within the sensor also reduces cost of full system**
- **Prototypes (see later) demonstrate concept of digital ECAL with same CMOS fabrication line that CERN and collaborators have shown, with appropriate design and processing, is now delivering radiation hardness to > $10^{15} n_{eq}/cm^2$**



ALICE

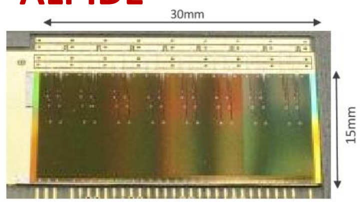
7 layers, 12.5 Gpixels covering **10 m^2** with 5 µm position resolution

Closer: Inner layer radius 39 mm -> 22 mm

Thinner: X/X_0 1.14% -> 0.3 % (inner layers)

Pixel size: 50 x 425 μm^2 -> 27 x 29 μm^2

ALPIDE



***ALICE-TDR-017 (~10^{10} Channels 10m^2)**

CMOS costs ~200kCHF/m^2 also suggested: Attilio Andreazza (private communication)

Table 9.1: Cost estimate

Item	Cost (kCHF)
Total	**12 039**
Pixel Chip	**5000**
CMOS wafers	3500
Thinning & dicing	1000
Series test	500

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The Digital EM Calorimeter Concept

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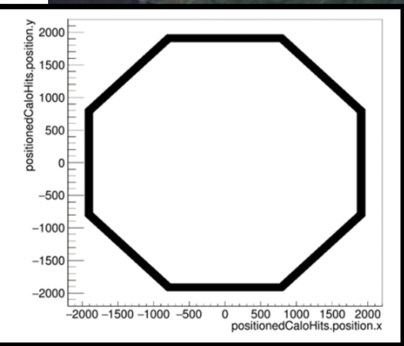
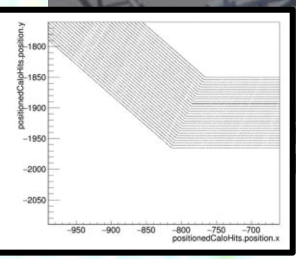
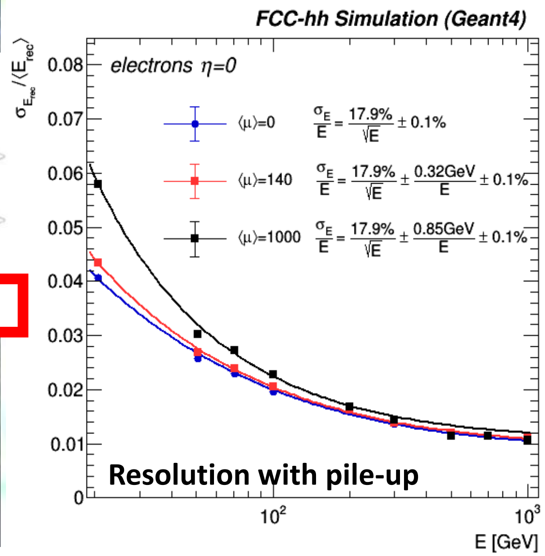






5 Alternative Technology for the EM Barrel Calorimeter

FCC Week (1/6/17) T. Price

Abada, A., Abbrescia, M., AbdusSalam, S.S. et al. Eur. Phys. J. Spec. Top. (2019) 228: 755. https://doi.org/10.1140/epjst/e2019-900087-0

Idea initially in context of CALICE but then adapted to FCC-hh environment.

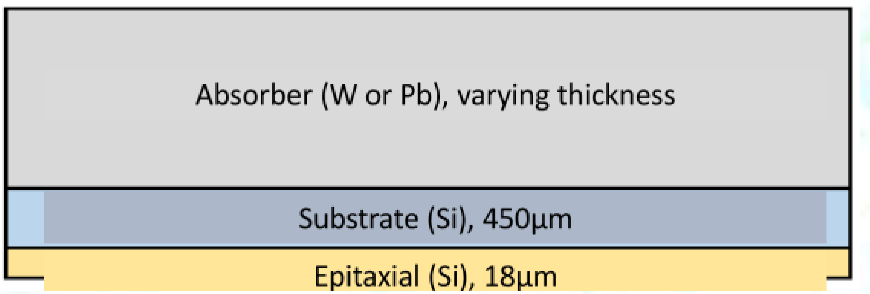
Simulated 4 different geometries:

30 Layers, 3.5mm W (30 × 1.0 X_0)

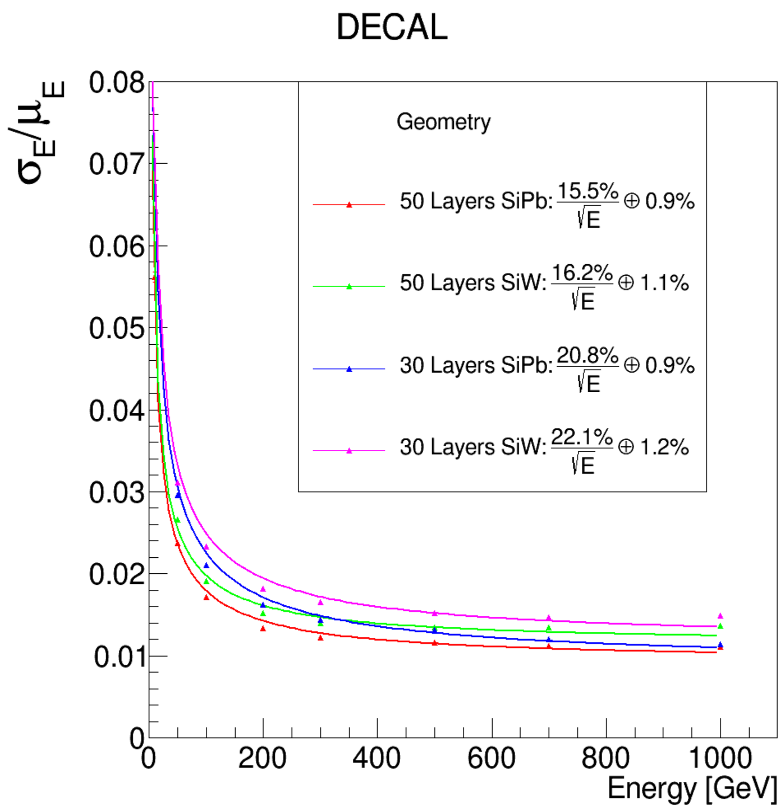
5.6mm Pb

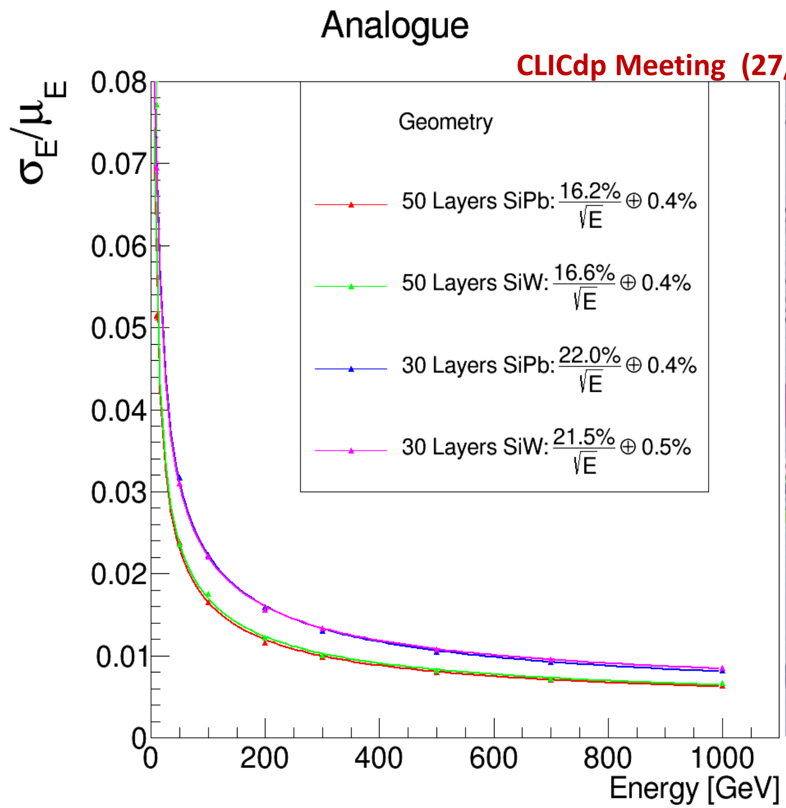
50 Layers, 2.1mm W (50 × 0.6 X_0)

3.4mm Pb

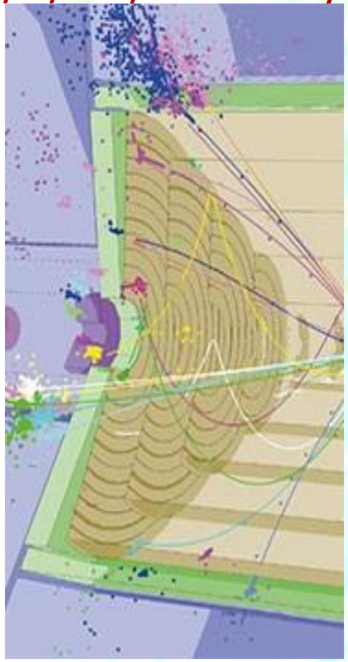


Silicon Calorimetry





CLICdp Meeting (27/08/2019) Robert Bosley

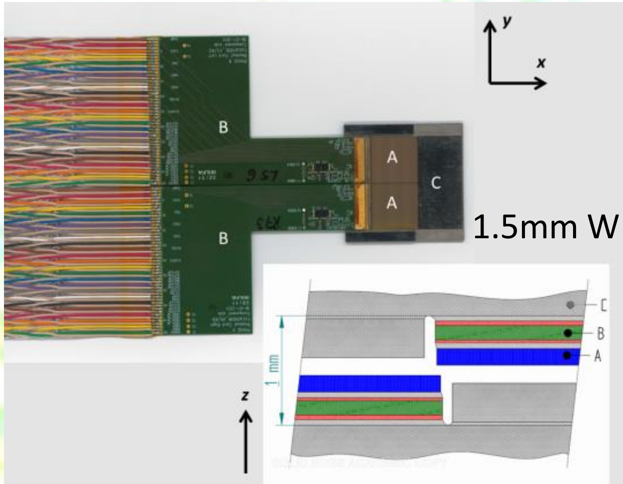


- **For single electrons, similar performance of Digital ECAL (with realistic channel threshold per pixel of 480e*) and Analogue ECAL (with perfect performance and full substrate signal per pad) up to around 300GeV (4T field without pile-up)**
- **Above this energy, saturation (more than one hit per $50\mu m \times 50\mu m$ pixel) starts to impact performance of digital compared with analogue ECAL**

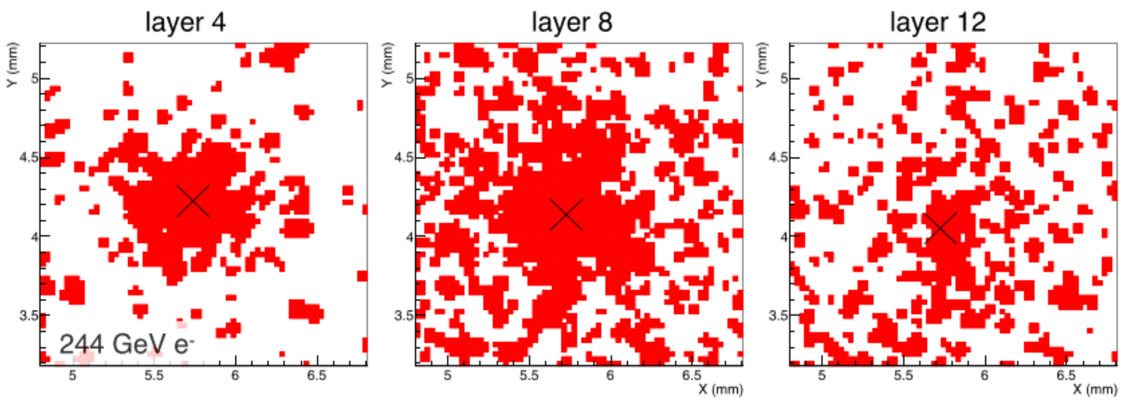
***$6 \times \sigma$ assuming noise of $\sigma = 80e$**

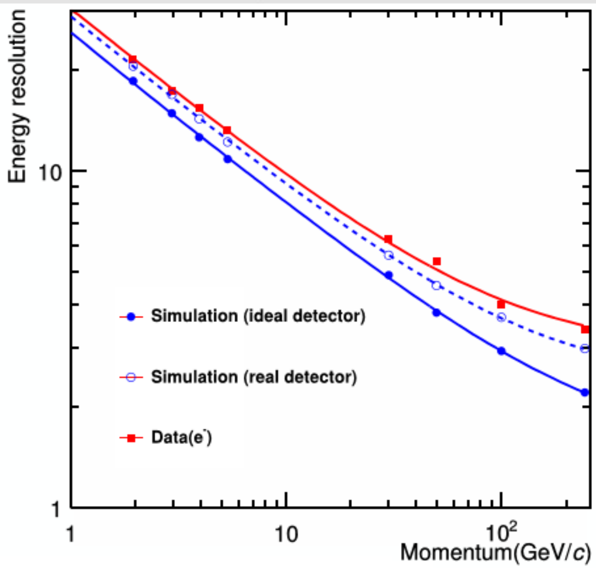
ALICE FoCal MAPS R&D

T. Peitzmann: "*R&D for the ALICE-FoCal Detector Proposal -Towards Truly High-Granularity Calorimeters*", CERN Detector Seminar 25/10/19



24 layer MIMOSA CMOS sensor calorimeter Si-W stack

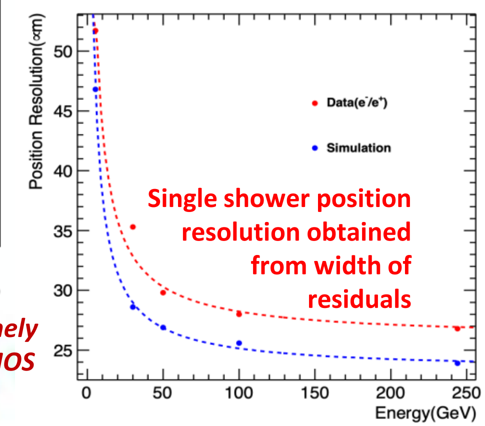




A. de Haas, et al., "*The FoCal prototype - an extremely fine-grained electromagnetic calorimeter using CMOS pixel sensors*", JINST13(2018) P01014

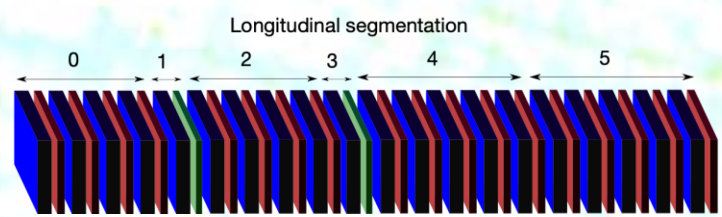
$$\frac{\sigma_E}{E} = a \oplus \frac{b}{\sqrt{E/\mathrm{GeV}}} \oplus \frac{c}{E/\mathrm{GeV}}$$

$$a = (2.95 \pm 1.65)\%$$
$$b = (28.5 \pm 3.8)\%$$
$$c = 6.3\%$$



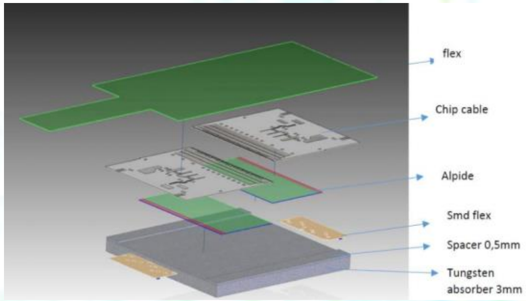
244 GeV electron: very high single particle hit rate in shower core

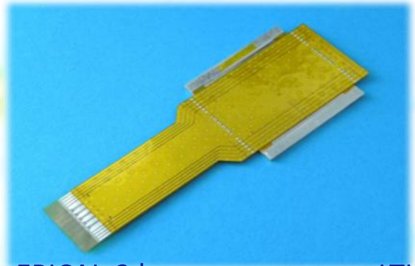
Good energy resolution but lower than simulations, particularly at higher energies



New ALPIDE CMOS sensor based 3cm×3cm area 24 layer stack

ALICE FoCal ALPIDE Test Beam



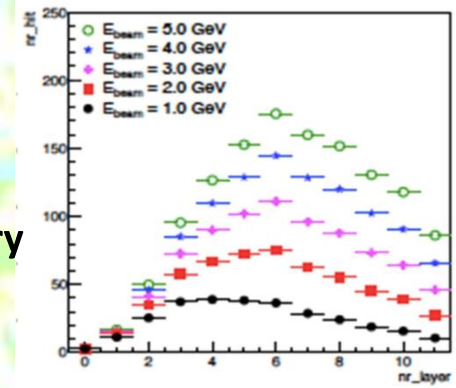


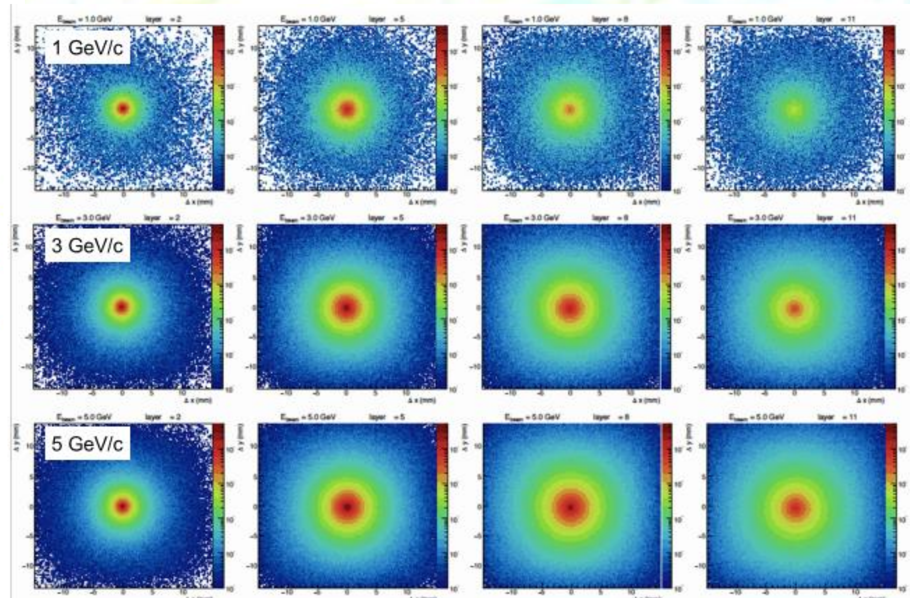
EPICAL-2 layer prototype at LTU

DESY Test Beam (Nov 2019)

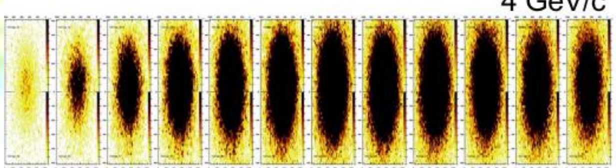
Online data displays

Raw hits already show very reasonable longitudinal shower profiles





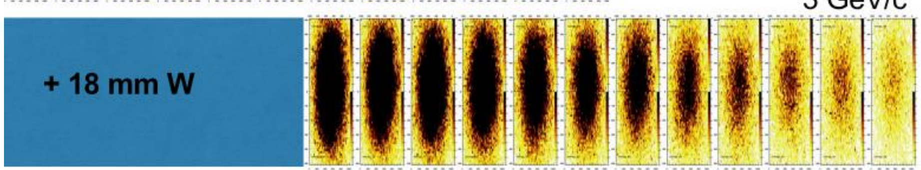
4 GeV/c



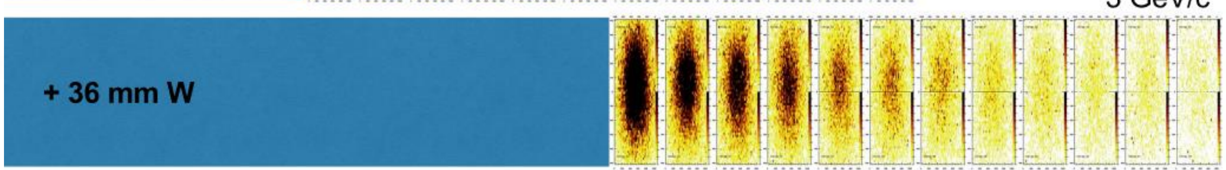
EPICAL-2

ALICE

3 GeV/c



3 GeV/c



Full test beam analysis results expected imminently.

Small Diode CMOS Prototyping

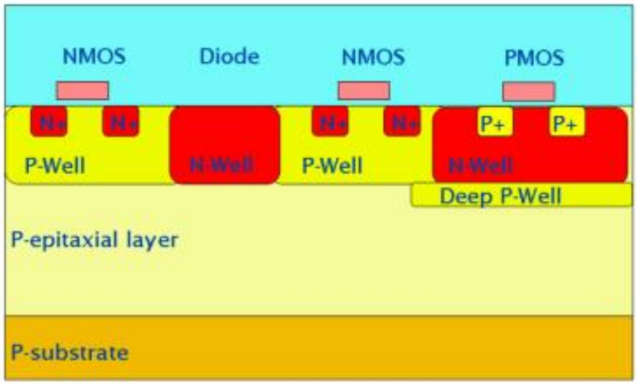
Birmingham Instrumentation Laboratory for Particle physics and Applications (BILPA)

UNIVERSITY OF BIRMINGHAM

Developments with STFC CMOS Sensor Design Group (CSDG) in technology also used for ALPIDE and MALTA developments by CERN

Walter Snoeys FCC workshop CERN, Jan 14, 2020

The INMAPS process: quadruple well for full CMOS in the pixel



STFC development, in collaboration with TowerJazz

Additional deep P-well implant allows complex in-pixel CMOS and 100 % fill-factor

New generation of CMOS sensors for scientific applications (TowerJazz CIS 180nm)

Also 5Gb/s transmitter in development

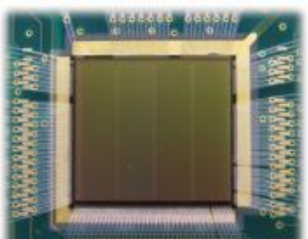
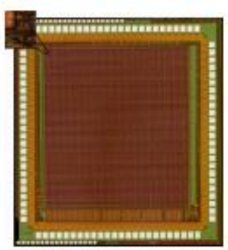
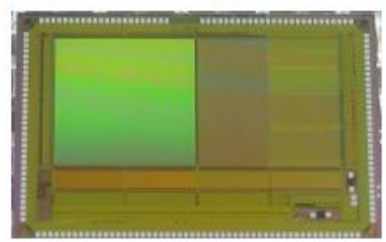
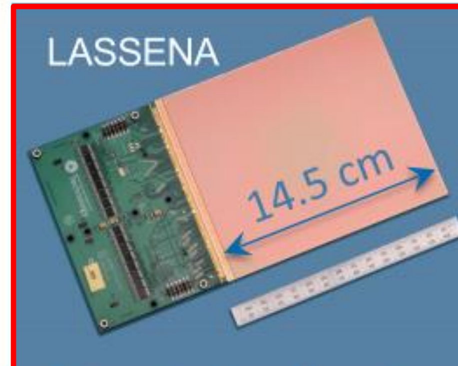
Sensors 2008 (8) 5336, DOI:10.3390/s8095336

https://iopscience.iop.org/article/10.1088/1748-0221/7/08/C08001/meta

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01006/meta

http://pimms.chem.ox.ac.uk/publications.php ...

courtesy of N. Guerrini, STFC

TPAC ILC ECAL (CALICE)	DECAL Calorimetry	PIMMS TOF mass spectroscopy	CHERWELL Calorimetry/Tracking	LASSENA
				
50μm pixel	50μm pixel	70μm pixel	48 μm x 96 μm pixel	50μm pixel, waferscale

walter.snoeys@cern.ch

Also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

9

Applications of Large Format Sensors

Developments with STFC CMOS Sensor Design Group (CSDG) in technology also used for ALPIDE and MALTA developments by CERN

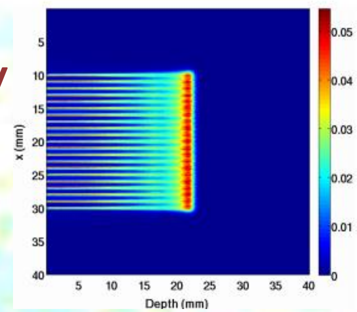
CSDG have also developed many applications of large format sensors for space, electron microscopy, x-ray detection and medical imaging.

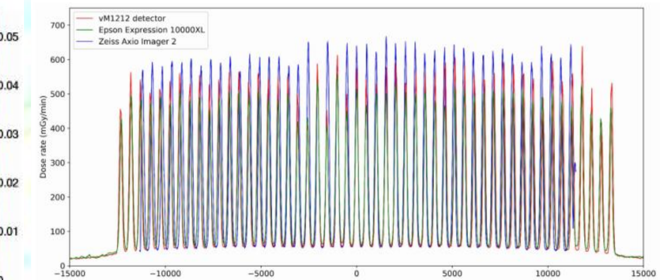
In radiotherapy, FLASH (2-40 Gy in less than 500ms) and Mini-beam or Micro-beam (sub mm) treatments currently very exciting as found to greatly improved sparing of healthy tissue (both x-ray and hadrons)

One recent example using the LASSENA senor shows resolution (contrast) better than film with fast (34fps) <u>real time image</u>

Needs further development
For use at hadron facilities

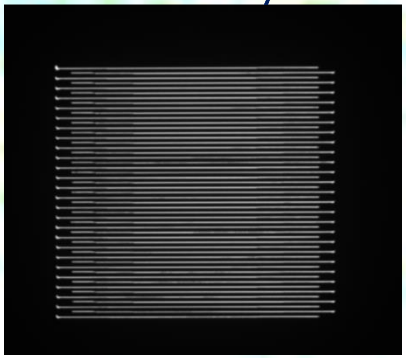
***"Evaluation of a pixelated large format CMOS sensor for x-ray microbeam radiotherapy"* Medical Physics, 2020**

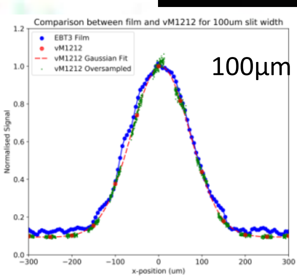


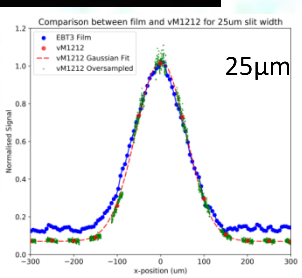


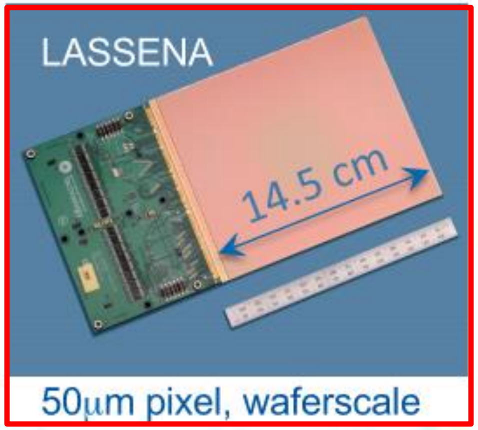
S. Flynn, T Price. (NPL and UoB)
225 kV, 1.65 Gy/min, Helmholtz Research Centre in Munich
https://doi.org/10.1002/mp.13971

Microbeam slit system









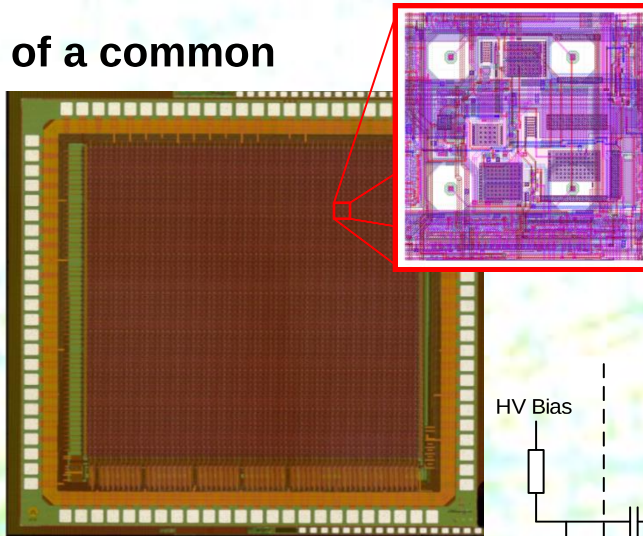
DECAL (4mm×4mm Array) Prototype Chip

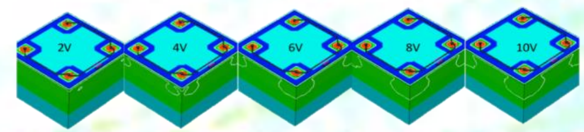
Concept, in FCC-hh context, of a common silicon development for:

- **Outer tracking**
- **Pre-shower**
- **EM calorimeter**

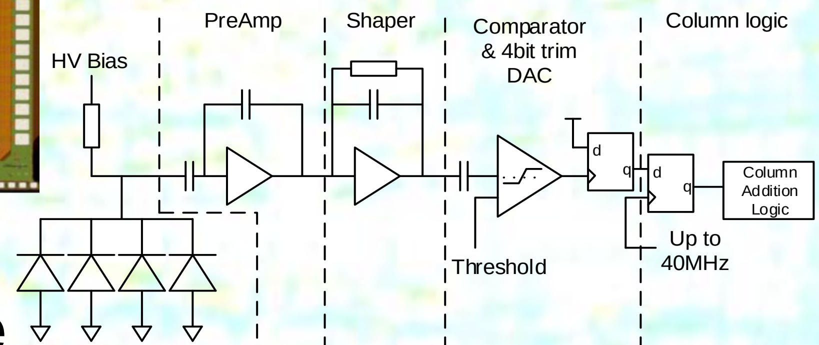
Reconfigurable sensor as:

- **5mm×50μm strips**
- **5mm×5mm pad**





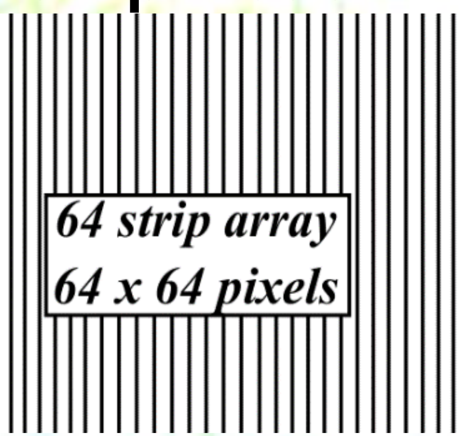
4 Diode TCAD Simulation: Giulio Villani



TWEPP (4/9/19) S.Benhammadi

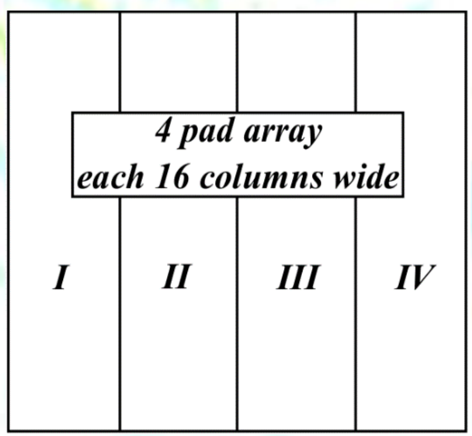
Prototype as proof of concept (180nm CMOS*)

Strip mode



Information on up to 3 hits per column gives data rate 5.12Gb/s

Pad mode

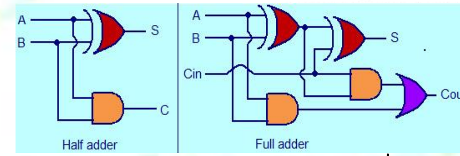


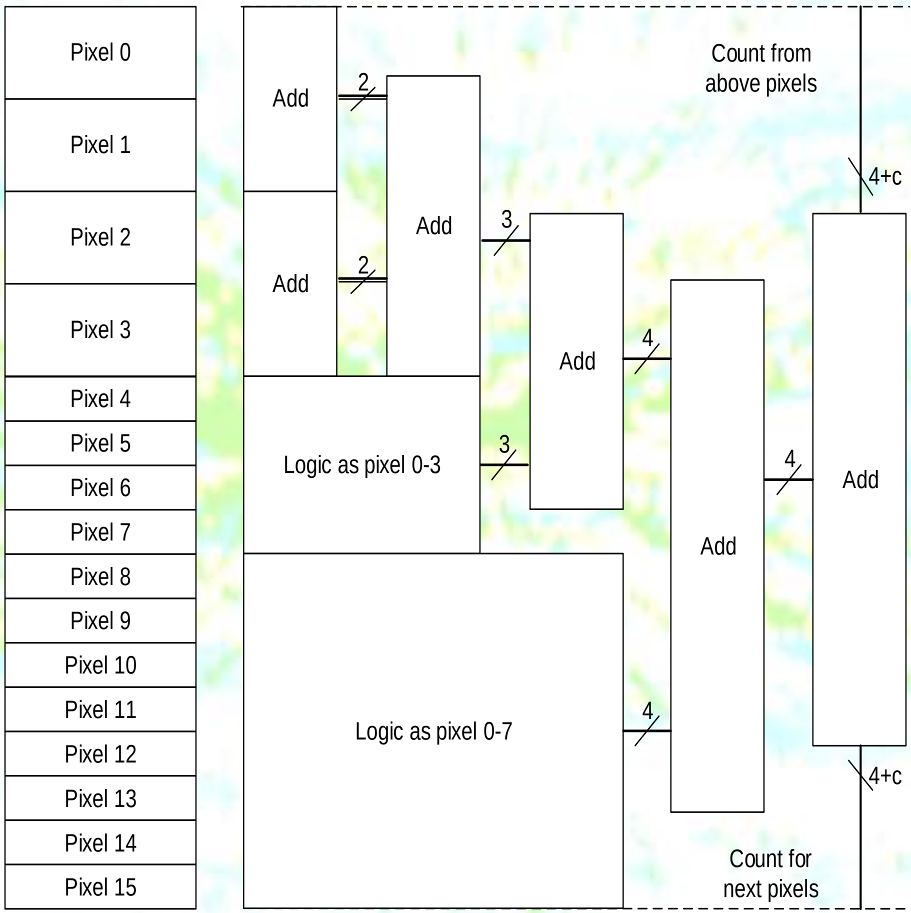
Information on up to 15 hits per column giving 240 hits per pad gives data rate of 2.56Gb/s

Specification	*Unit*	*Value*
Pixel Pitch	um	55
Resolution	pix	64 x 64
Frame Rate	MHz	40
Input Referred Noise	e- rms	80
Max hits/col (pad mode)	hits	15
Max hits/col (strip mode)	hits	3

***TowerJazz (Small collecting node)**

DECAL- Summing Logic





16 pixels are grouped together

For PAD mode:

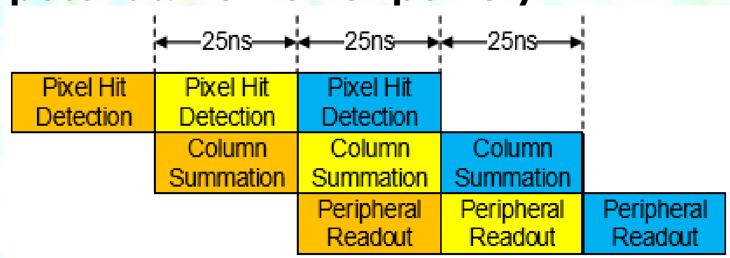
- **4 bits of data + carry (pad mode)**

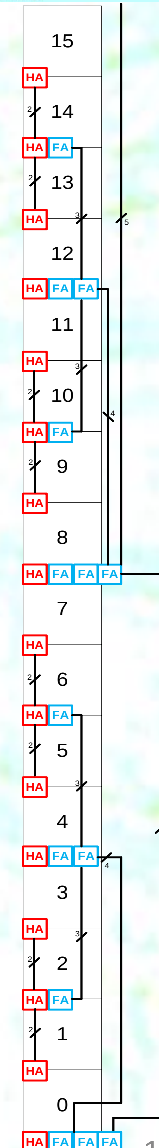
For STRIP mode:

- **only the 2 first bits of data used**

To achieve data rate of 40MHz column sum has to be complete within 25ns using fast logic

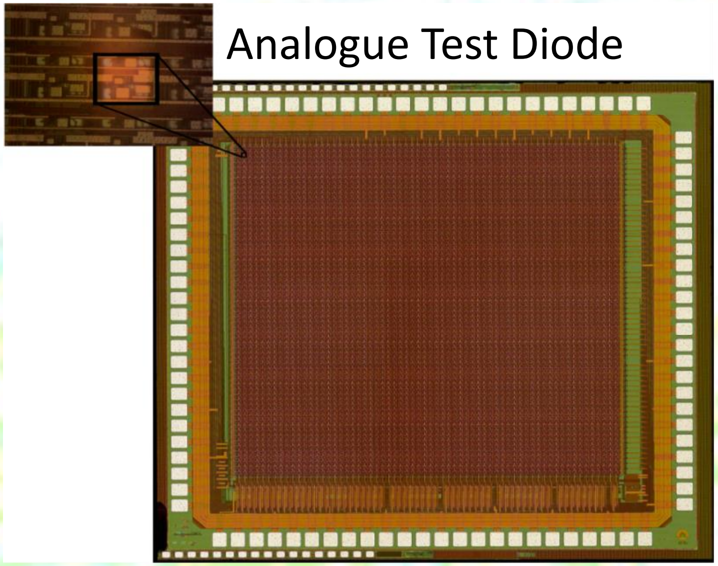
(Approach should also have potential for lower power)

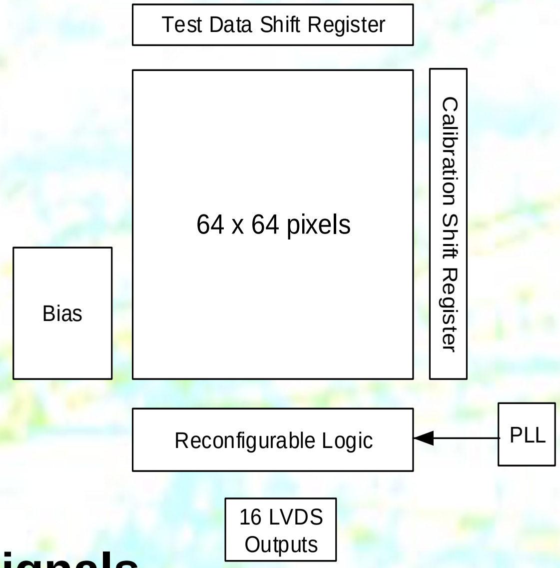


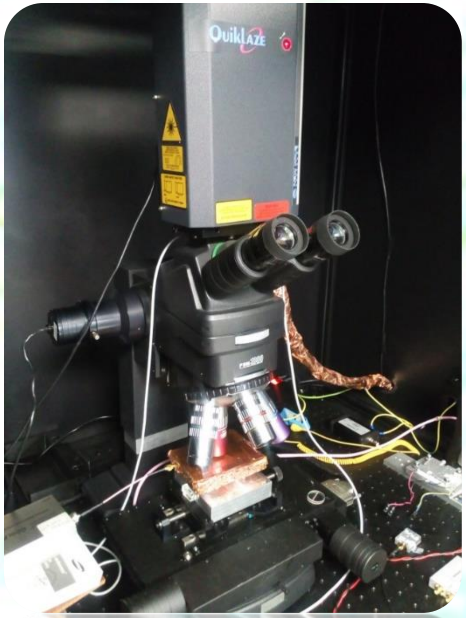


DECAL – Analogue Performance

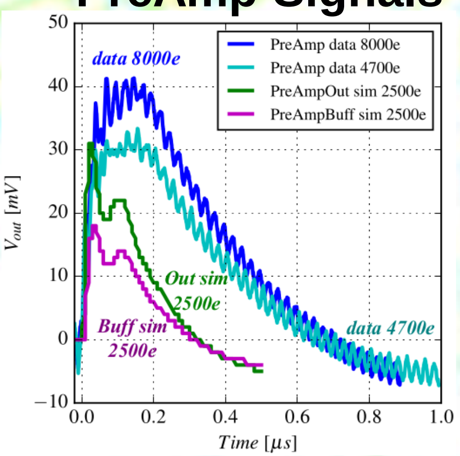
Analogue Test Diode



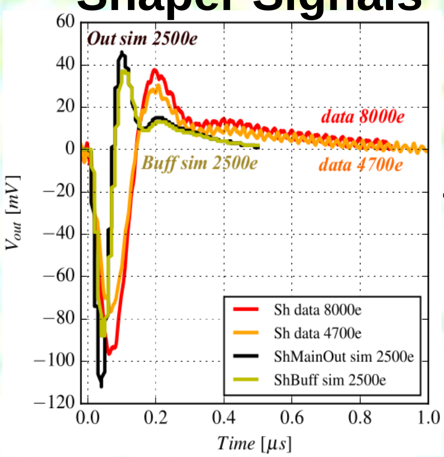




PreAmp Signals



Shaper Signals

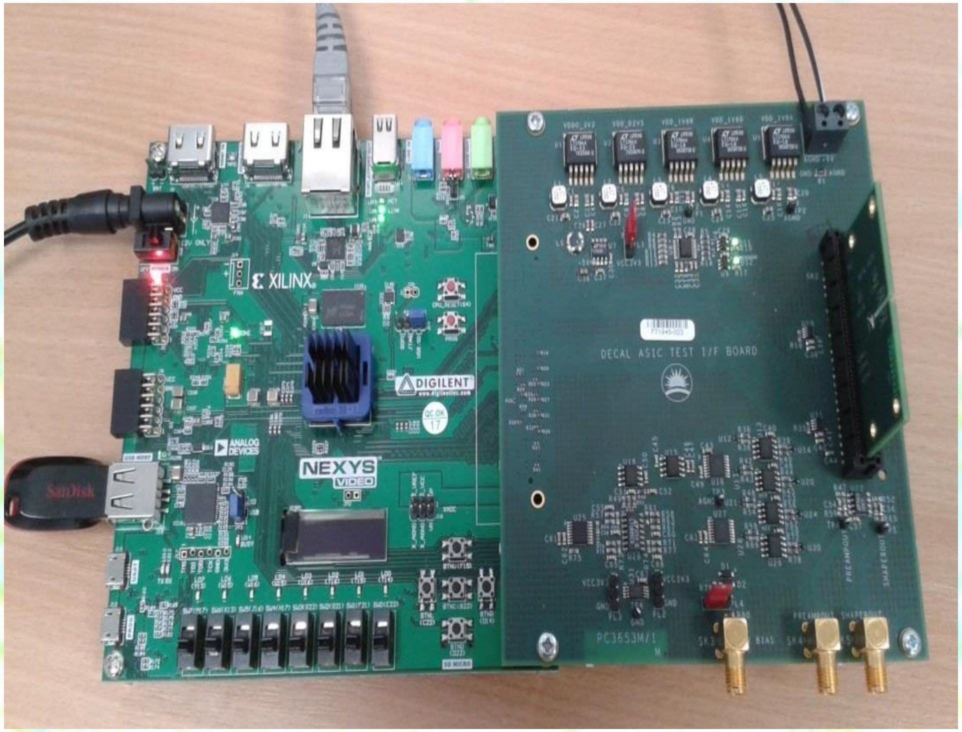


Some delay in measured response time with respect to FE simulation (but expect ~10ns signal collection)

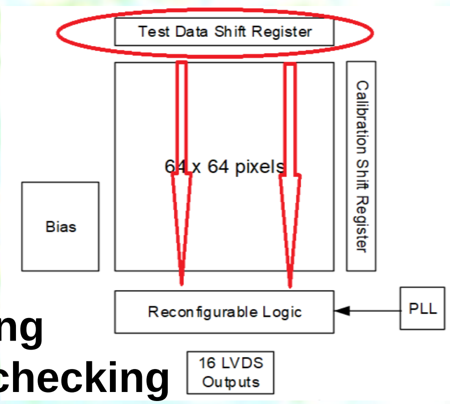
10x10µm^2 TriLite laser (pJ/pulse, λ=1064 nm)

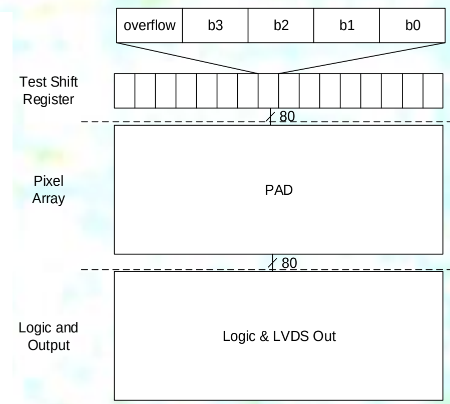
Estimate of injected charge in 18 µm epitaxial layer of DECAL sensor uses measured signal in photodiode

DECAL Prototype: Data Acquisition System



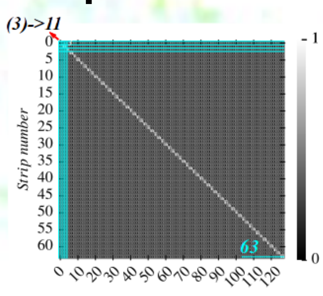
- DIGILENT NEXYS Video Board
- DECAL motherboard allows all the bias voltages and currents to be software controlled.
- Ethernet based readout using ATLAS ITSDAQ software and hardware.
- System allows readout at 40MHz



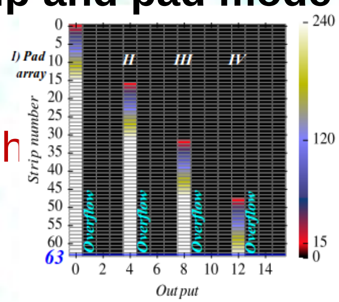


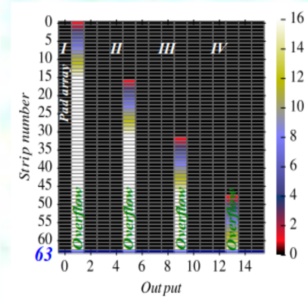
DECAL on Carrier Board

Simulate pixel output by placing data in test shift register and checking output is correct for both strip and pad mode



Pattern of 11'b clocked through in **strip** mode

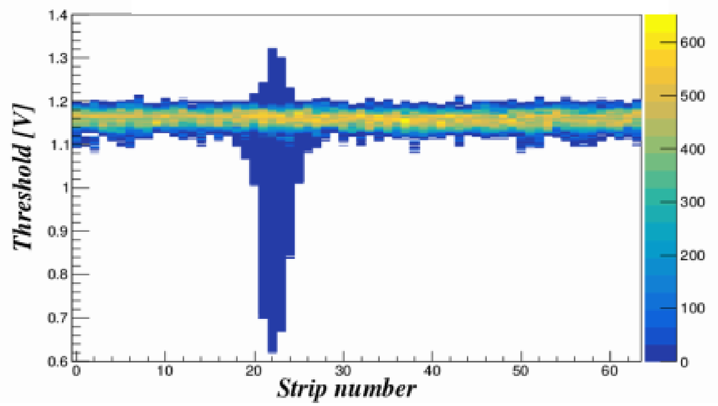




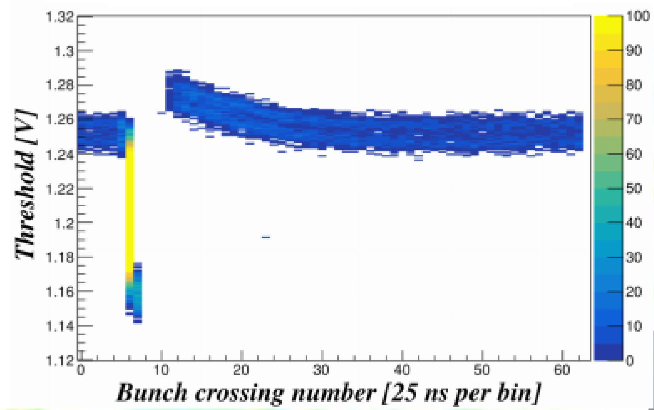
Patterns of 01111'b and 10000'b clocked in **pad** mode

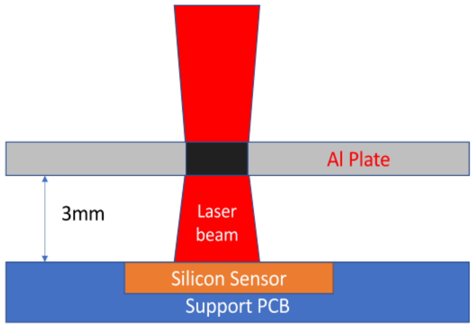
DECAL Prototype: Laser Testing

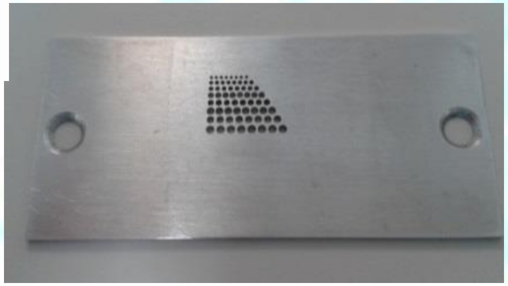
Threshold at which output of comparator first fires vs strip #



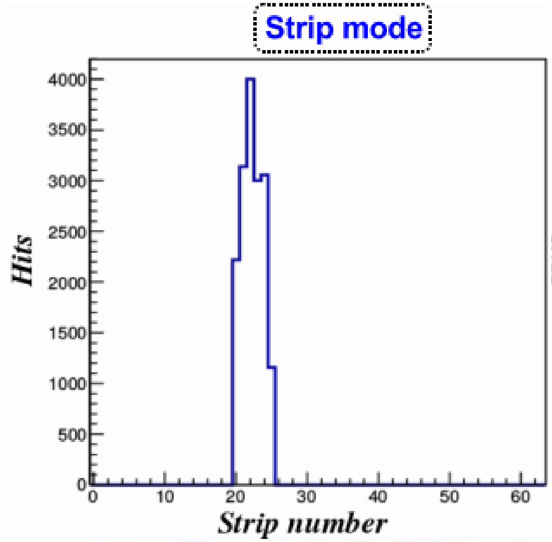
Single strip threshold at which comparator first fires vs time

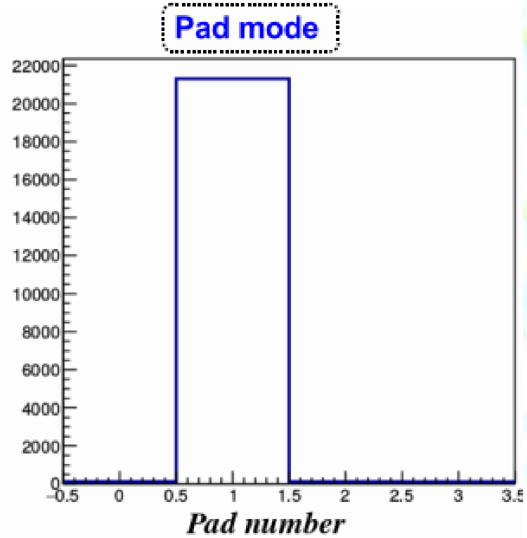






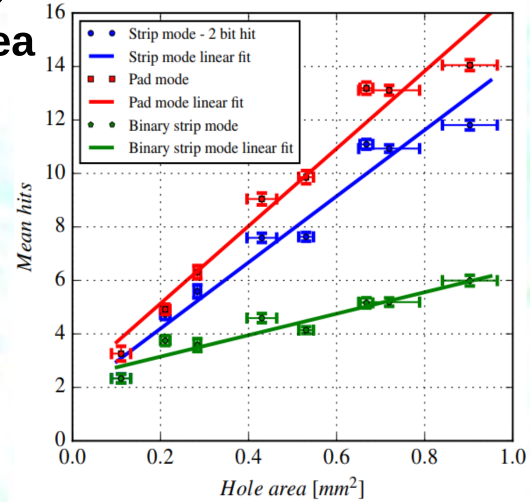
IEEE MIC-NSS (30/10/19) I. Kopsalis





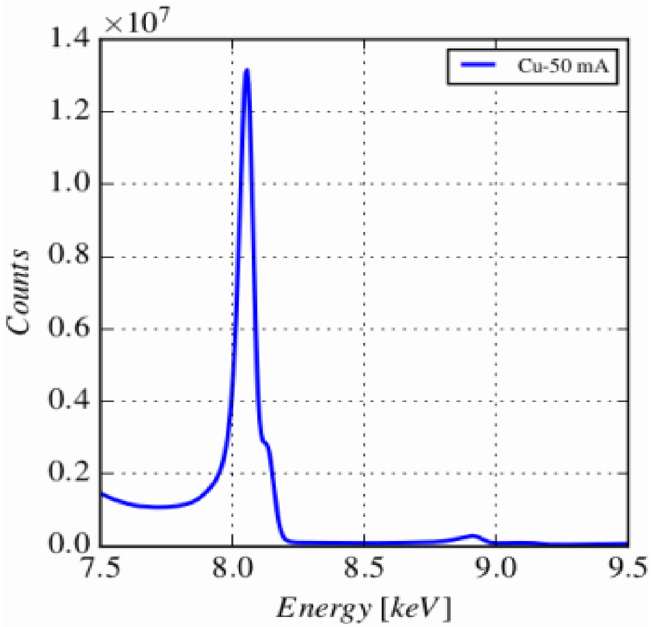
Global threshold value of 1 V

Check pad and strip mode response to different area light spots

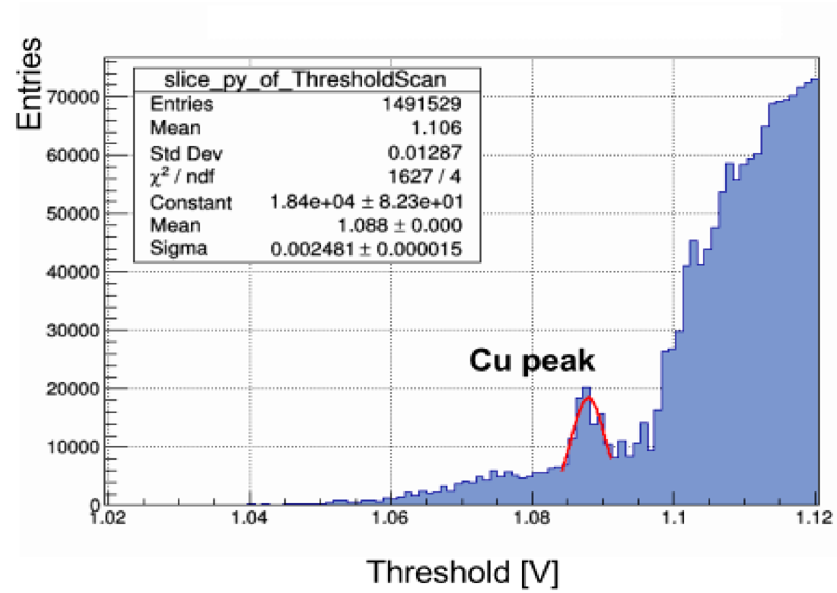


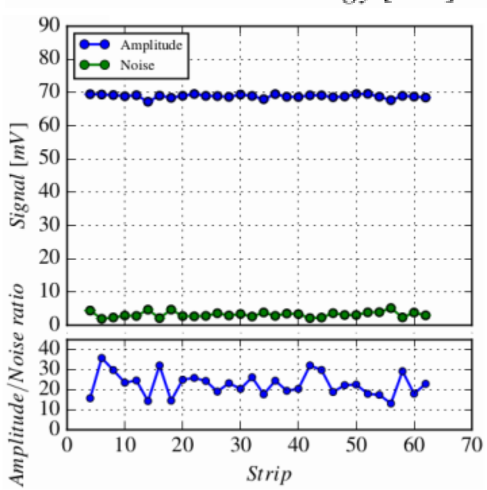
DECAL Prototype: Cu K_α Calibration

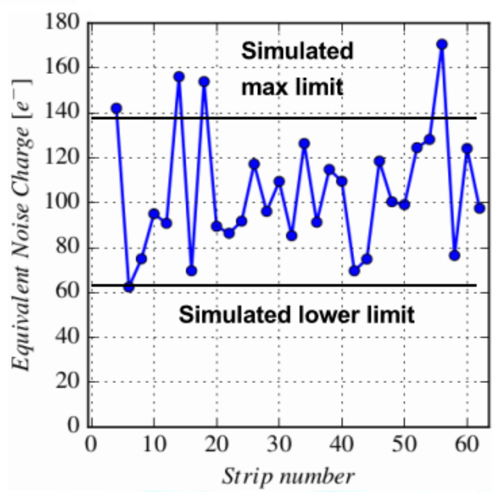
Energy spectrum of Cu measured with RAL HEXITEC detector



Scan of single strip threshold at which comparator first fires







Expected signal: 8050eV /3.6eV = 2236*e*

Taking width of fitted peak as estimator of noise gives Signal/Noise ≈ 22

Noise ≈ 100*e*

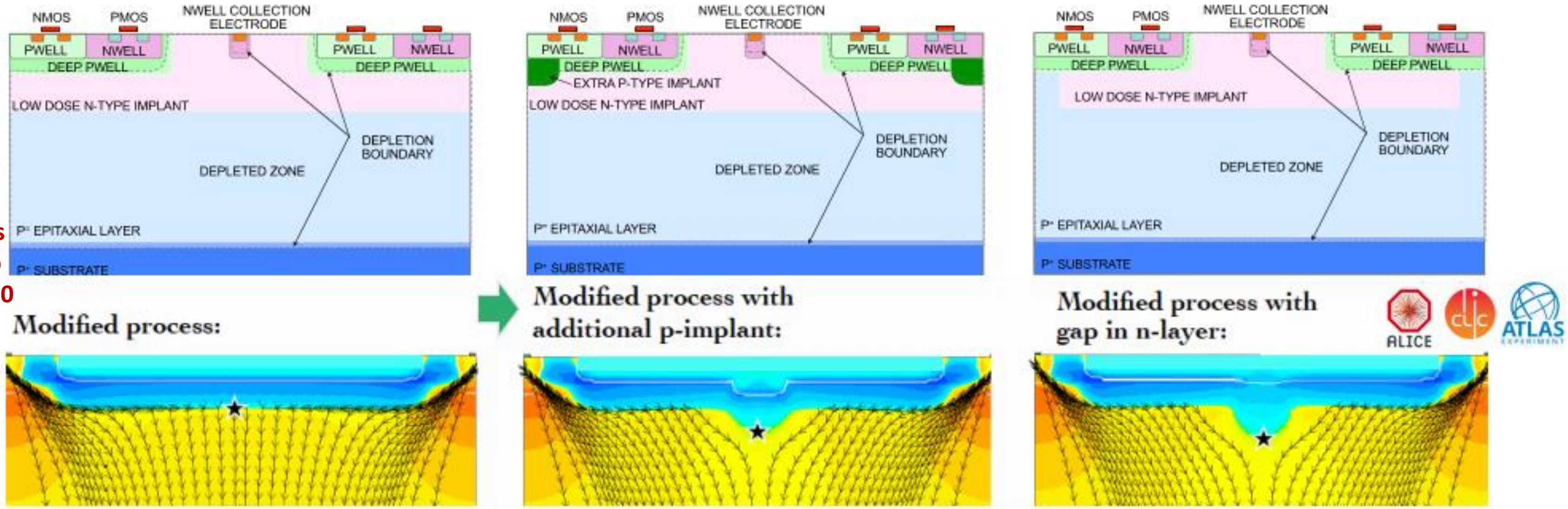
CERN TJ Developments

Birmingham Instrumentation Laboratory for Particle physics and Applications (BILPA)

UNIVERSITY OF BIRMINGHAM

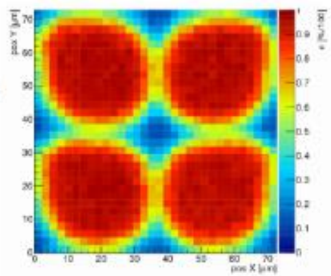
- **From ALPIDE, CERN has further developed the radiation hardness of the TJ process**

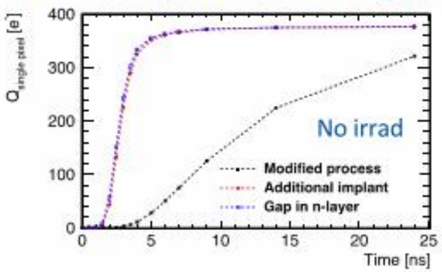
Walter Snoeys
FCC workshop
CERN, Jan 2020



Extra p-type implant or gap in the n-layer for improved lateral field

Efficiency drop at pixel edges after irradiation for 36.4 x 36.4 μm² pixel needs improvement
E. Schioppa et al, VCI 2019

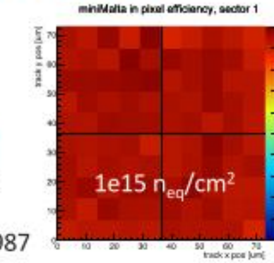




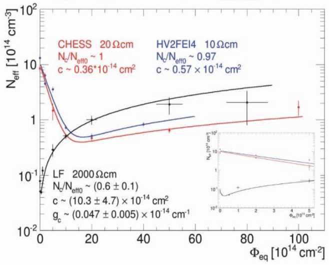
3D TCAD simulation
M. Munker et al. PIXEL2018

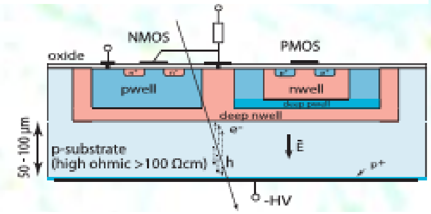
Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019

M. Dyndal et al., arXiv:1909.11987



- **Similar results with other processes and designs**
- **Excellent for fast, full signal collection, as well as radiation hardness suitable for hadron colliders**

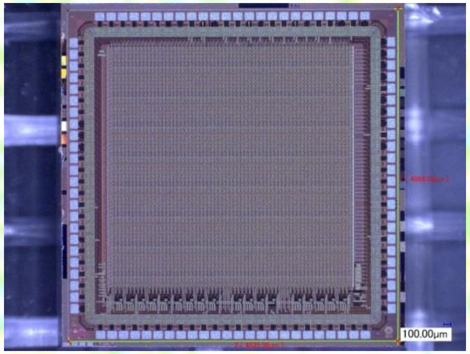




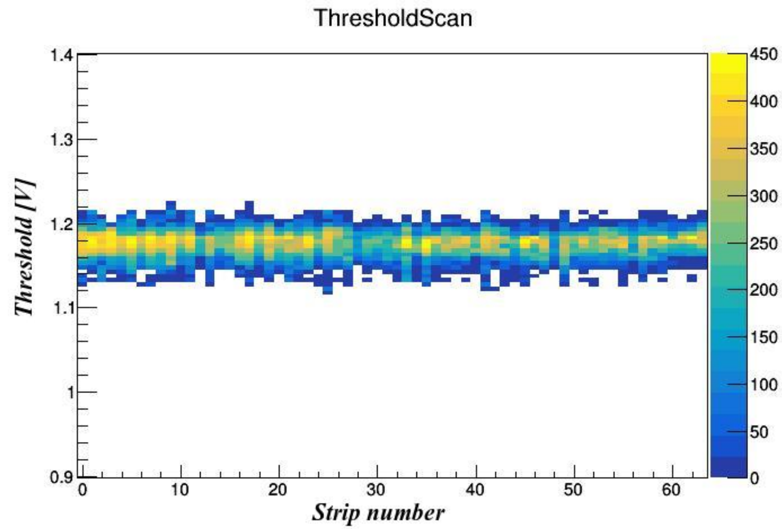
Garcia-Sciveres, M. & Wermes, N. A review of advances in pixel detectors for experiments with high rate and radiation. *Rep. Prog. Phys.* **81**, 066101 (2018).

DECAL in Modified TJ Process

- **For the programme between RAL Particle Physics, Birmingham and STFC CMOS Sensor Design Group, we have now had a new version of the DECAL designed and fabricated in the TJ modified process with help from the CERN group which was delivered in August**
- **So far we see threshold scans working and are exercising the digital functionality including checking a few minor bug fixes in the new chip, but still early days**

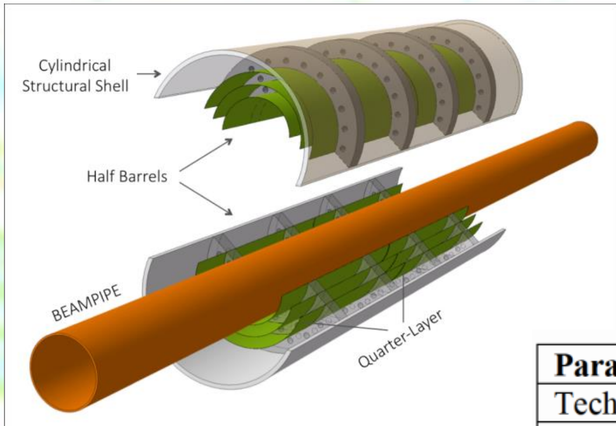


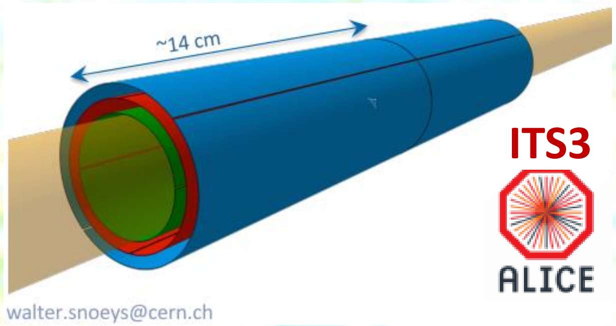
- **In parallel, we are working towards MAPS for the EIC vertex detector in collaboration with nuclear physicists at LBNL and Birmingham**
- **Following participation with the MALTA team, we are contributing to the EP-RD-ET process as part of WP 1.2 with a view to exploiting the 65nm process being explored by CERN (see below) for EIC and FCC/ILC activities**



Towards 65nm CMOS Sensors

- **From ALPIDE, CERN has further developed the radiation hardness of the TJ process**
- **Working towards the ITS3 upgrade of ALICE and longer-term CMOS R&D**



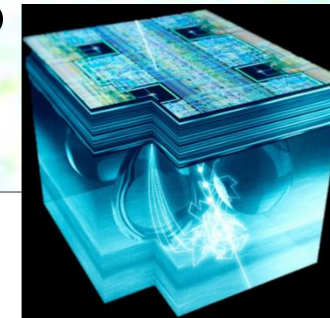


ITS3

ALICE

Walter Snoeys
FCC workshop
CERN, Jan 2020

Sensitive area: 4.12 cm²
Inner Barrel: 36.9 mW/cm²
Outer Barrel: 20.2 mW/cm²
In the matrix:
(analog + digital)/area
(22.2 + 3.2)/4.12 = 6.2 mW/cm²



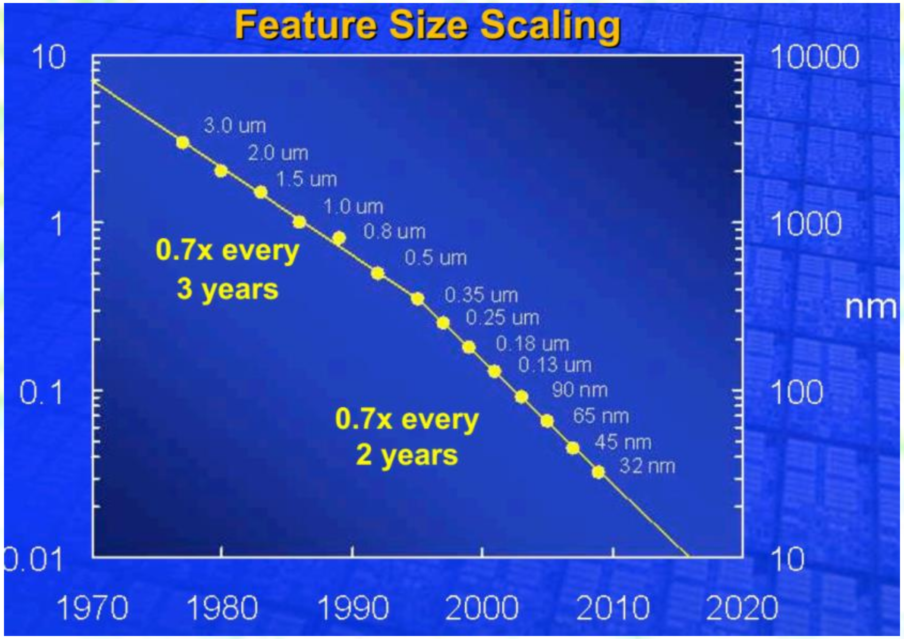
ALPIDE

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 μm	20-40 μm
Pixel size	27 x 29 μm	O(10 x 10 μm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 μs	~ 200 ns
Time resolution	~ 1 μs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 | 5

More Observations on CMOS Costs

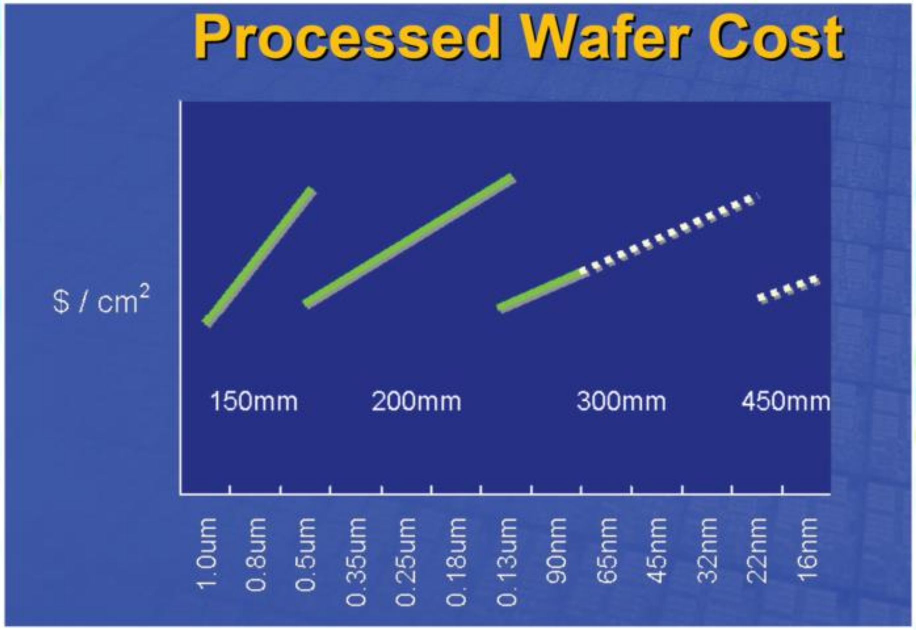
- Getting prices for commercial CMOS Imaging Sensors (CIS) not so easy, but entry costs (NRE, design, etc) are progressively higher with smaller feature size, so R&D prototyping expenses make it highly advantageous to have more common developments.
- Cost per transistor, rather than cost per area, tends to be what Moore's law scaling drives down most quickly (but we do not need *cutting edge*).



Measuring Moore's Law:
Evidence from Price, Cost, and Quality Indexes[1]

https://www.nber.org/chapters/c13897

Kenneth Flamm



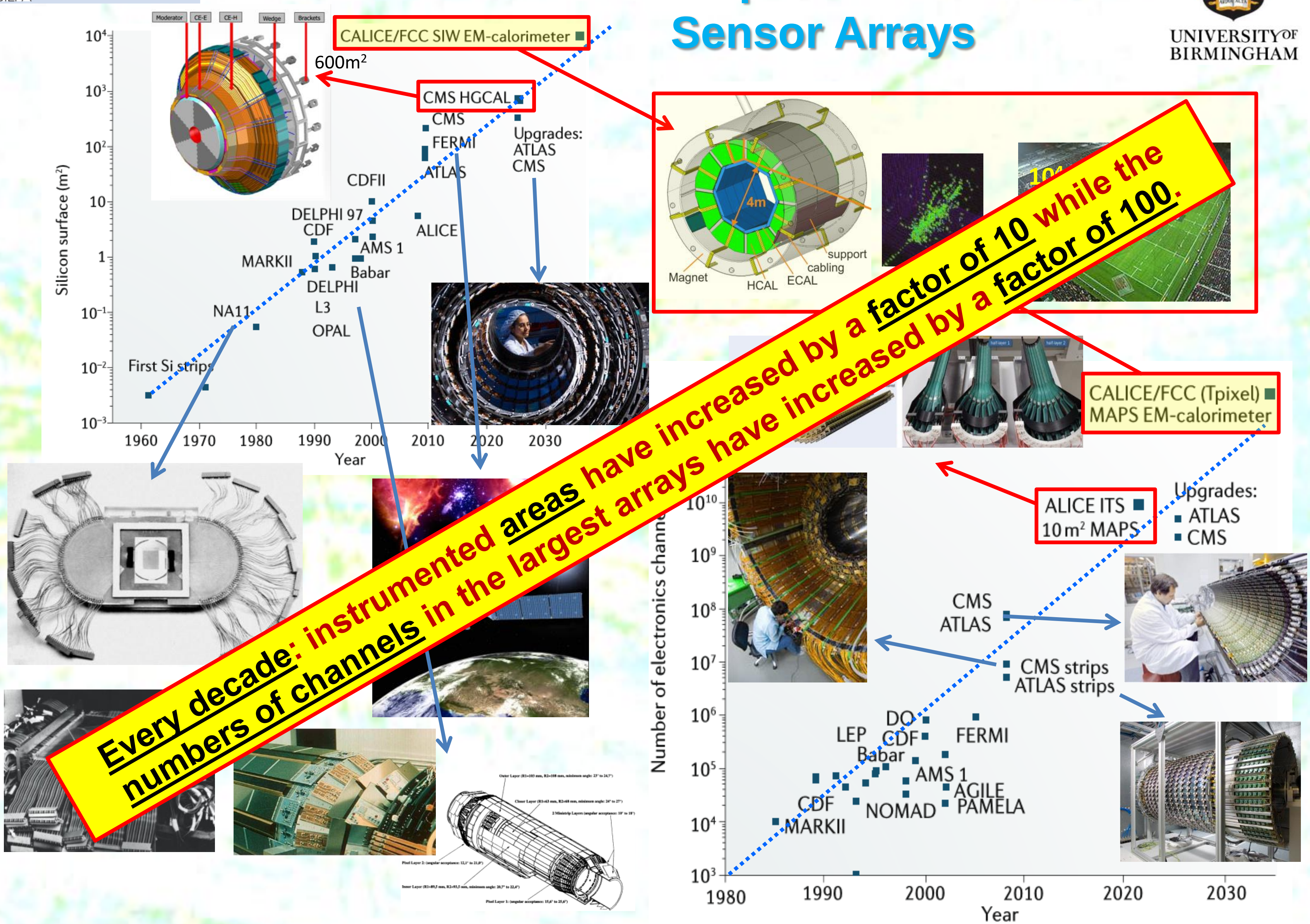
Source: Holt (2005).

(Clearly for our purposes, we care about larger area, as well as greater functionality, unlike the main commercial drivers)

Birmingham Instrumentation Laboratory for Particle physics and Applications BILPA

Historical Development of Silicon Sensor Arrays

UNIVERSITY OF BIRMINGHAM



Conclusions and Observations

- Si-W calorimetry should allow excellent PFA performance with a seamless transition from outer tracking → pre-shower → ECAL in potentially the same technology
- For future Si-W (Si-Pb) calorimeters to be affordable, need silicon sensor costs to come down to ~few CHF/cm^2 (as potential silicon areas are » 10^7cm^2)
- It could be that this becomes more achievable in CMOS Imaging Sensor technologies given the very large, fast growing commercial market and the overall system cost impact of integrating the front-end electronics with the sensor substrate
- ➢ Power needs study as at FCC data rates, CMOS sensor dissipations ~several ×10mW/cm^2 with no power pulsing could be problematic (*cf* CMS HGCAL: ~200kW)
- A prototype has been developed which proves concept of digital ECAL with same CMOS fabrication line that CERN and collaborators have shown, with appropriate design and processing, is now delivering radiation hardness to > $10^{15} n_{eq}/cm^2$
(Reprocessed DECAL prototype recently delivered taking advantage of these features)
- Digital EM calorimetry also provides an excellent potential solution for electron-ion and e^+e^- facilities with very fast charge collection which could also be useful for triggering
- Aspects could also be employed with other calorimeter technologies, for example as high granularity pre-shower integrated with outer tracking layers
- RD50 was publishing first results on irradiations in the p-type detector technologies currently being implemented for the HL-LHC ATLAS and CMS upgrade trackers in 2004

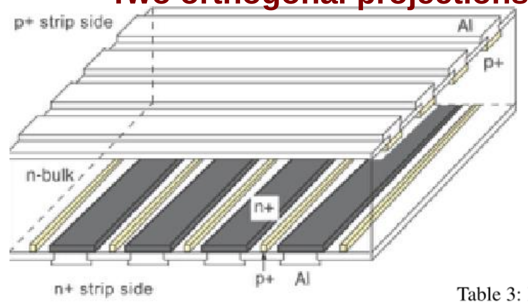
→ **Require ~20 year lead-time for starting R&D targeting largest future systems**

BACK-UP

Historical Development of Silicon Sensor Arrays

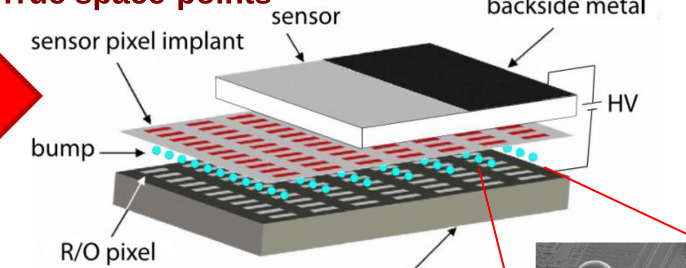
The highest channel count arrays are based on pixelated detectors. For **hybrid pixel sensors** connection to the electronics requires flip-chip technologies.

Two orthogonal projections



Double sided strip sensor

True space-points



Hybrid pixel detector

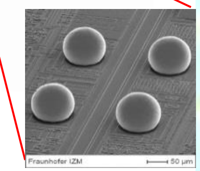
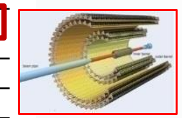


Table 3: Project cost estimate breakdown.

Item	R&D (kCHF)	Construction (kCHF)	Total Cost (kCHF)
Total	2000	3300	5300
Beampipe	600	900	1500
Pixel CMOS Sensors	700	700	1400
Sensor test	100	150	250
Thinning & dicing	200	300	500
Hybrid printed circuit	100	100	200
Mechanics	150	350	500
Assembly & test	50	200	250
Installation tooling	0	200	200
Air cooling	100	150	250
Services	0	100	100
Patch panels	0	150	150

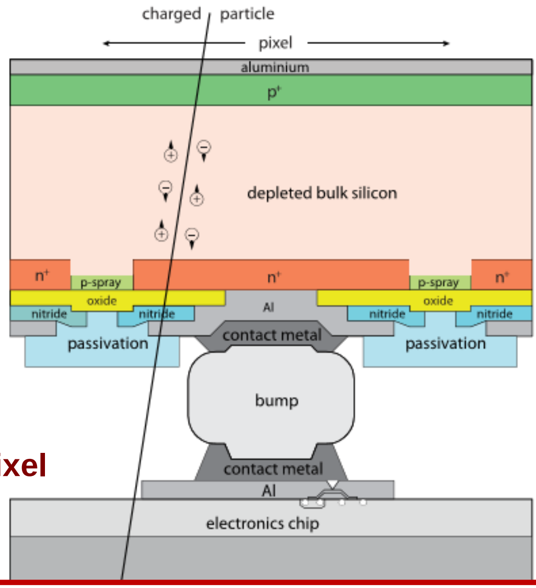
Monolithic Active Pixel Detectors



CALICE/FCC (Tpixel) MAPS EM-calorimeter

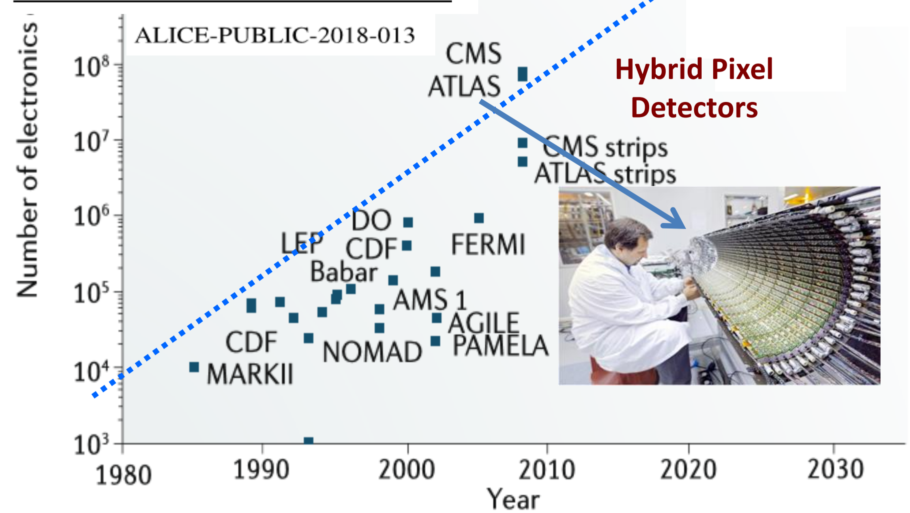
ALICE ITS 10 m² MAPS

Upgrades: ATLAS CMS



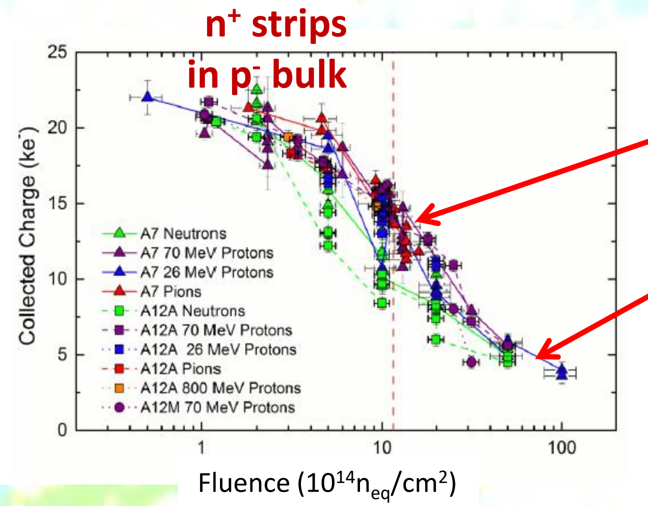
Hybrid Pixel Readout ASICs

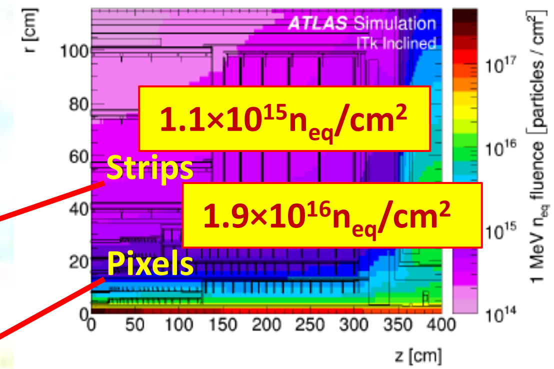
Minimum feature size	250nm	130nm	65nm
Example Read-out Hybrid Pixel Chips	ATLAS FE-I3 CMS Medipix	NA62 TDCPix ATLAS IBL FE-I4 LHCb VeloPix Medipix3RX TimePix3	CLICpix RD53A TimePix4
Typical hit data storage density capabilities	<1Gb/s/cm^2	~5Gbp/s/cm^2	40Gb/s/cm^2
Output Bandwidth	40-160 Mb/s	0.3-1.2 Gb/s	2-20 Gb/s



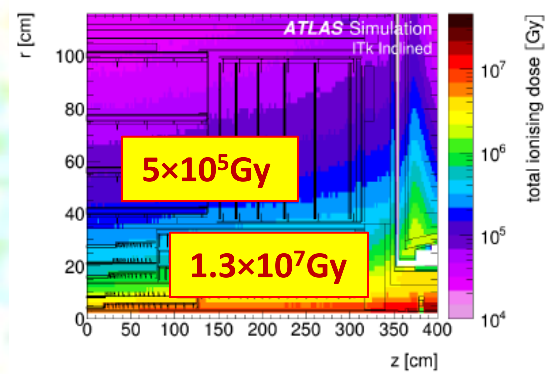
Radiation Effects: Sensors and Electronics

- Hybrid silicon detectors (pixels/strips) **signal** output drops with irradiation to very high doses



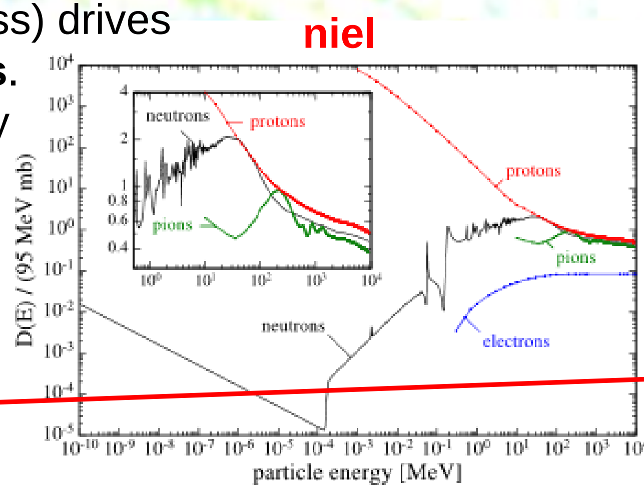


Example of radiation expected at High Luminosity LHC (HL-LHC)
(Typically apply 1.5 safety factor)

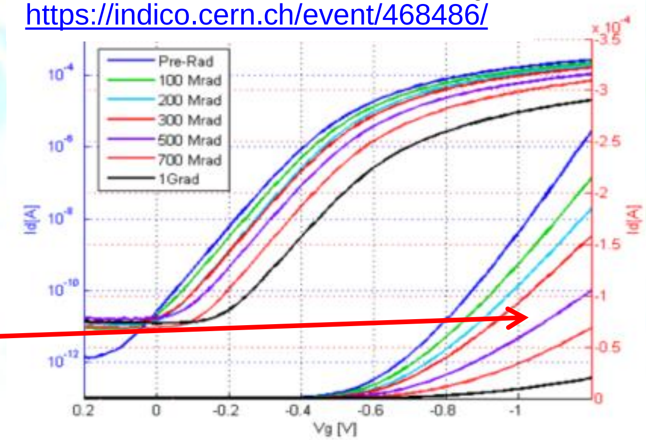


For Monolithic CMOS sensors initially target $\sim10^{15}n_{eq}/cm^2$

- **Bulk damage** (measured in units of 1MeV equivalent neutrons/cm^2 (assuming scaling with **n**on-**i**onising **e**nergy **l**oss) drives the deterioration of **sensors.**
- For **microelectronics** worry about **t**otal **i**onising **d**ose.
- (65nm CMOS - **RD53**) can start to see significant deterioration above **500Mrad (5MGy)**
  ◊Many different effects◊

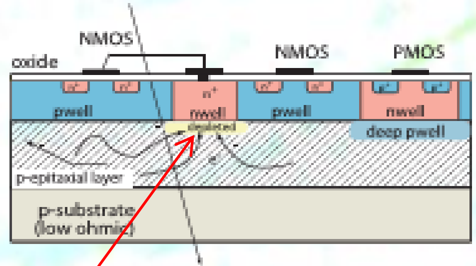


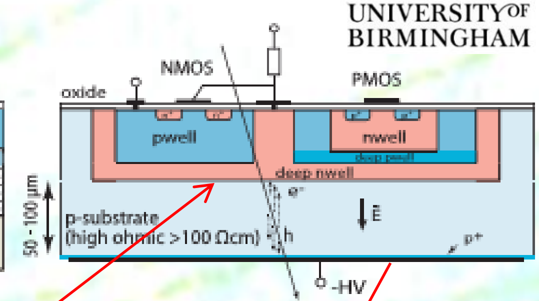
Federico Faccio: PMOS turn-on V_g
https://indico.cern.ch/event/468486/

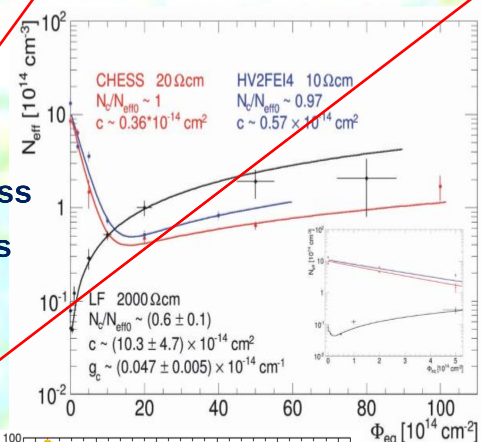


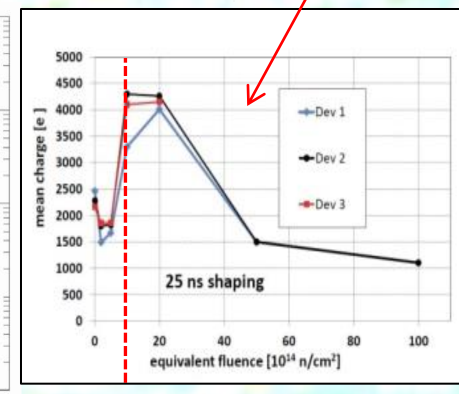
MAPS: HV/HR-CMOS Detectors

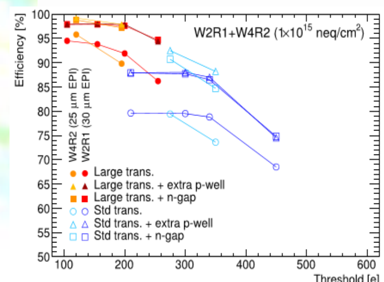
- **Commercial CMOS Image Sensors offer possible dramatic decrease in costs (Monolithic Active Pixel Sensors)**
- **MAPS can deliver very low power consumption at low R/O speeds, possibly <100mW/cm²** **i.e. simple water cooling**
  - **Ultra low material budget (cf ALICE ITS upgrade: <0.5% for inner layers, <1% for outer layers)**
  - **But these devices limited in speed and radiation hardness**
  - **Current and near future MAPS for heavy ion experiments**
    - **integration time up to 4μs (noise, electron diffusion)**
    - **radiation resistance up to few 10^{13} $n_{eq}cm^{-2}$**
- **Major developments in HV/HR-CMOS → deep depletion region with charge collection by drift not diffusion → huge improvements in collection speed and radiation hardness**
- **Can usually either have small collecting node (and therefore faster and low noise) but shallow charge collection or deplete from the deep n-well with larger signal produced in up to 100μm of silicon but higher capacitance (→more noise & slower)**

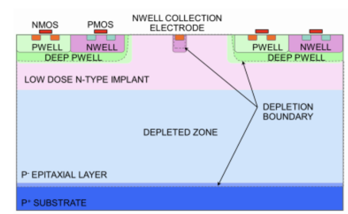








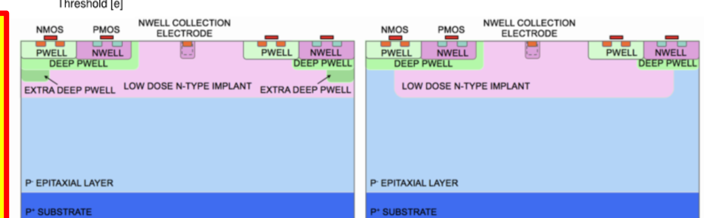




(a) The standard MALTA substrate

Modified process with junction in substrate

See presentation https://indico.cern.ch/event/803258/contributions/3582758/ by Heinz Pernegger



(b) The extra deep p-well (left) and n- gap (right) substrates