Multi-PMT Electronics

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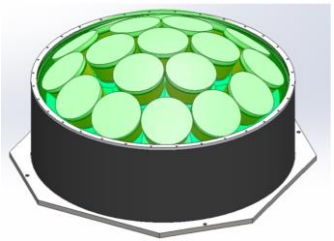
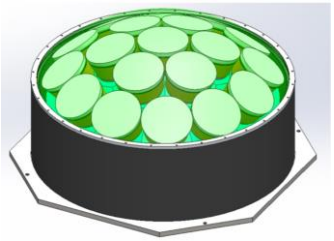
WCTE workshop, Zoom, 2020-11-24

WCTE/IWCD Electronics – Block Diagram





(redundant?)

Copper link
(twisted pairs)

Min. 100 Mb/s,
Max 1 Gb/s

Optical links
(redundant)

MCC

DAQ

Clock system

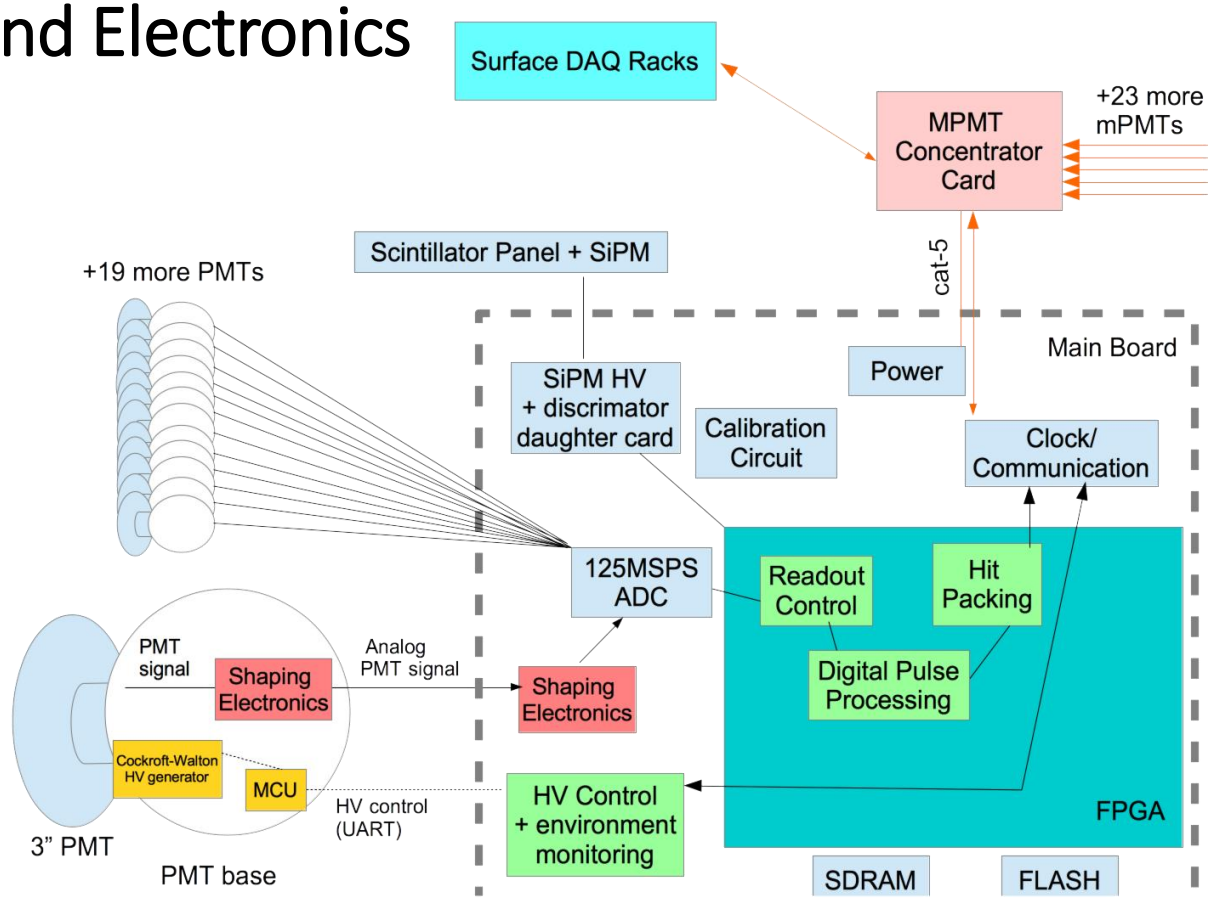
- PMT HV
- Signal digitization
- Feature extraction
- Compression of atypical waveforms

- Pack mPMT data into single stream
- Distribute power and clock
- Apply data compression (?)

- Recording
- Offline processing of complex exents (waveform-level pile-up)
- All other DAQ stuff…

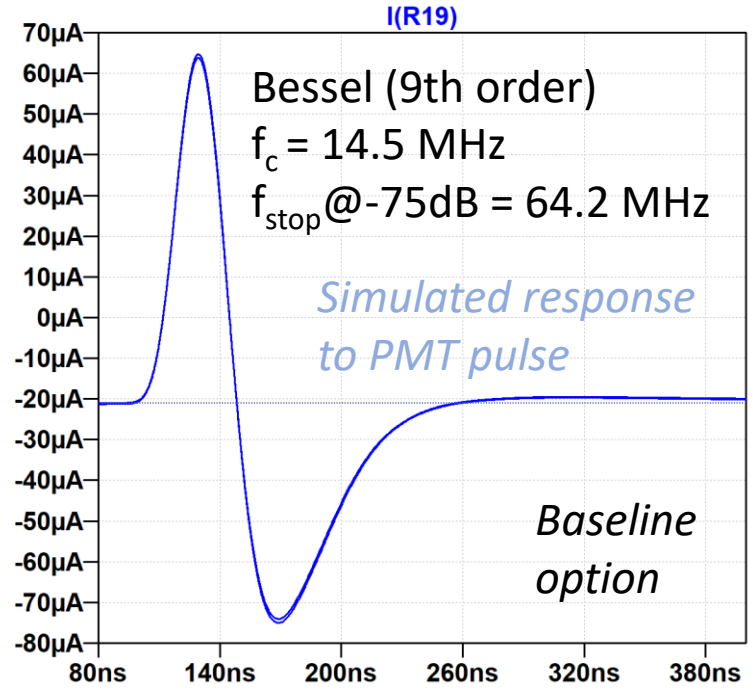
WCTE/IWCD Front-End Electronics

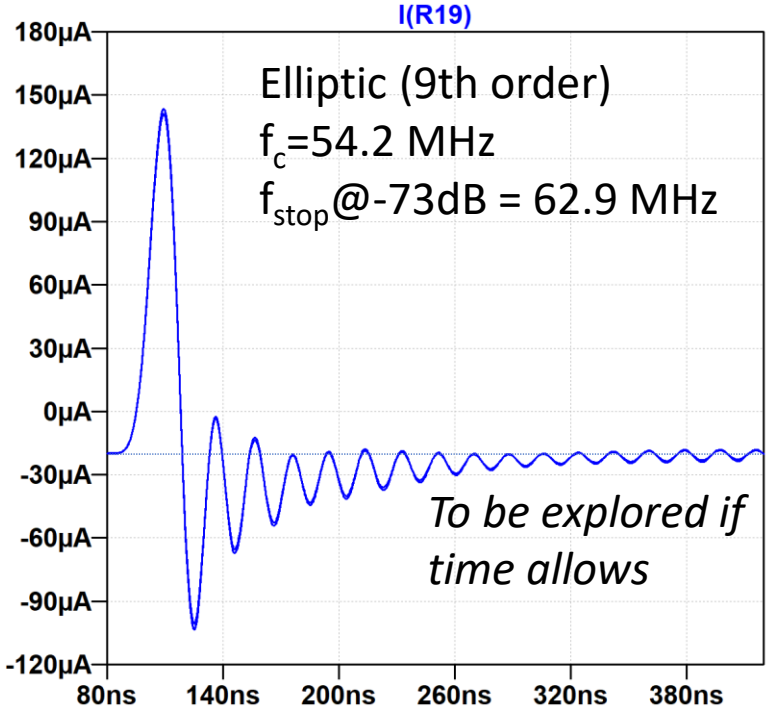
- Good reliability
  - Apply FMECA/FMEDA methodology
- Power <10 W
- Rate tolerance
  - Using waveform digitizer
- Timing & charge resolution < 10% of that of 3” PMT

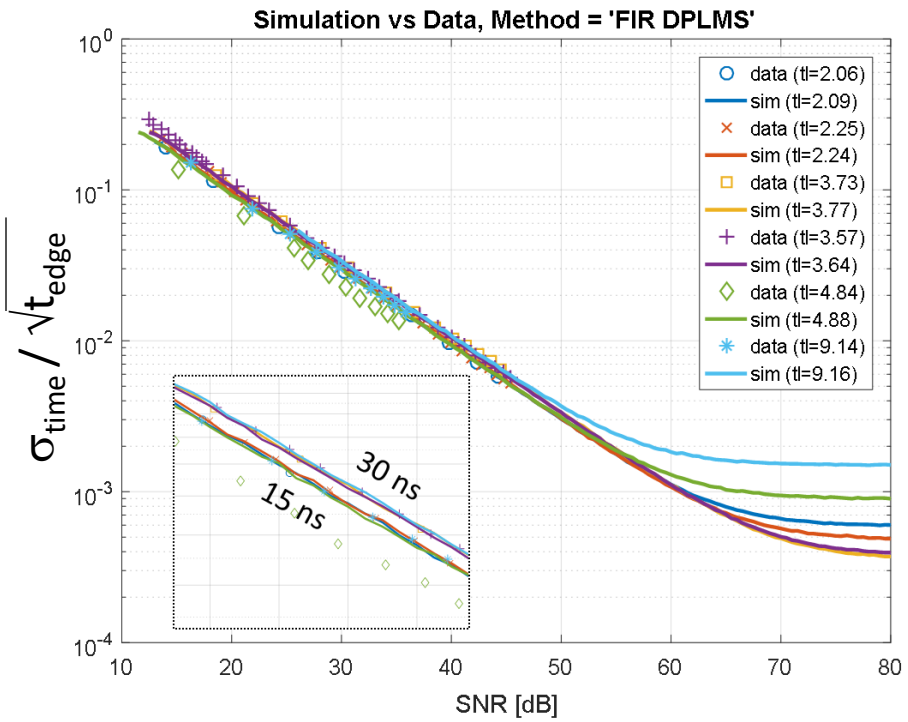


- Self-triggering system – digitize all photo-sensor signals above a certain threshold
- On-the-fly feature extraction and estimation of the quality of the estimates; if unsatisfactory, compress waveform and send full buffer to DAQ
- HV generated at the PMT base

Shaper Investigation







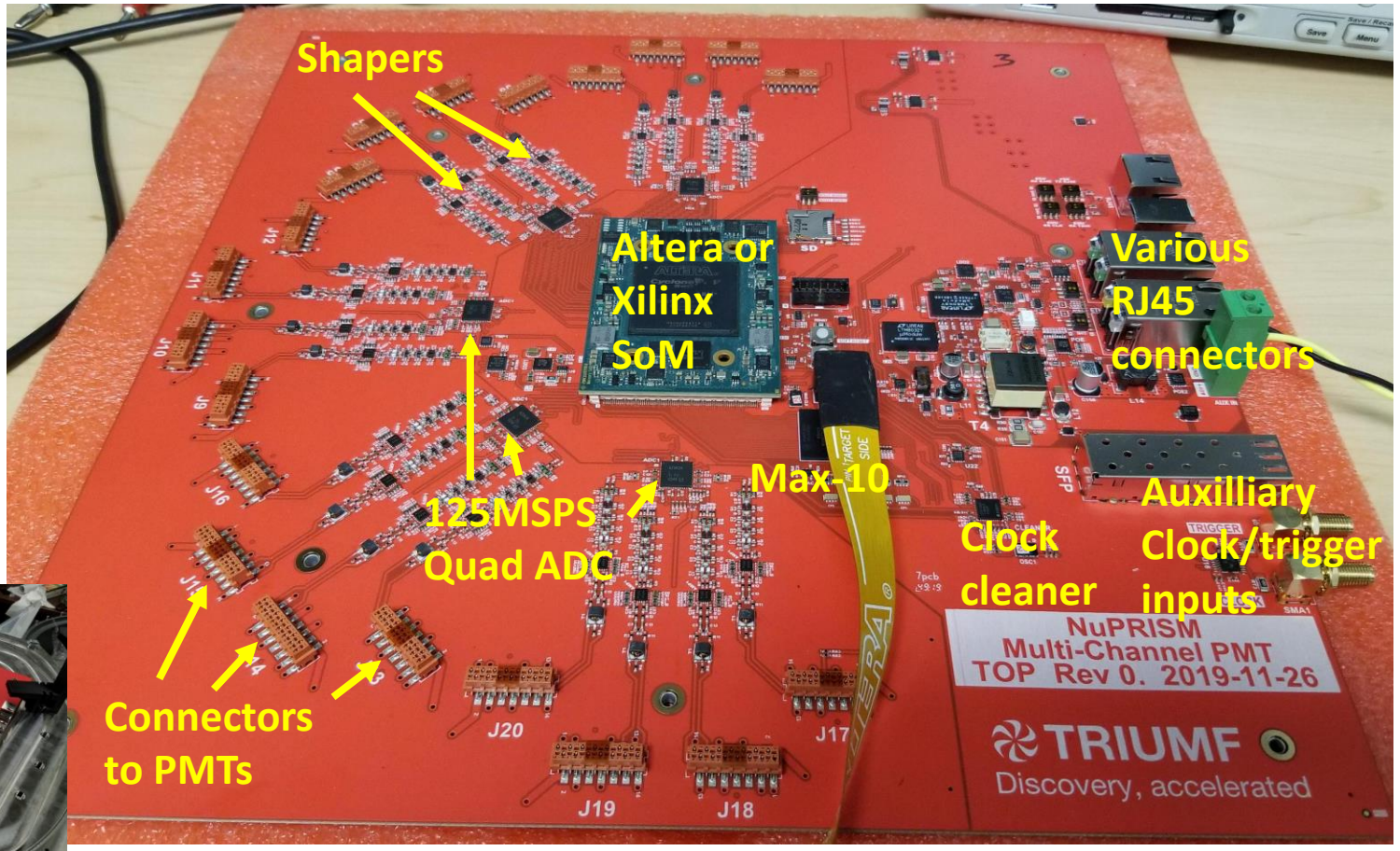
- Don't need extremely high sampling rates to maintain good timing resolution, as long as the SNR is enough → used 125 MSPS ADC
- Prefer to keep sharp Edges → logical, as we don't cut bandwidth of the signal that still has valid information
  - Sharp edges help in waveform-level pile-up resolution
  - Need high order shaping filter

mPMT Mainboard

T. Lindner

- Currently testing prototypes (5 boards)
- Nearly completed work with Altera SoM (without feature extraction).
- Xilinx firmware work in progres (incl. feature extraction)
- Working UART link with front-end card on the PMT base

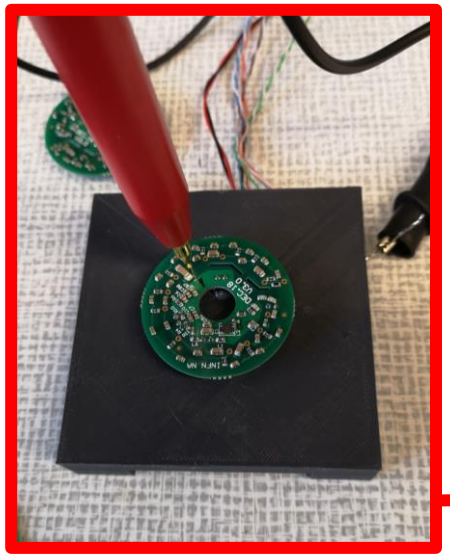
Some layout mistakes have been found, to be corrected in the next revision

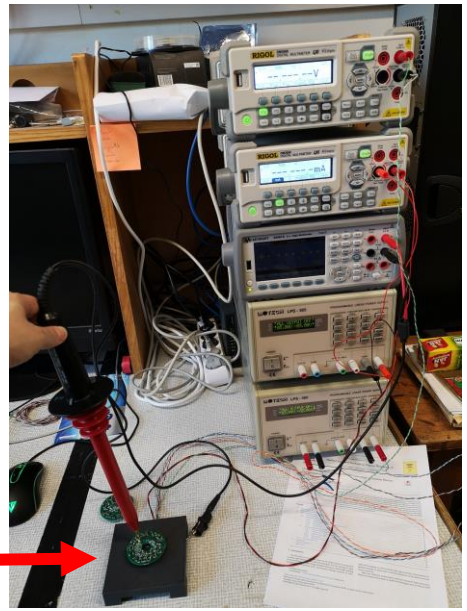


HV/FE Status

- HV multiplier design by INFN (same as far detector)
- Front-end card (controller and signal output) – shared INFN/WUT design
- Negative HV, up to 1500 V
- Confirmed low EMI operation
- Few layout optimizations could be beneficial for mass-scale production and testing

HV probe
(1:1000, R_{IN} = 10 GΩ)



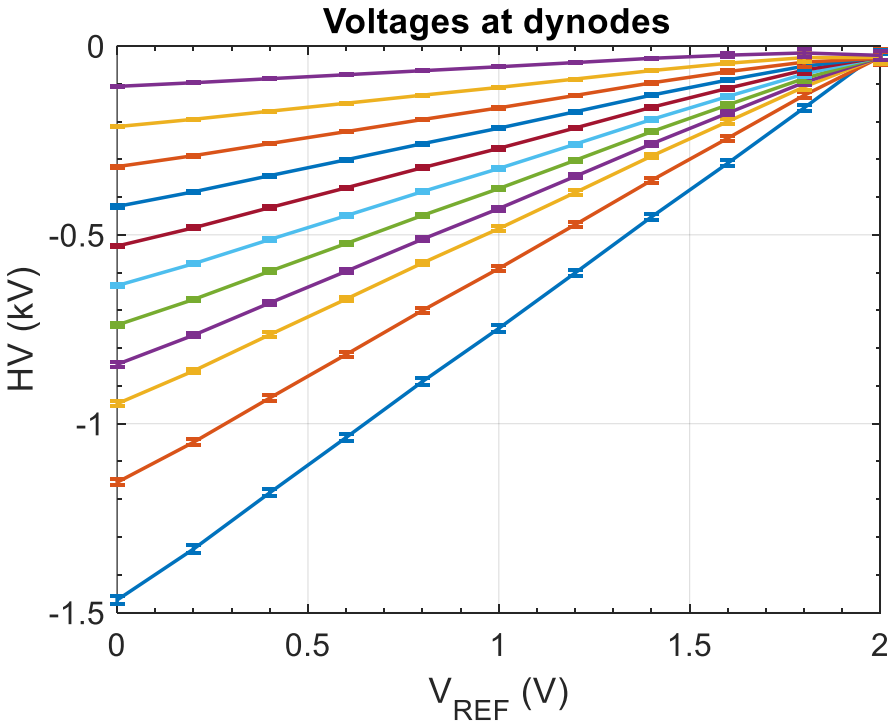


Controller & signal board

HV multiplier (Cockroft-Walton)

Tested first prototypes using a lab test bench

Test results (36 HV boards)



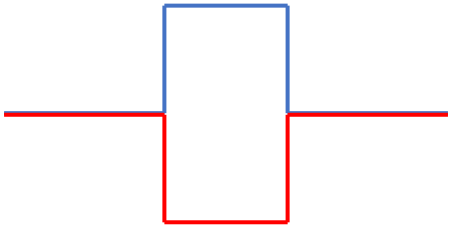
No major problems found

Need to check behavior with large pulses

- Produced 100 HV & FE boards
  - Cost: HV = 43 USD/pcs, FE = 26 USD/pcs
- Current work:
  - Make a device for quick automatic evaluation of the HV board for the assembly line (will give an OK/fail information) – an on-going project at WUT
  - Change communication protocol to save pins on mainboard
  - Change microcontroller and provide new firmware for enchanced diagnostic
  - New FE layout by WUT

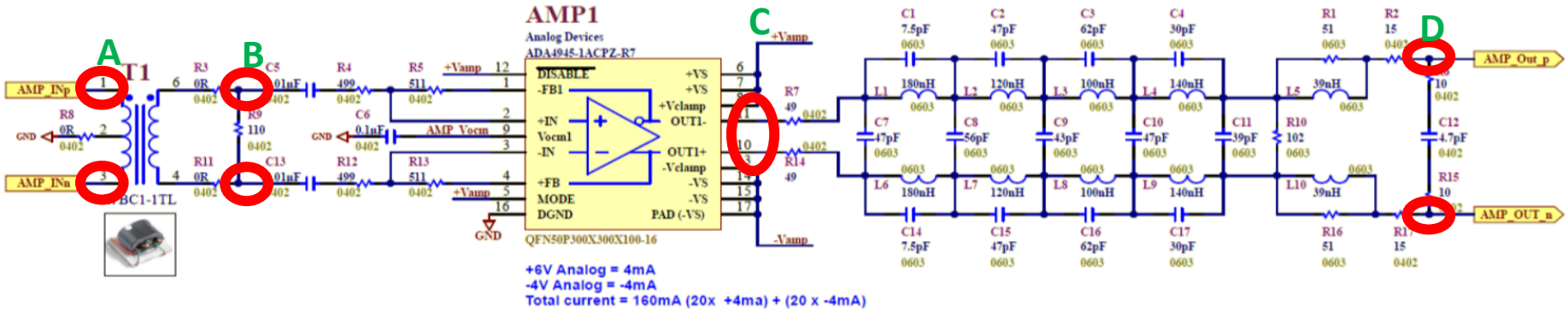
Pulse shape distortion

- See problem with distortion of pulse shape for large pulses and evidence of time slewing (peak of large pulse shifted to later times)
- Expected this to be related to the slew-rate of the amplifier
- Tests done with generator
- Still see some amiguities, but it seems that they are not related to shaper.



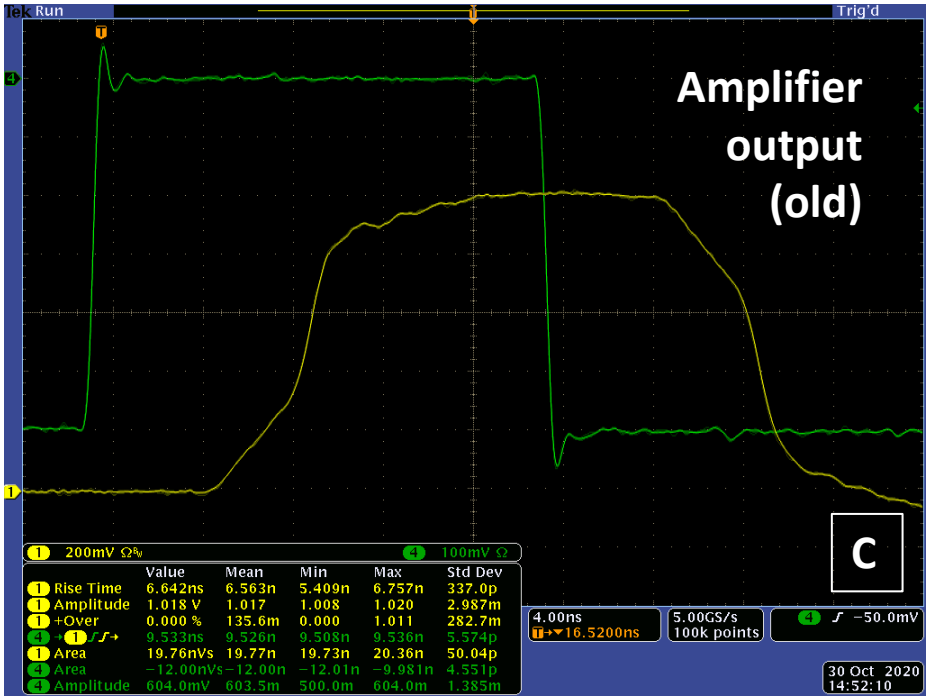
Test pulse – 20 ns wide, 1.6 ns edge, symmetric (2 generator channels), feed via 2 50-ohm coax cables
Later used 6 ns wide

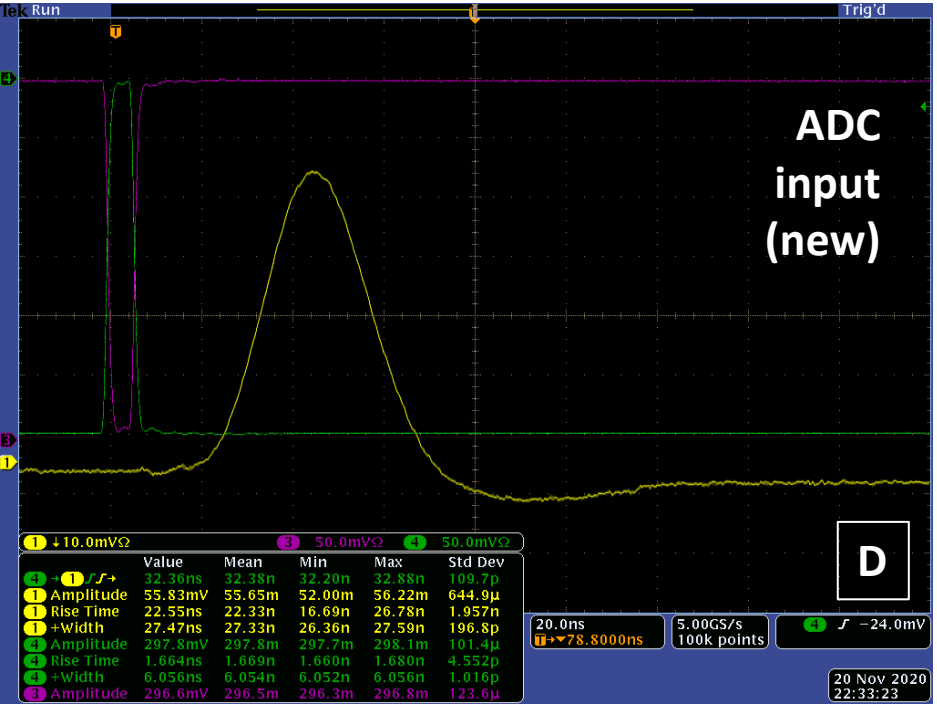
- TDP1500 differential probe
- 1 GHz/5GS Scope (DPO4104)

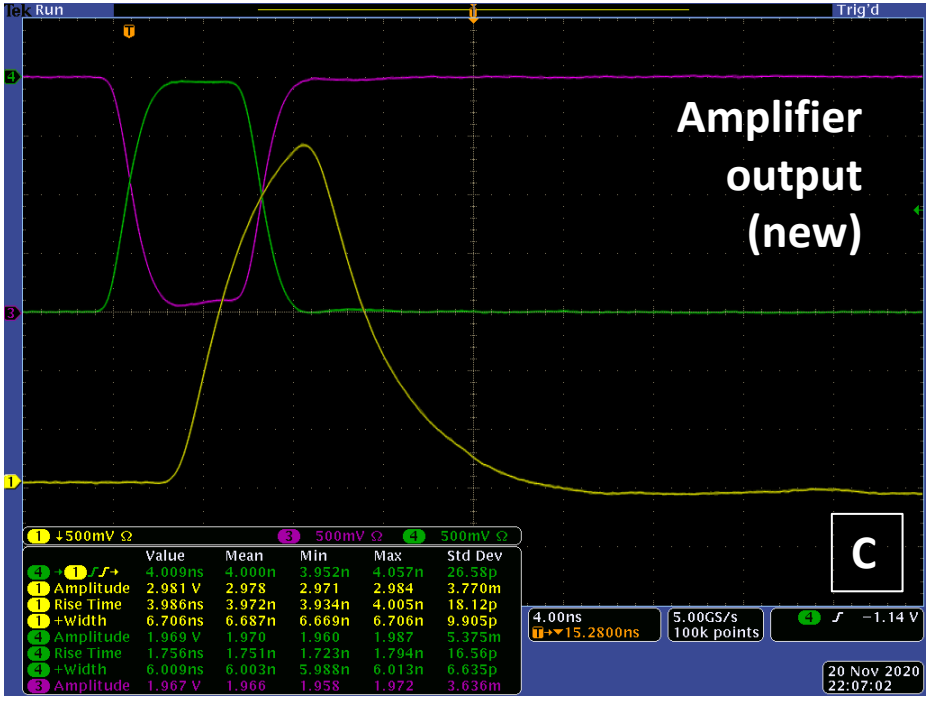


Shaper study

- Found insufficient performance of the initially selected op-amp
- Replaced op-amp to a faster one (90 mW instead of 45 mW per channel)
- Now seems OK
- Preliminary checks show that shaper seems linear (ongoing investigation).

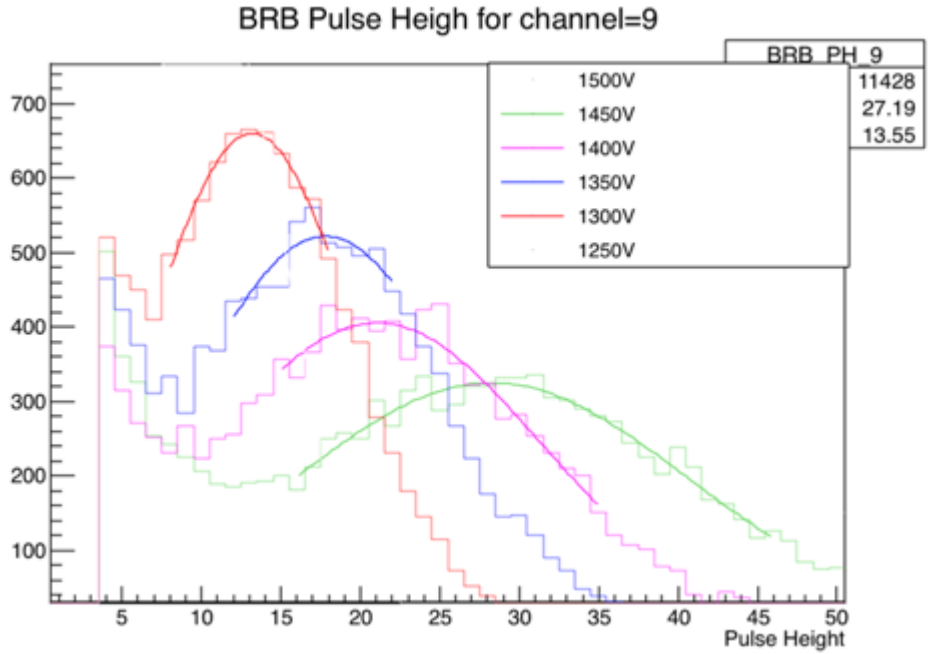


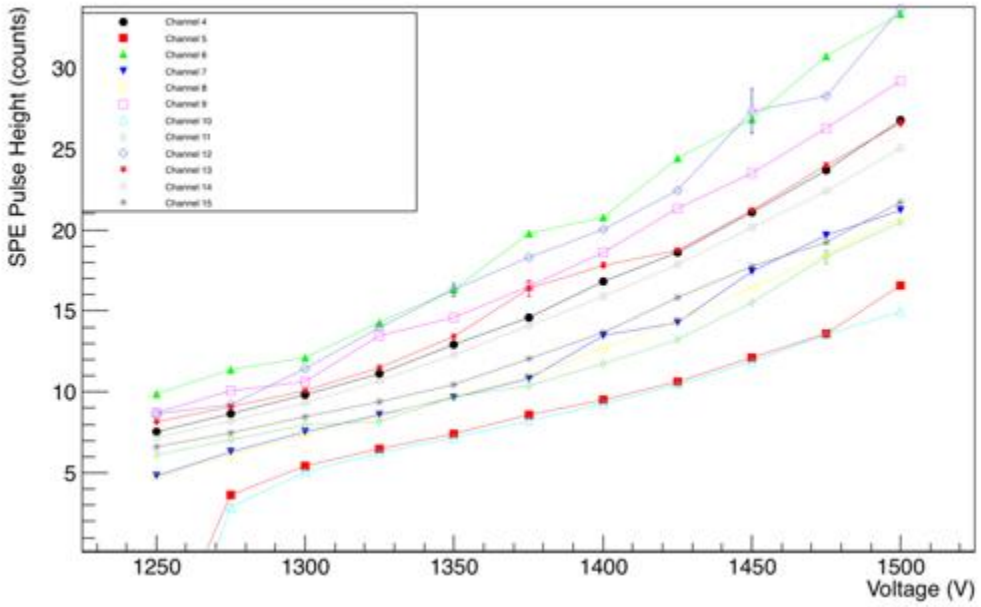




PMT Gain Equalization

- Developed automated scheme for voltage scan and gain equalization.
  - Using MIDAS sequencer
- Currently setting the HV to achieve pulse height of 16 ADC counts (~8mV) for single PE.
  - Implies dynamic range of 0-125PE.
- Believe this corresponds to ~1E7 gain
  - to be confirmed
- Each PMTs draw ~14mW of power; consistent with INFN estimate.

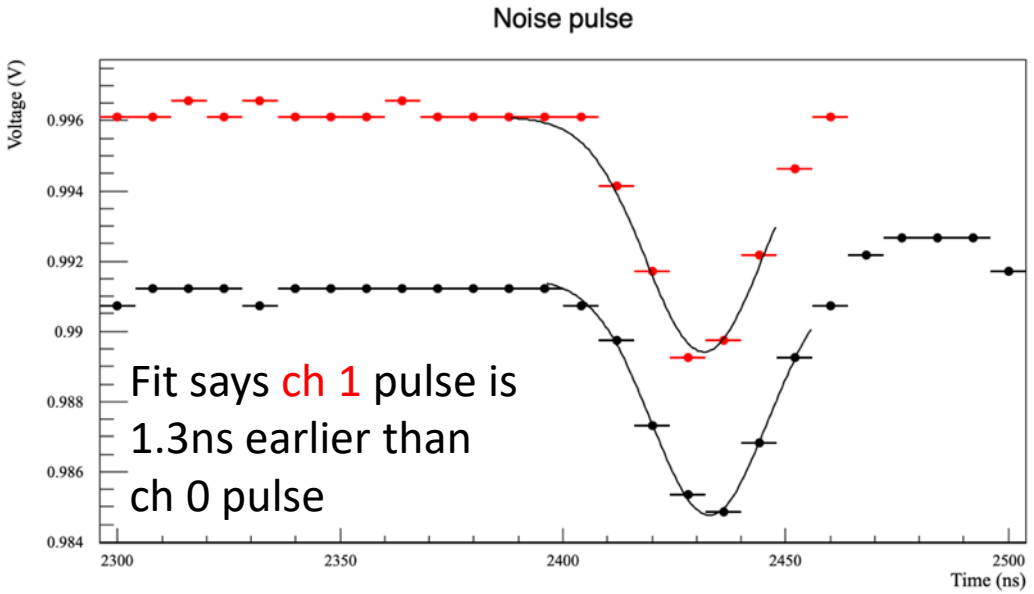


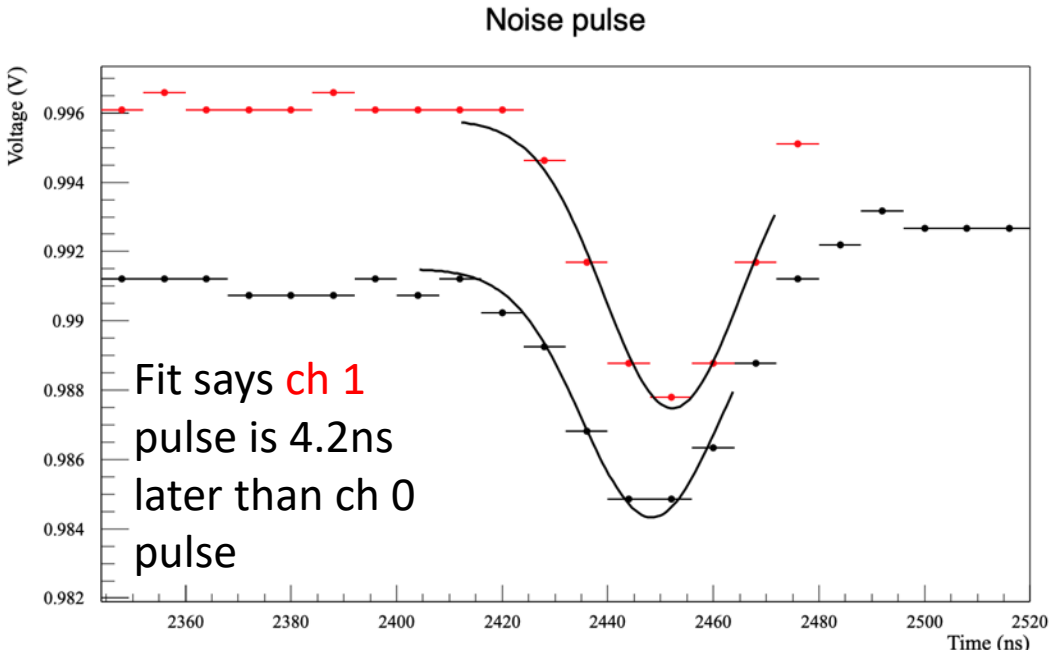


T. Lindner

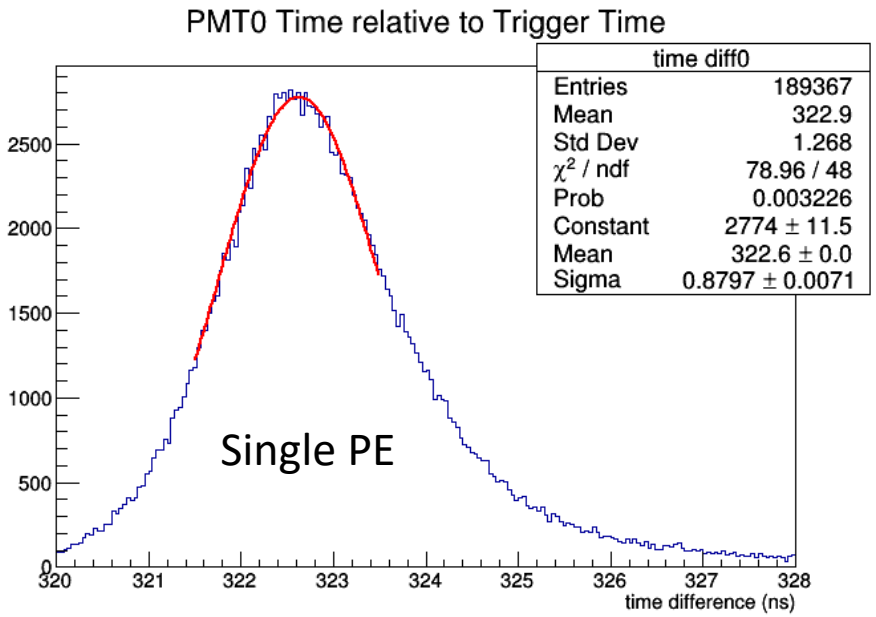
Examples PMT Fits – 1PE

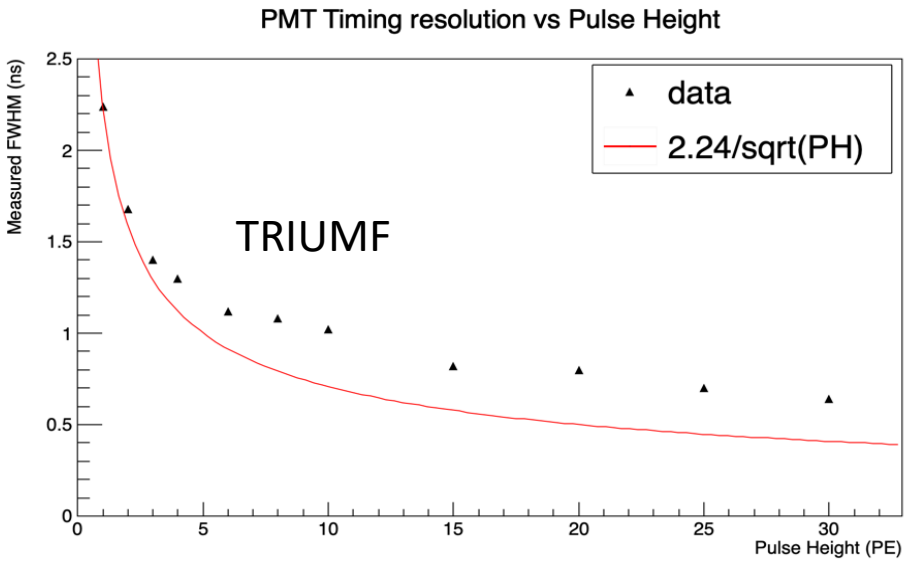
- Fit pulse with exponentially modified gaussian.
- Gaussian mean and amplitude are allowed to float.
  - Pulse shape and offset are fixed.
- Most fits seem reasonably good.
- Already took measurements of step response to derive fit formula based on inverse Laplace transform





PMT 0 hit time relative to injected pulse





- Decide to characterize TTS with FWHM, to make it easier to compare to Tokyo Tech results.
  - Calculate FWHM from data, rather than from fit (use fit to estimate maximum).
- Measured FWHM at 1PE: 2.24ns
  - Compared to 1.65ns in Japanese measurements.
  - Investigating…

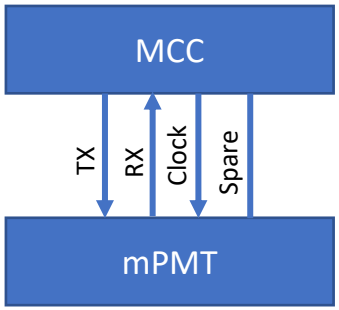
MCC (mPMT Concentrator Card)

- Shared between WCTE/IWCD/Far detector
- Expose mPMTs to the DAQ the same way as 20” tubes
- Pack data from 24 mPMTs to conserve bandwidth
- Receive reference clock and distribute clock and power to mPMTs
  - May change frequency of the reference clock depending on mPMT needs
- Compress data (???)

(*) denotes a spare signal

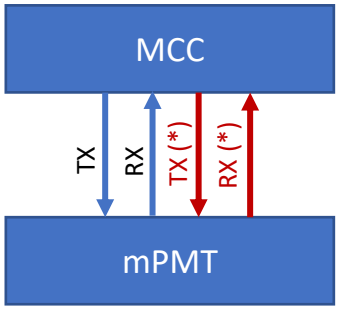
mPMT to MCC connection

Ethernet



- Current baseline
- Both TRIUMF/WUT prototype and INFN prototype currently use this scheme
- No possibility for redundant link
  - But need to verify whether one can attach two transceivers to single cable
- Dedicated clock line – no problem with phase

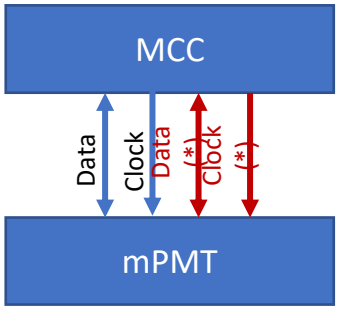
Custom link



- Use LVDS buffers
- Can have custom speed, confirmed to work up to 250 Mbps on 50 m cable
- Possible to make redundant link
- Clock embedded in data, need recovery; R&D needed
- Need to resolve phase ambiguity
- Less resources needed in FPGA

Transmission tests completed in Cracow

Single pair Ethernet

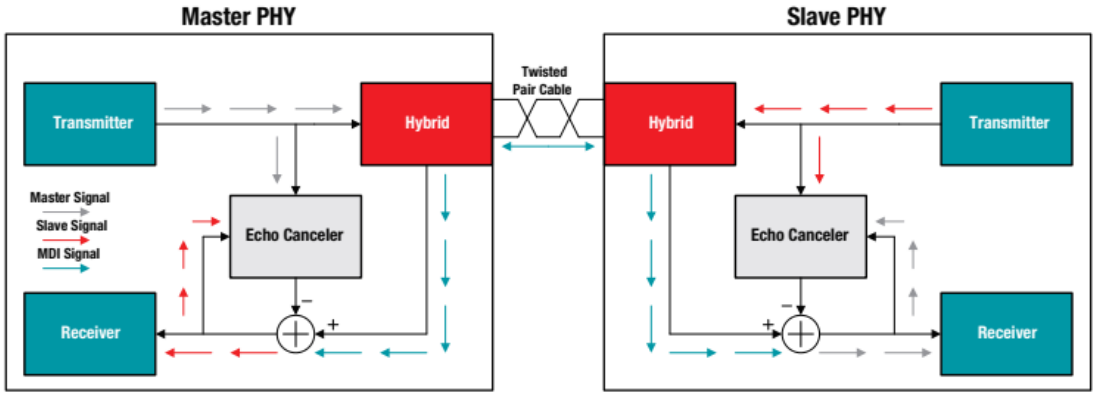


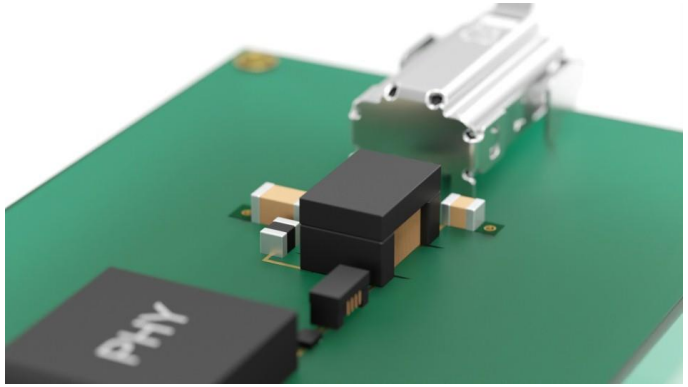
- Automotive standard IEEE 802.3bp
- Potentially less risky than custom link – all is already tested, since it's a standard
- Same transceiver interface as Ethernet – no need for new firmware blocks
- Dedicated clock line – no problem with phase
- Possible to make a redundant link
- Need dedicated transceivers – currently found that Texas Instruments and Marvell supply them, but only these two companies so far

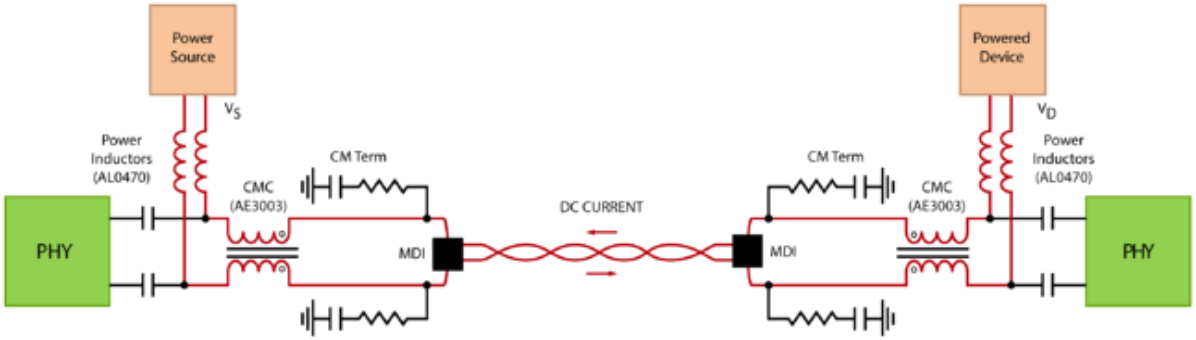
Start testing at WUT from early October

MCC – mPMT link

- Single Pair Ethernet
  - One pair for bidirectional link
  - One pair for clock – no need to encode it in data
  - 2 other pairs as backup
- It's a standard - IEEE 802.3bp
  - Less risky than custom link, but less flexible
- Power delivery is also standardized, though we may need to build our own circuit due to amount of needed power
  - Guidelines provided in the standard
- Need dedicated transceivers from Marvell (1 Gbps) or Texas Instruments (100 Mbps)
- Standard specifies Cat7 cable, but allows 4 interconnects; we will only have 2 interconnects

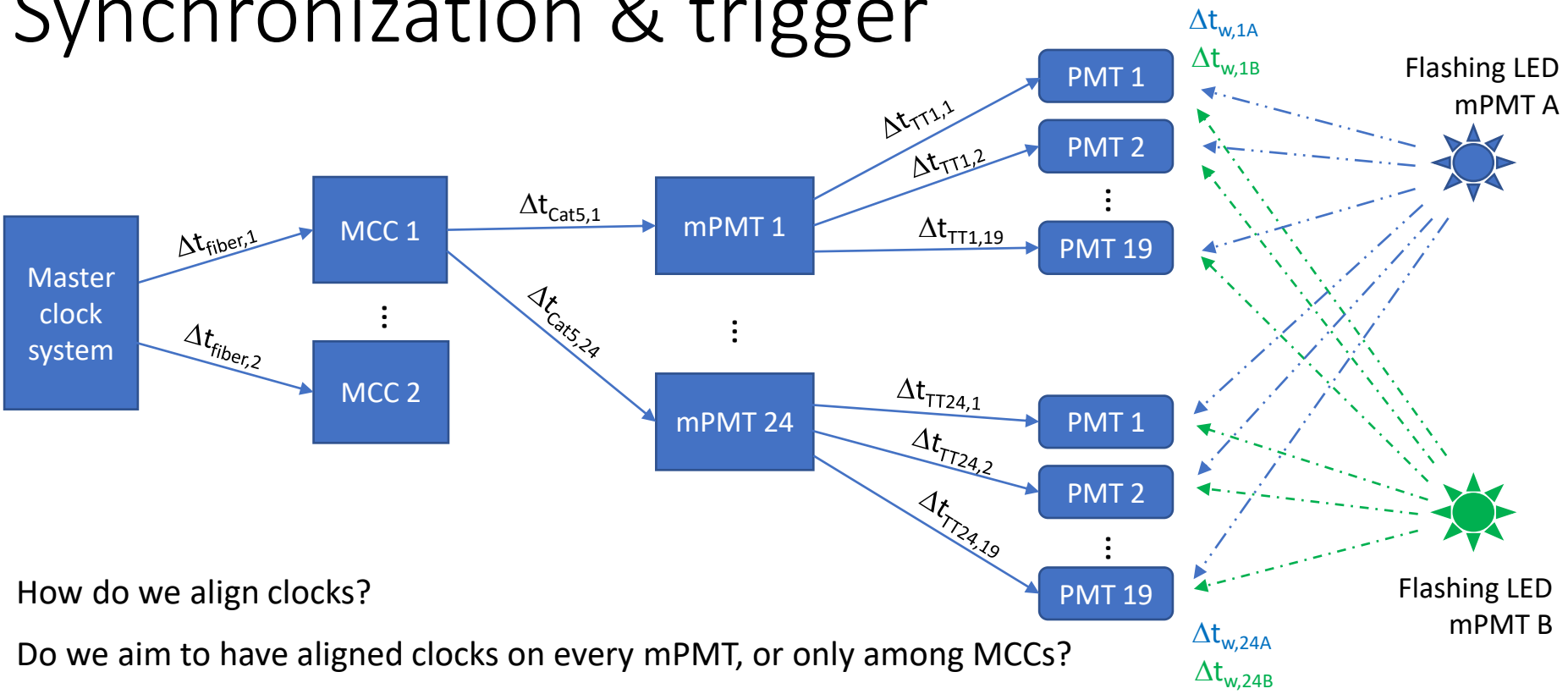






Currently being tested at WUT

Synchronization & trigger



- How do we align clocks?
- Do we aim to have aligned clocks on every mPMT, or only among MCCs?
- Cat5 cable will introduce offsets among mPMTs connected to the same MCC due to inter-pair skew, even if length of the cables is the same (up to 50 ns - IEEE Std 802.3-2008).
- What about fibers – do we need to account for fiber skew?
- We will anyway have uncertainties due to transit time of PMTs. So, so we need to align clock phase at all? To me we anyway need calibration from LED or other light source inside detector, to time-align every individual channel.
- It was shown that such a calibration is possible with LED flashers built into mPMTs, even if all delays are unknown at the beginning (at least this is my understanding).
- Do we need a dedicated trigger line or can the trigger be encoded in data. Purpose of the trigger?

Plans

- Goals for Rev 1 (Jan 2021)
  - Further prototyping, another 15 boards
  - Fix errors found with rev 0
  - Add scintillator power/readout board (need interface)
  - Add connector for LED driver board
  - Improve FPGA flash/boot hardware
  - Remove Max-10 – possible due to switch to MODBUS communication with the controllers on FE; now using bus-topology rather than dedicated UART lines (with safeguards)
  - Add mezzanine connector for single-pair Ethernet
  - Switch to readout optimized for Xilinx SoM
  - Finalize shaping circuit
- Goals for Rev 2 (April 2021?)
  - For full WCTE production : 30-120 boards
- MCC
  - Cracow now developing initial firmware to estimate required FPGA size
  - MCC will also use mezzanines for connections to mPMTs, to allow for easy switch of comm-link in case we choose to do so.
  - Clock receiver will be provided by the French group in a form of mezzanine

Summary

- Prototypes of mPMT electronics produced, already got first data
  - Some problems found, seem solvable (ongoing investigation)
  - Will soon test feature extraction on actual signals
  - Plan for rev 1 in early 2021
- Got substantial experience with HV & FE boards
  - Need slightly larger holes on HV boards
  - Could use extra header for testing FE cards
  - Will modify the original INFN firmware and the front-end card itself.
- MCC development slightly delayed due to COVID.
- Many students are working on characterizing PMTs
  - Still plenty of work to do
- Other welcome contributions:
  - Slow control
  - LV supply
    - Maybe we could rent it from CERN E-pool – though we need approx. 2-3 kW 48V power supply, so need to check if it is available