



Muon Detector Upgrade

Electronics for the Upgrade



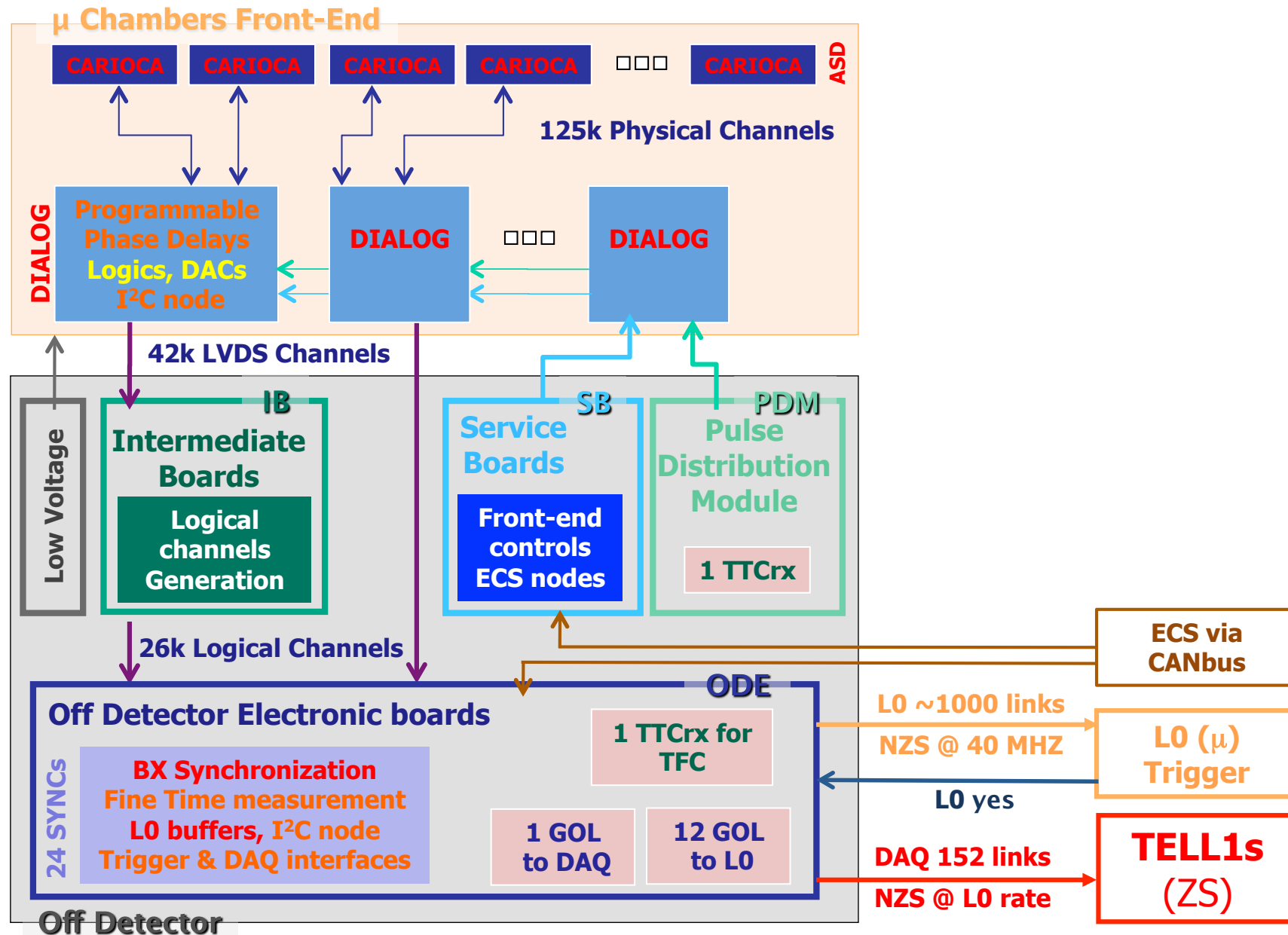
Starting points

- L0 Muon trigger will (most probably!) stay as it is now
- ODIN will send data both with the TTCrx and the GBTX links
 - The interaction trigger will be received by the ODE and could be used to select a set of event to be send to TELL40 with the TDC information
- M1 eliminated
 - There will be only 104 ODE (M2 to M5)
 - The M1 48 ODE could be used as “spares”
- Under these hypothesis the electronics upgrade could consist:
 - No change into the cavern: no change on the ODE board
 - Add a new board: a translation board
 - In D3?
 - No radiation zone → commercial components can be used

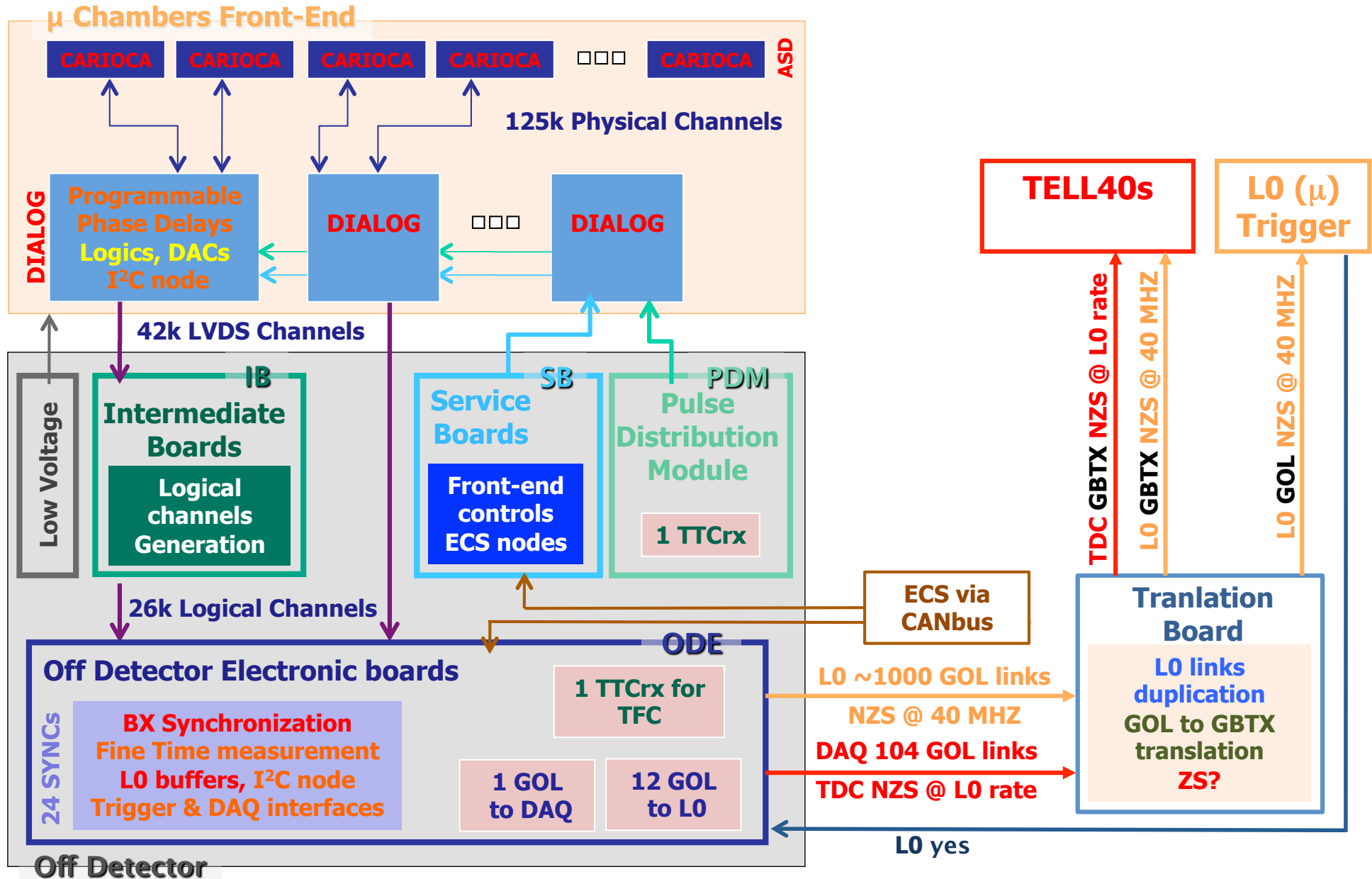
Translation Board

- Input →
 1. L0 links @ 40 MHz from ODE (32 bits GOL protocol); NZS bit/channel information
 - 104 bundles of 12 fibers each
 2. DAQ link @ 1 MHz from ODE (32 bits GOL protocol); NZS TDC/channel information
 - 104 single fibers
- Behavior:
 - Duplicate the L0 link NZS bit/channel information
 - The first link to be forwarded to L0mu with the GOL protocol
 - The second link to be converted into GBTX protocol and sent to the TELL40
 - Convert the DAQ link NZS TDC/channel information
 - From GOL to GBTX protocol
- Output ←
 1. L0 links @ 40 MHz to L0mu (32 bits GOL protocol); NZS bit/channel information
 2. L0 links @ 40 MHz to TELL40 (68 data-bits GBTX protocol); NZS bit/channel information
 3. DAQ link @ 1 MHz to TELL40 (68 data-bits GBTX protocol); NZS TDC/channel information

Present Muon Electronics Architecture



Minimal Upgrade → Case-A --



Conclusions

1. Only this Case-A - - is under evaluation if:
 - L0 muon trigger will stay as it is
 - TTCrx will be maintained on new ODIN
 - Do we consider this minimal architecture valid even if the L0mu trigger will change?
2. Currently **NO responsibility** has been taken with respect to the electronics development, implementation and commissioning
 - The development of the Translation Board could start after the LHCb upgrade approval and in any case not before of 2 years from now
3. Which kind of details have we to specify before put the project in standby?
 1. An approved documentation with the requirements (no change on L0mu, TTCrx protocol and ECS)
 2. Count and evaluation of spares (all devices related to FEE, ECS, ODE ...)
 3. ...

Architectures Cases

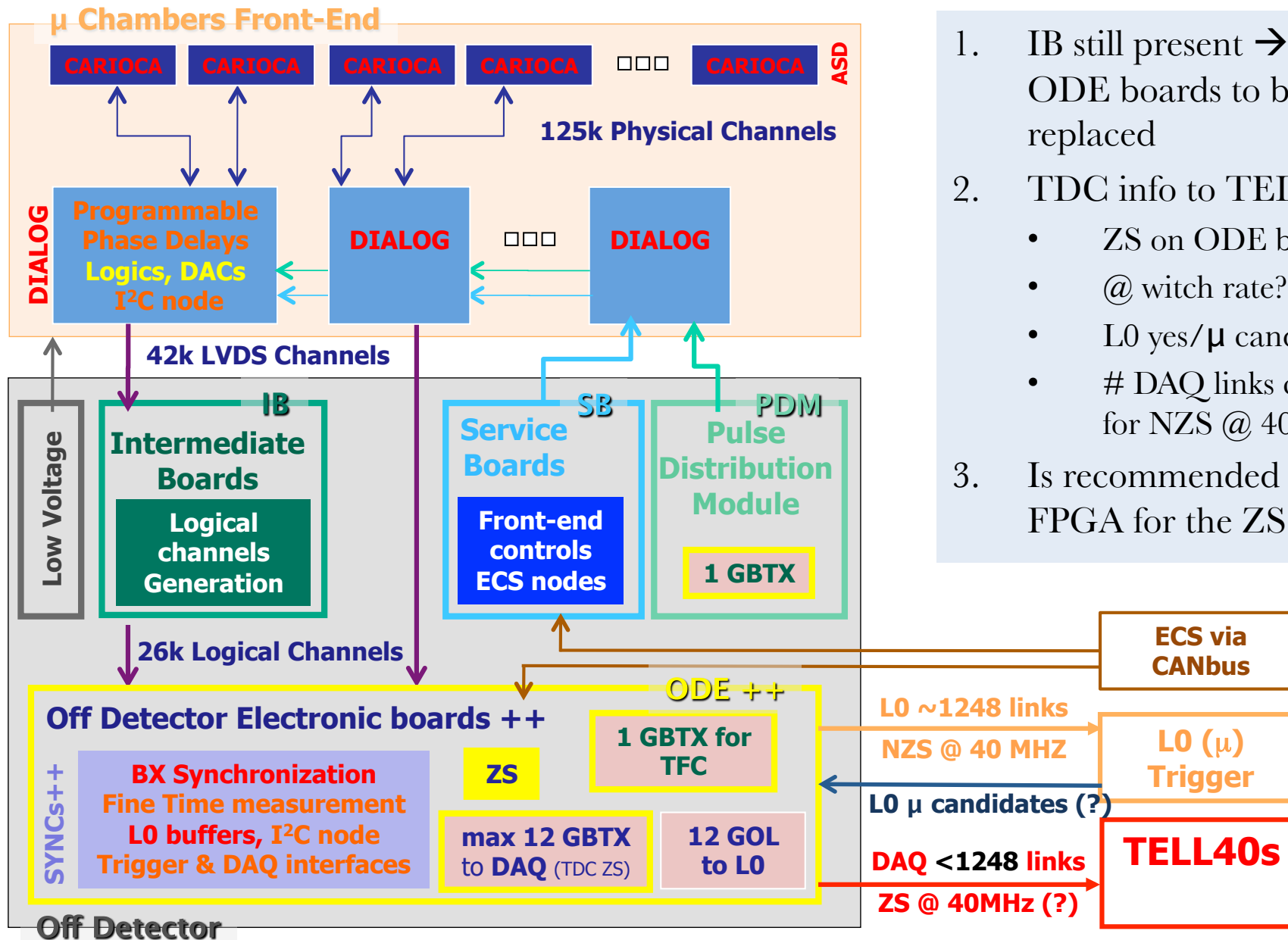
Case-A: minimal upgrade

- L0 links
 - **L0 trigger does not change** at all and the new ODE must have the same L0 interface
 - Trigger Sector information must be maintained
 - Intermediate Boards cannot be eliminated
 - send the bit/channel **NZS** information @ 40 MHz with the GOL chip (we could not have enough GOL chips!)
 - can the ODE have back the L0 mu candidates? → TDC data selection
- DAQ links
 - the ODE must send the bit/TDC channels information **ZS (?)** to the TELL40 using the GBTX (@ witch rate? L0 trigger if any or with random rate?)
- ECS & TFC
 - ECS with ELMB via CAN bus
 - TTC data via GBTX

Case-B: upgrade

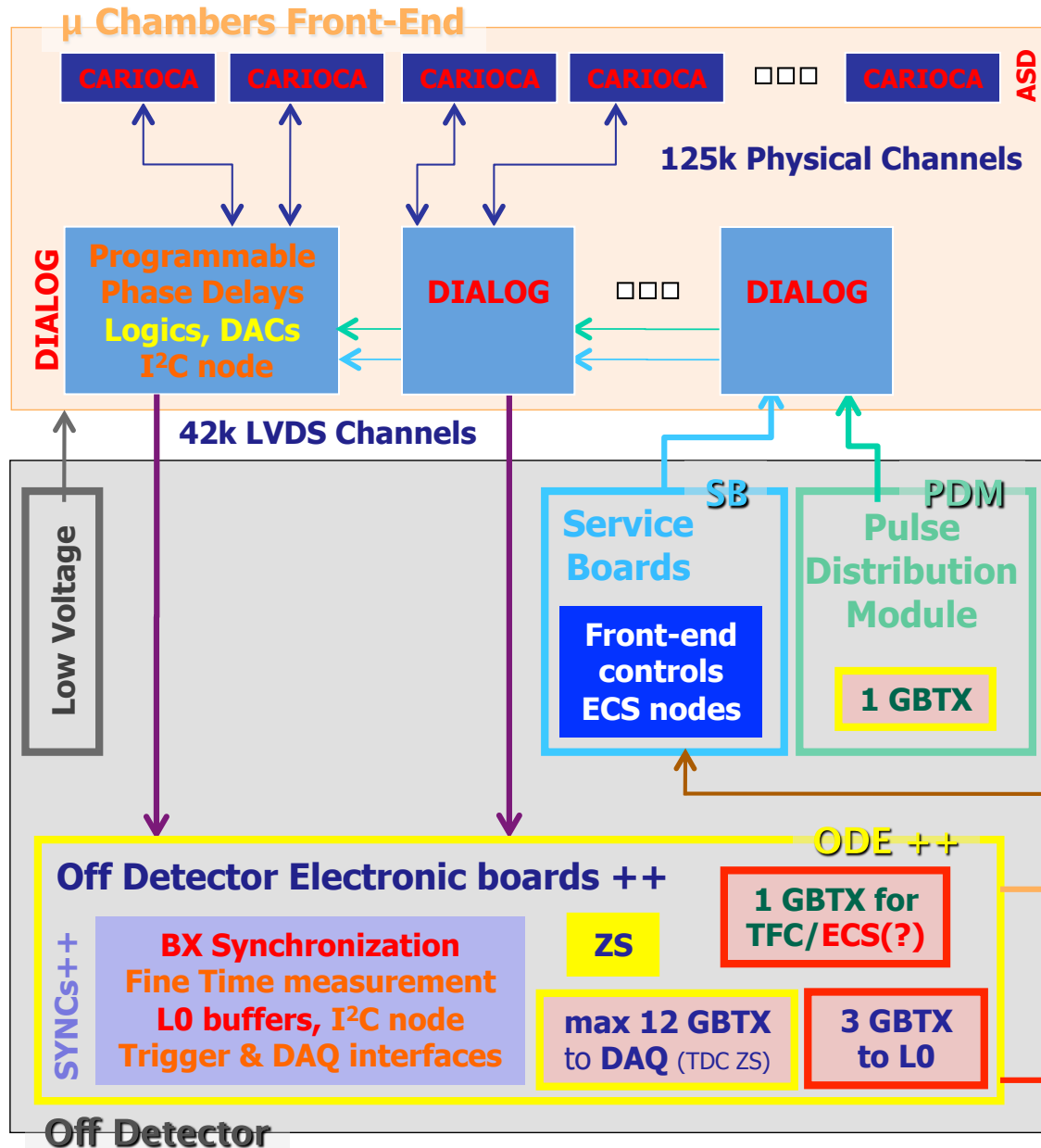
- L0 links
 - L0 trigger WILL change
 - ~~• Trigger Sector information~~
 - ~~• Intermediate Boards~~
 - send the bit/channel **NZS** information @ 40 MHz with the GBTX
- DAQ links
 - the ODE must send the bit/TDC channels information **ZS** to the TELL40 using the GBTX (@ witch rate?)
- ECS & TFC
 - ECS with ELMB via CAN bus or via GBTX to be decided
 - TTC data via GBTX

Minimal Upgrade → Case-A



1. IB still present → only 104 ODE boards to be replaced
2. TDC info to TELL40
 - ZS on ODE board?
 - @ witch rate?
 - L0 yes/μ candidates?
 - # DAQ links calculated for NZS @ 40 MHz
3. Is recommended to use FPGA for the ZS

Upgrade → Case-B



1. IB eliminated → 200 ODE boards to be replaced
2. TDC info to TELL40
 - ZS on ODE board
 - @ witch rate? Random trigger? No trigger from L0
 - # DAQ links calculated for NZS @ 40 MHz
3. ODE ECS via GBTX with TFC (?)
4. Is recommended to use FPGA for the ZS

