



1st CERN Baltic Conference (CBC 2021)

June 28, 2021



**TAL
TECH**

Test System HW/SW for LHC Data Links and Other Projects Done for CERN and ESS

Artur Jutman



Inventor of Embedded Virtual Instruments

Solutions in
20+ countries

Patented
in 2013



Testonica



Testing Right From the Inside

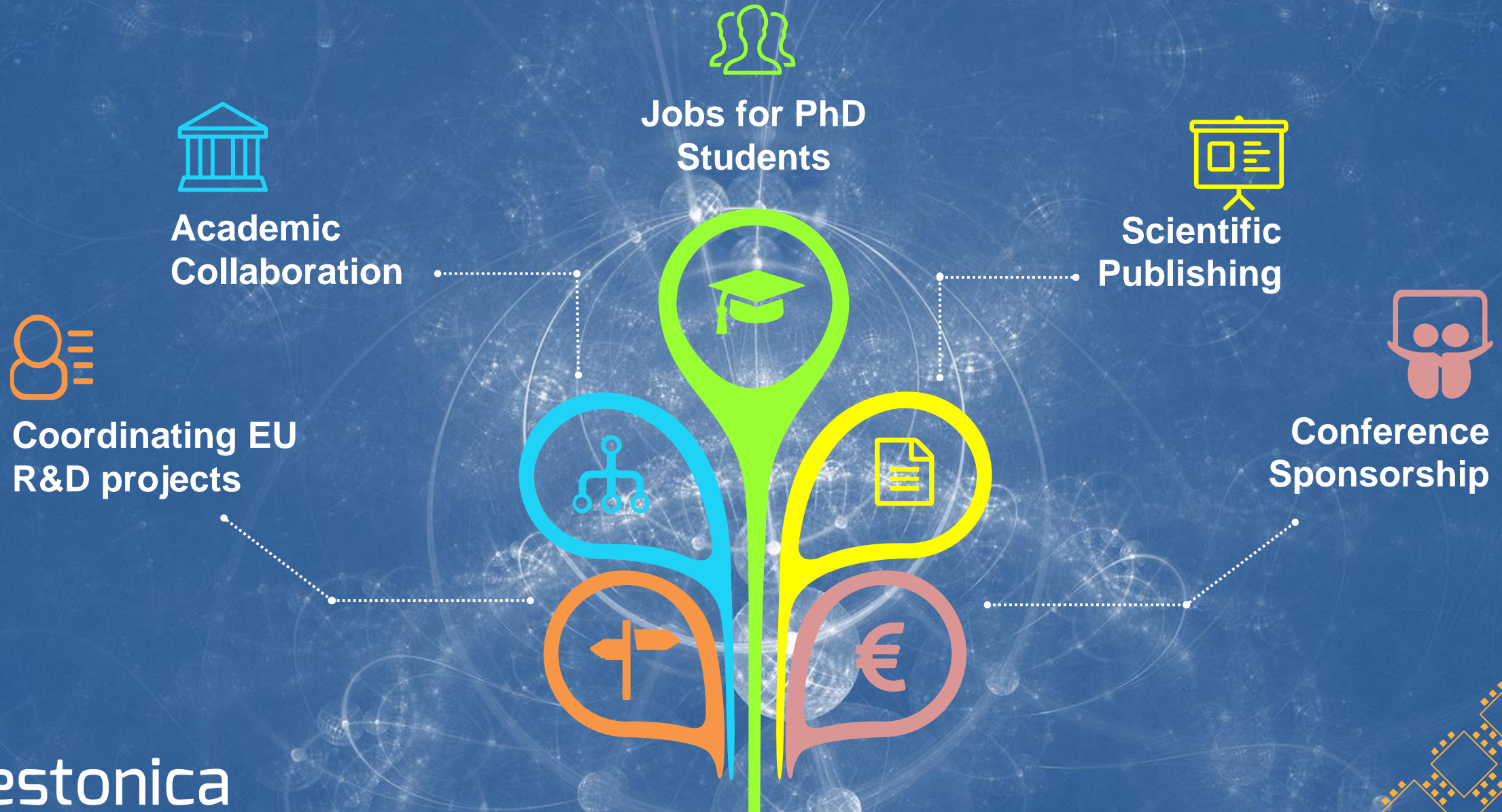
QUICK
instruments

Tester
on Chip

External
Tester

At Speed. Always.

We Invest In R&D and Support The Community

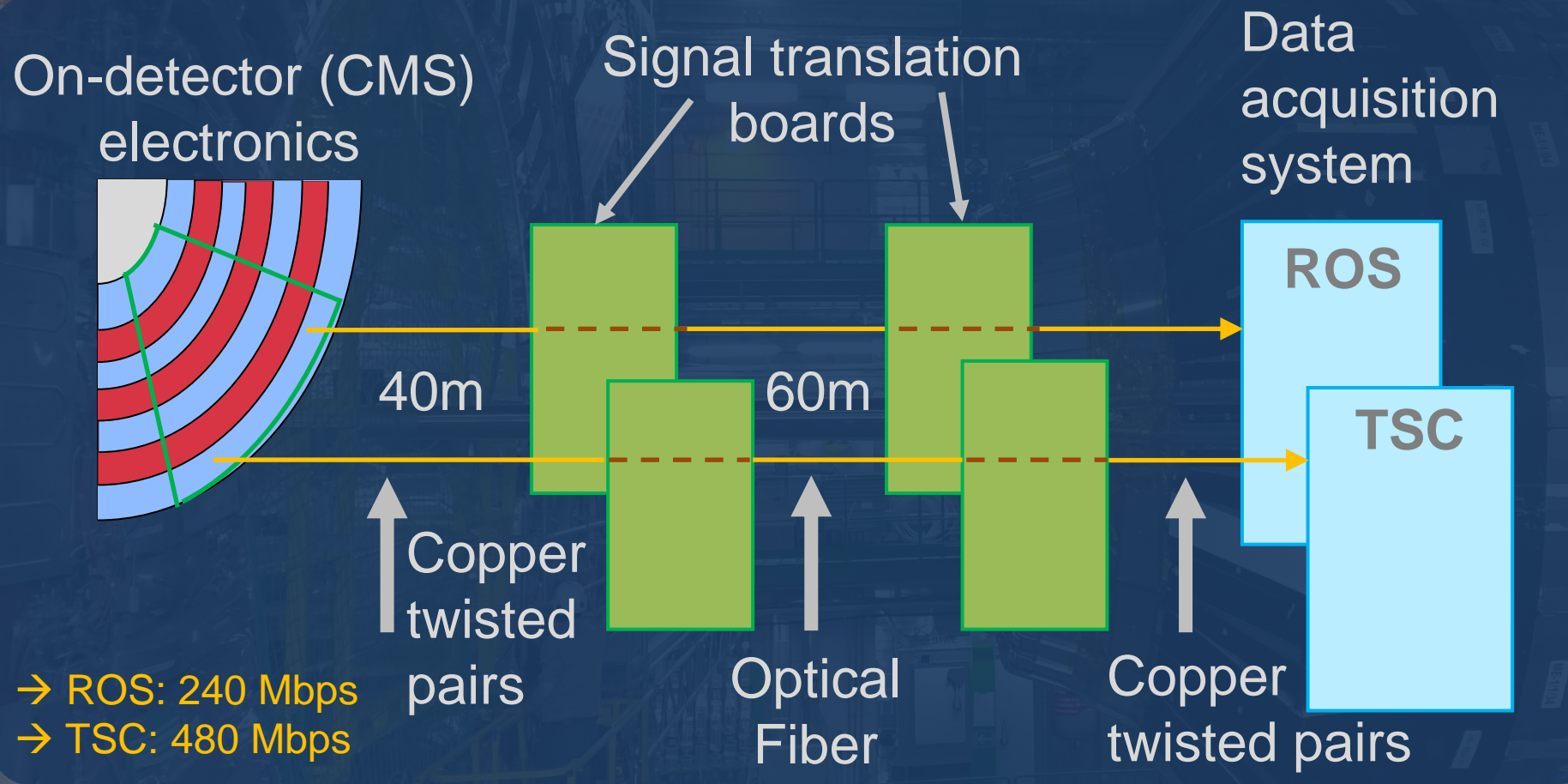


Presentation Outline

- ❖ Custom BERT Equipment – 2011
- ❖ Tau lepton decay triggering algorithm – 2020
- ❖ ESS/ERIC: FPGA-Based I/O and Control System



CMS Data Links



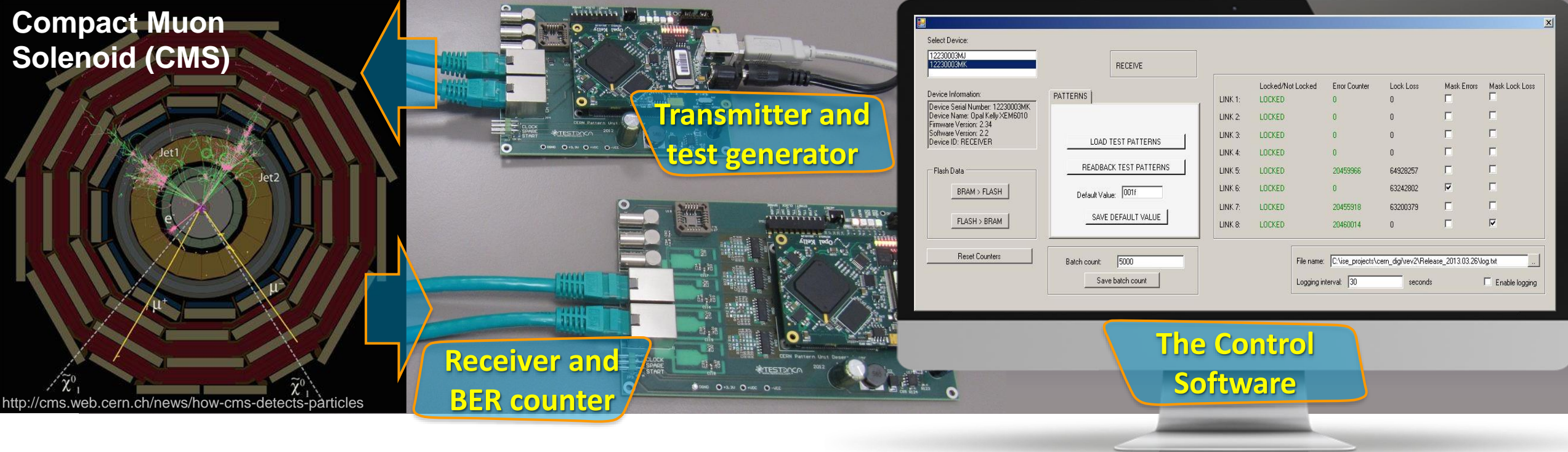
Problem:

- signal integrity
- full custom design

Needs:

- end-to-end test
- push-button start
- autonomous exec
- HW and SW dev

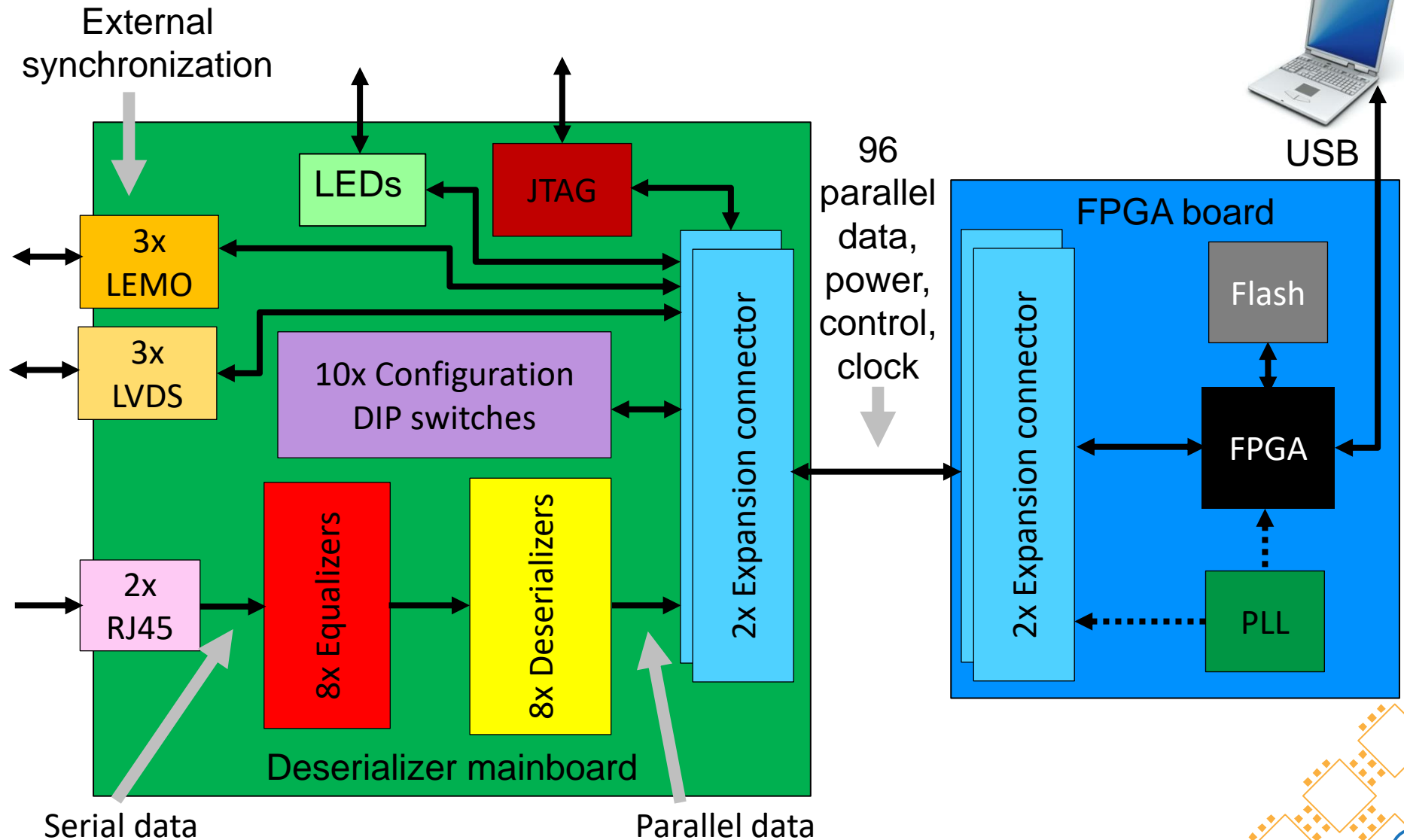
ROS – Read Out Server
TSC – Trigger Sector Collector



Delivered: Custom BERT Equipment

- ❖ System Under Test: communication channels of LHC/CMS
- ❖ Delivered: custom Bit Error Rate (BER) Test Equipment on FPGA
- ❖ Usage: test and certification of communication channels of LHC/CMS
- ❖ Hardware and FPGA design, software, final integration, and test by Testonica and TalTech (*subcontractor*)
- ❖ Successfully delivered in 2013 with positive feedback from CERN

The Receiver Module HW



USB

FPGA board

Flash

FPGA

PLL

2x Expansion connector

96 parallel data, power, control, clock

2x Expansion connector

8x Deserializers

8x Equalizers

10x Configuration DIP switches

3x LEMO

3x LVDS

2x RJ45

Deserializer mainboard

External synchronization

Serial data

Parallel data

LEDs

JTAG

The Control Software Application

Receiver
side GUI

The screenshot shows the Receiver side GUI with the following components and callouts:

- Connected devices**: A list of devices with a dropdown menu showing "12230003MJ" and "12230003MK".
- Device status**: A "RECEIVE" button.
- Whether specific link is locked**: A callout pointing to the "Locked/Not Locked" column in the table.
- Error rates per link**: A callout pointing to the "Error Counter" column in the table.
- Number of lock losses per link**: A callout pointing to the "Lock Loss" column in the table.
- Mask specific counter**: A callout pointing to the "Mask Lock Loss" column in the table.
- Device info**: A callout pointing to the "Device Information" section.
- BRAM / FLASH operations**: A callout pointing to the "Flash Data" section with buttons "BRAM > FLASH" and "FLASH > BRAM".
- Reset counters**: A callout pointing to the "Reset Counters" button.
- Test patterns upload / readout**: A callout pointing to the "LOAD TEST PATTERNS" and "READBACK TEST PATTERNS" buttons.
- Enable logging**: A callout pointing to the "Enable logging" checkbox.

Device Information:

- Device Serial Number: 12230003MK
- Device Name: Opal Kelly XEM6010
- Firmware Version: 2.34
- Software Version: 2.2
- Device ID: RECEIVER

Flash Data:

- BRAM > FLASH
- FLASH > BRAM

PATTERNS:

- LOAD TEST PATTERNS
- READBACK TEST PATTERNS
- Default Value: 001f
- SAVE DEFAULT VALUE

Table:

	Locked/Not Locked	Error Counter	Lock Loss	Mask Errors	Mask Lock Loss
LINK 1:	LOCKED	0	0	<input type="checkbox"/>	<input type="checkbox"/>
LINK 2:	LOCKED	0	0	<input type="checkbox"/>	<input type="checkbox"/>
LINK 3:	LOCKED	0	0	<input type="checkbox"/>	<input type="checkbox"/>
LINK 4:	LOCKED	0	0	<input type="checkbox"/>	<input type="checkbox"/>
LINK 5:	LOCKED	20459966	64928257	<input type="checkbox"/>	<input type="checkbox"/>
LINK 6:	LOCKED	0	63242802	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LINK 7:	LOCKED	20455918	63200379	<input type="checkbox"/>	<input type="checkbox"/>
LINK 8:	LOCKED	20460014	0	<input type="checkbox"/>	<input checked="" type="checkbox"/>

Batch count: 5000

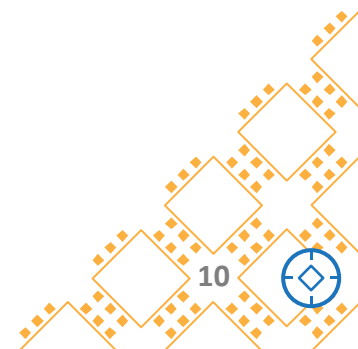
File name: C:\ise_projects\cern_dig\rev2\Release_2013.03.26\log.txt

Logging interval: 30 seconds

Enable logging ☐



DEVELOPMENT OF THE TAU LEPTON DECAY TRIGGERING ALGORITHM



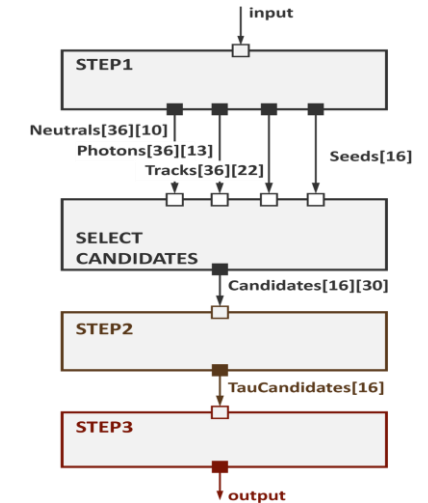
Project Facts

- ❖ Development of the tau lepton decay triggering algorithm
- ❖ Project initiated by
 - ⦿ Estonian National Institute of Chemical Physics and Biophysics (NICPB)
- ❖ Development in collaboration with NICPB and TalTech
- ❖ *On-going project: started in 2020 and to be continued until 2024*
- ❖ Key challenge: process 10 billion objects (particle data) per second on a single FPGA



Requirements

- Allowed latency
 - 1uS (max time before the processing results must be ready)
- Design clock frequency: 360MHz
- Platform
 - VirtexUltrascale+ FPGA (the most advanced on the market)
 - Tool-chain: Vivado and Vivado HLS (High-Level Synthesis)
 - Used languages: C++ (HLS version) and VHDL
- Challenge: fit and route the design inside the FPGA while maintaining the required level of throughput



	odd	even	odd	even	
odd	0	1	2	3	0
even	4	5	6	7	0
odd	8	9	10	11	1
even	12	13	14	15	1
odd	16	17	18	19	2
even	20	21	22	23	2
odd	24	25	26	27	3
even	28	29	30	31	3
odd	32	33	34	35	4
	0	0	1	1	

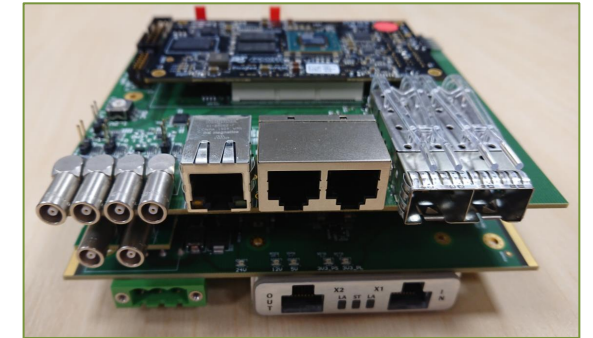


DEVELOPMENT OF AN FPGA-BASED I/O AND CONTROL SYSTEM FOR ESS/ERIC



ESS/ERIC Projects at TalTech

- ❖ Embedded control SW, driver extensions, FPGA design and test strategy development in 3 projects (2016-2021):
 - ⦿ Development FPGA-Based I/O and Control System
 - ⦿ Embedded software development and HW design
 - ⦿ Implementation of an EtherCAT slave card
- ❖ Project is run and coordinated by TalTech
- ❖ Testonica provides consultancy and engineering support



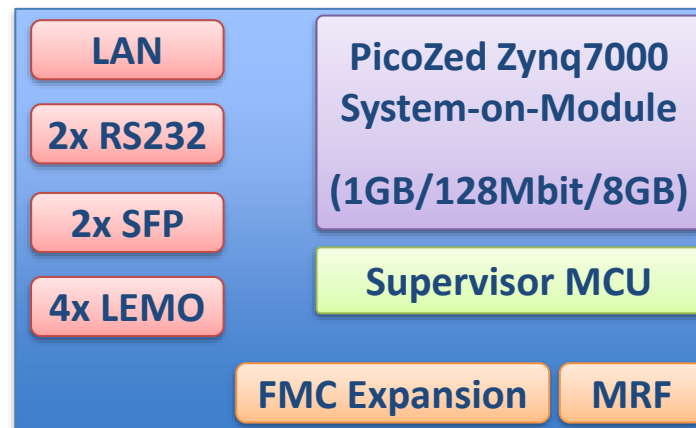
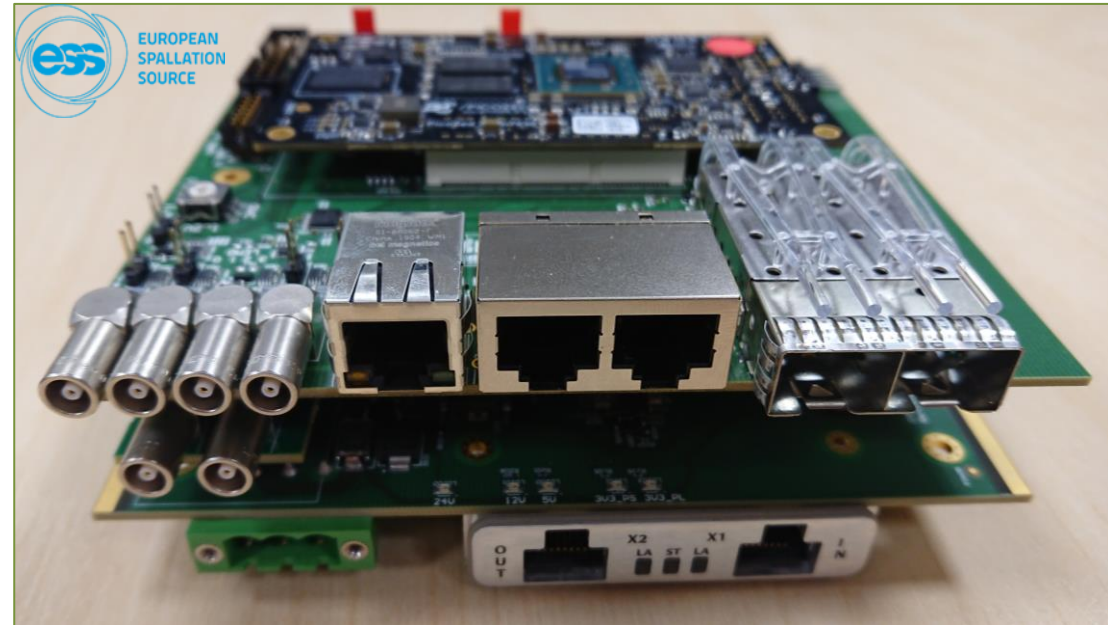
FPGA-Based I/O and Control System

Technical Specifications

- ⊗ Zynq7000 SoC-FPGA
- ⊗ System-on-Module (SoM) based
- ⊗ Ready-made Linux SW package
- ⊗ 1GB DDR3 memory
- ⊗ 128Mbit QSPI Flash (boot)
- ⊗ 8GB eMMC Flash (application)

Interfaces

- ⊗ +24V DC, passive cooling
- ⊗ Gigabit Ethernet
- ⊗ 2x SFP (up to 6.6Gbps)
- ⊗ 2x RS232 UART (RJ45)
- ⊗ 4x LEMO connectors
- ⊗ FMC slot (1.2V/1.5V/1.8V)
- ⊗ MRF expansion slot
- ⊗ JTAG interface



Summary

- ❖ Custom BERT Equipment – 2011
- ❖ Tau lepton decay triggering algorithm – 2020
- ❖ ESS/ERIC: FPGA-Based I/O and Control System



Thank You!

We **love** solving problems

