1st CERN Baltic Conference (CBC 2021)
June 28, 2021

Testonica

TAL TECH

Test System HW/SW for LHC Data Links
and Other Projects Done for CERN and ESS

Artur Jutman

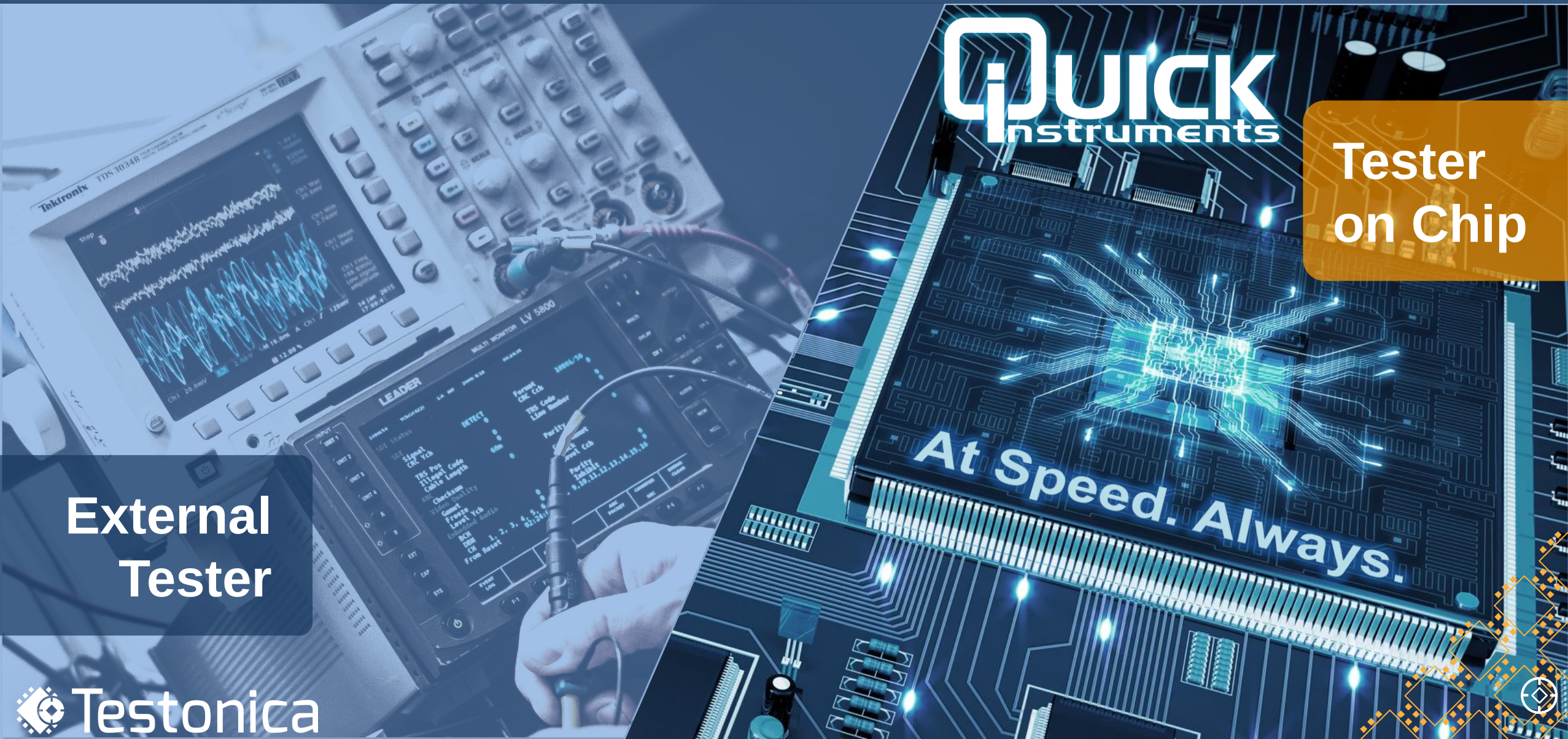
Inventor of Embedded Virtual Instruments

Solutions in 20+ countries

Patented in 2013

Testonica

Testing Right From the Inside



We Invest In R&D and Support The Community

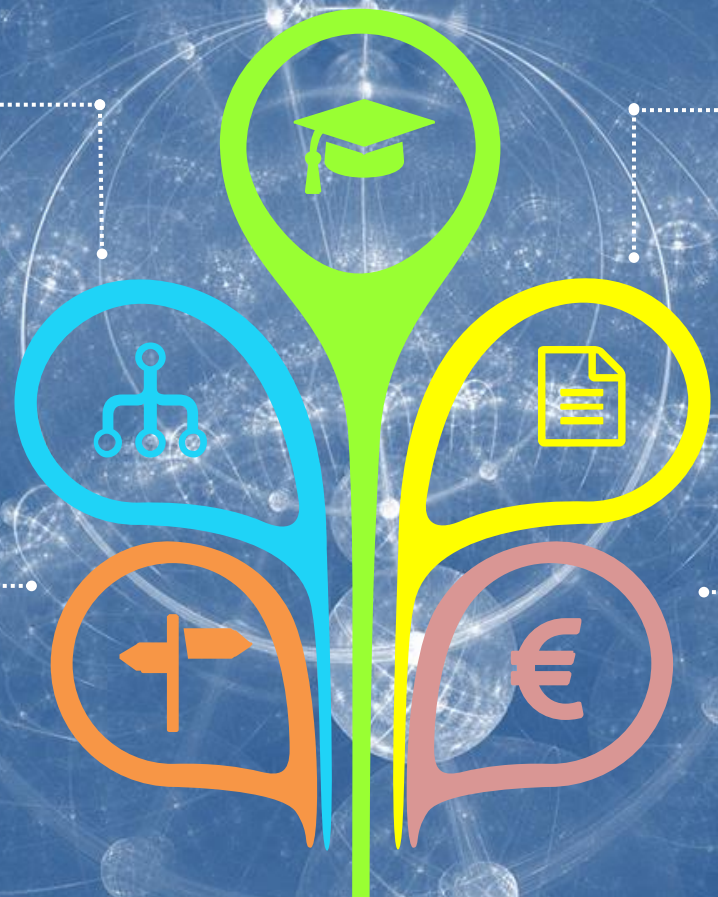
Jobs for PhD Students

Academic Collaboration

Scientific Publishing

Coordinating EU R&D projects

Conference Sponsorship



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Presentation Outline

- Custom BERT Equipment – 2011
- Tau lepton decay triggering algorithm – 2020
- ESS/ERIC: FPGA-Based I/O and Control System

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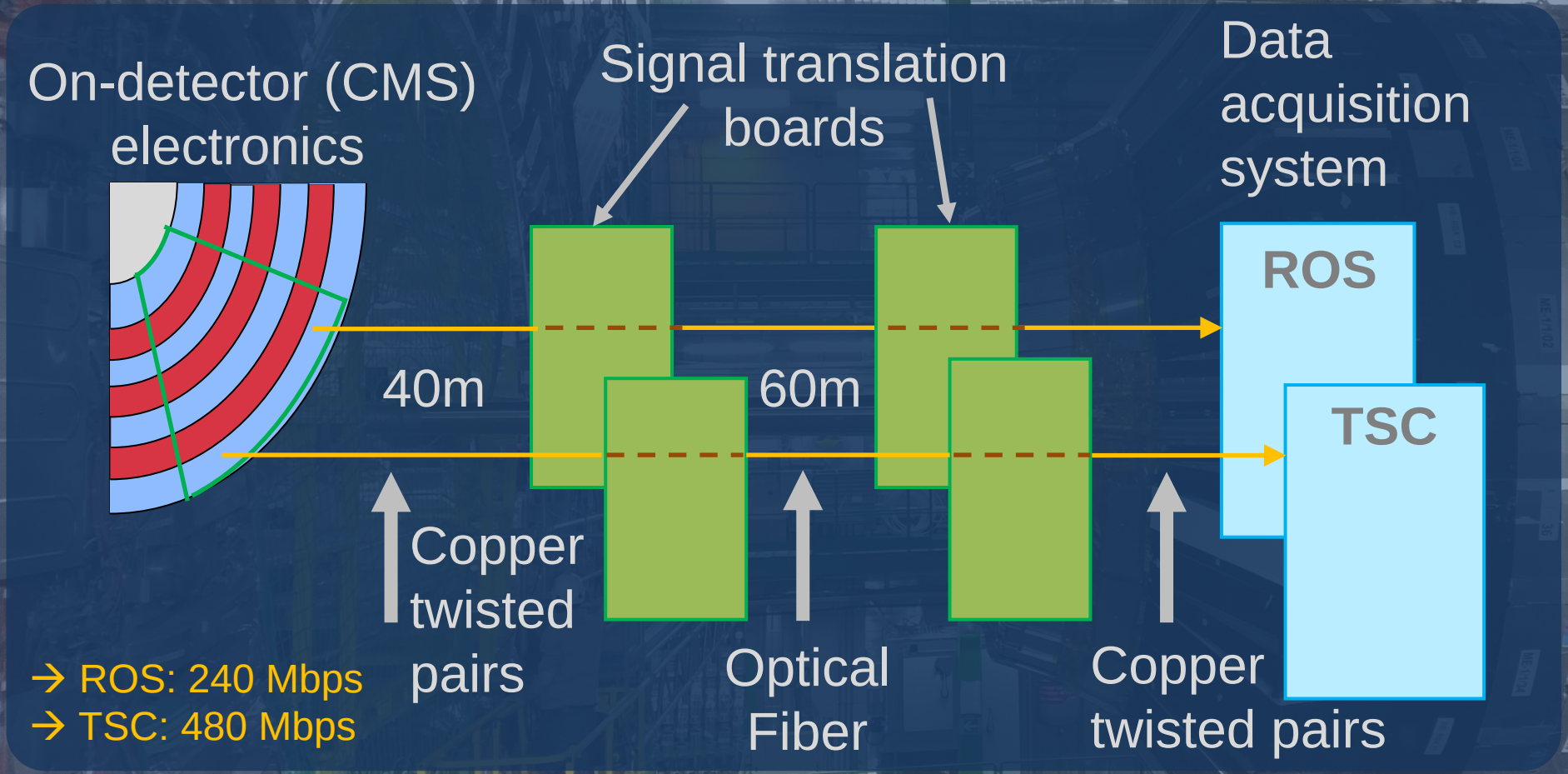
In collaboration with TAL TECH

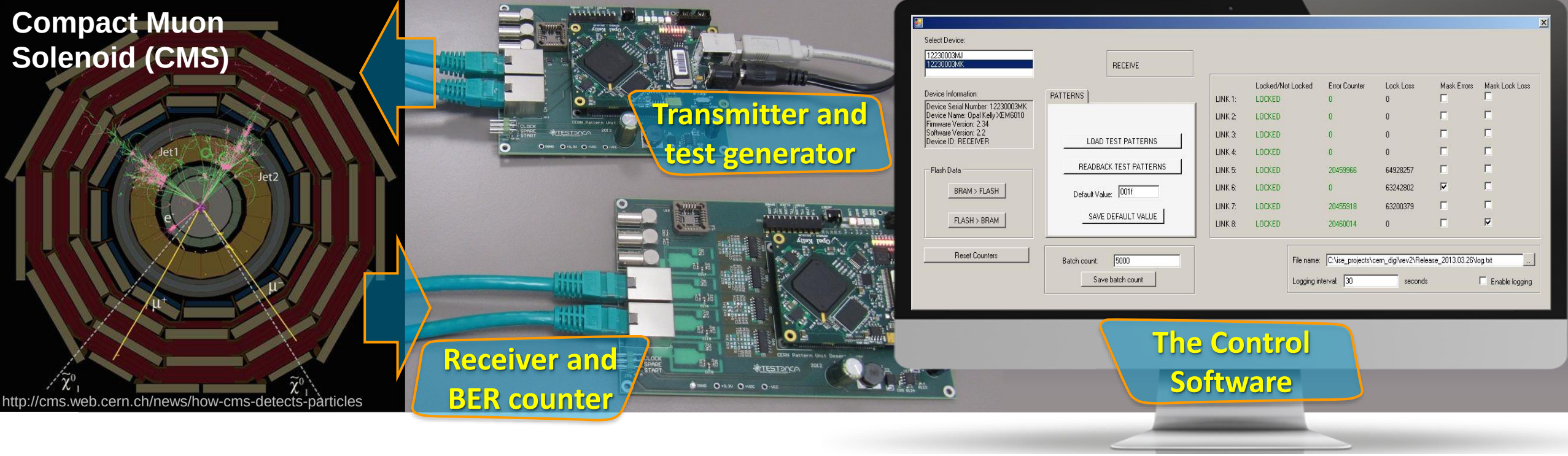
CMS Data Links



Problem:
- signal integrity
- full custom design

Needs:
- end-to-end test
- push-button start
- autonomous exec
- HW and SW dev

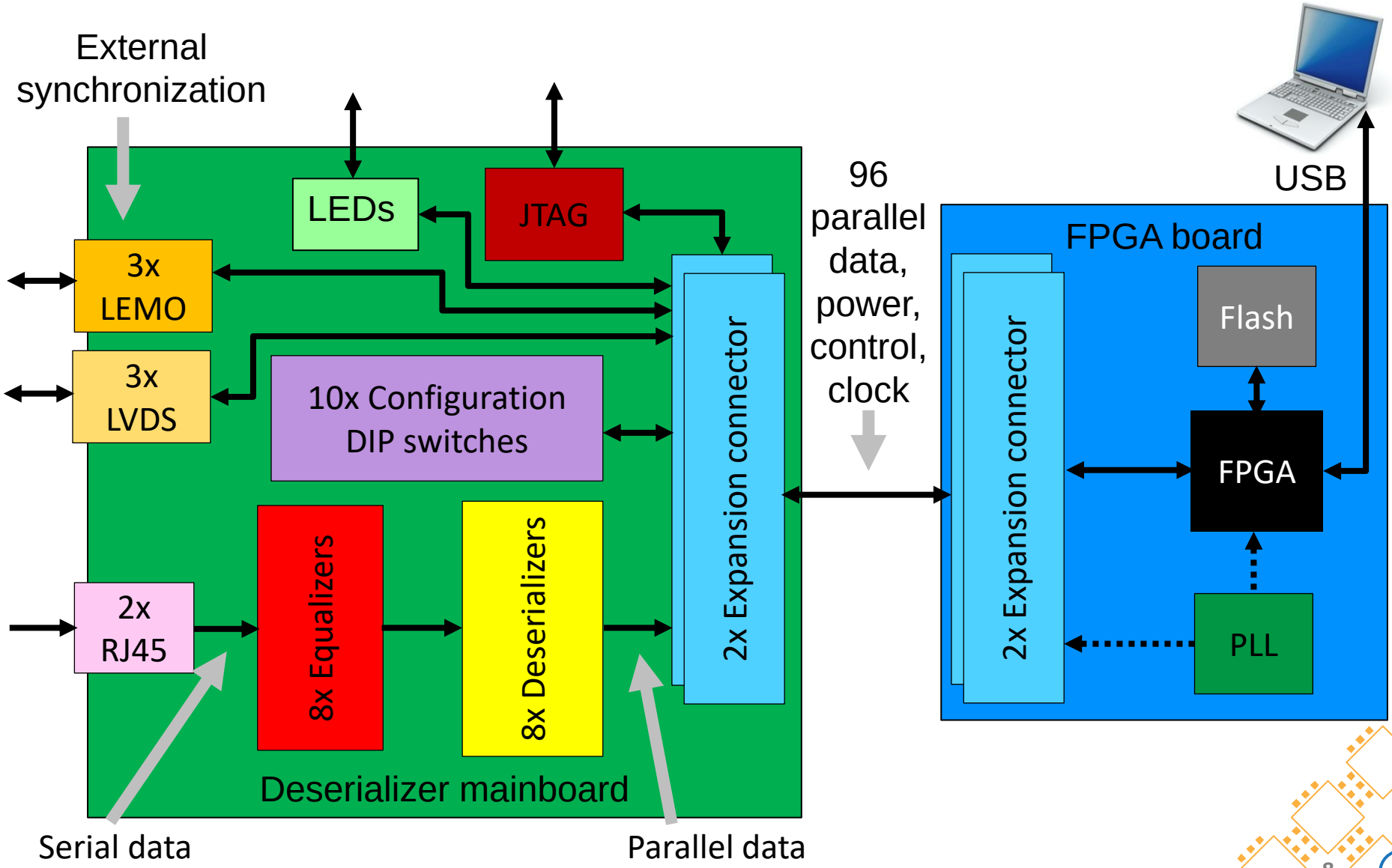
ROS – Read Out Server
TSC – Trigger Sector Collector



Delivered: Custom BERT Equipment

- System Under Test: communication channels of LHC/CMS
- Delivered: custom Bit Error Rate (BER) Test Equipment on FPGA
- Usage: test and certification of communication channels of LHC/CMS
- Hardware and FPGA design, software, final integration, and test by Testonica and TalTech *(subcontractor)*
- Successfully delivered in 2013 with positive feedback from CERN

The Receiver Module HW



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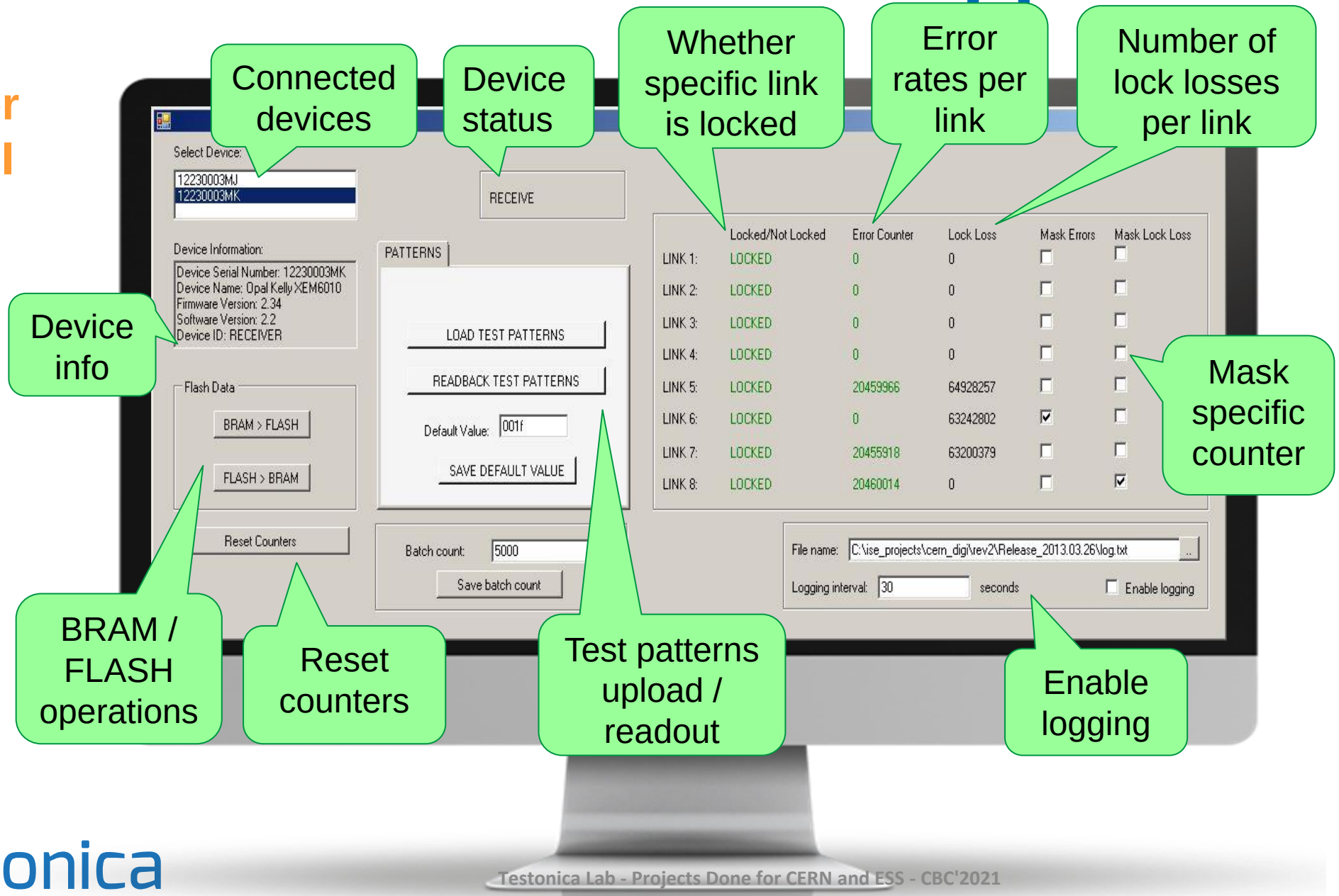
The Control Software Application

Receiver side GUI



DEVELOPMENT OF THE TAU LEPTON DECAY TRIGGERING ALGORITHM

Project Facts

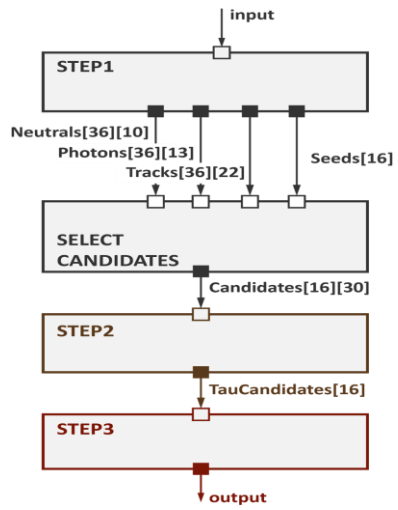
- Development of the tau lepton decay triggering algorithm
- Project initiated by
  - Estonian National Institute of Chemical Physics and Biophysics (NICPB)
- Development in collaboration with NICPB and TalTech
- *On-going project: started in 2020 and to be continued until 2024*

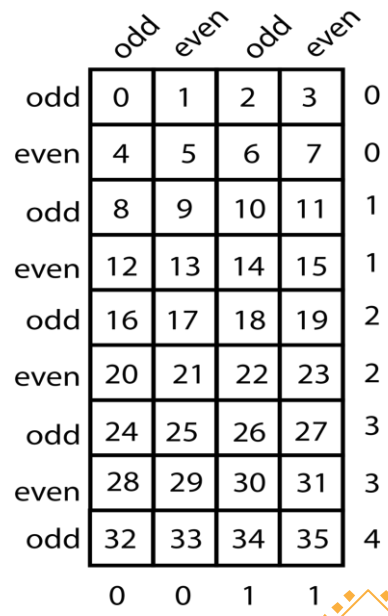
- Key challenge: process 10 billion objects (particle data) per second on a single FPGA

Requirements

- Allowed latency
  - 1uS (max time before the processing results must be ready)
- Design clock frequency: 360MHz
- Platform
  - VirtexUltrascale+ FPGA (the most advanced on the market)
  - Tool-chain: Vivado and Vivado HLS (High-Level Synthesis)
  - Used languages: C++ (HLS version) and VHDL

- Challenge: fit and route the design inside the FPGA while maintaining the required level of throughput





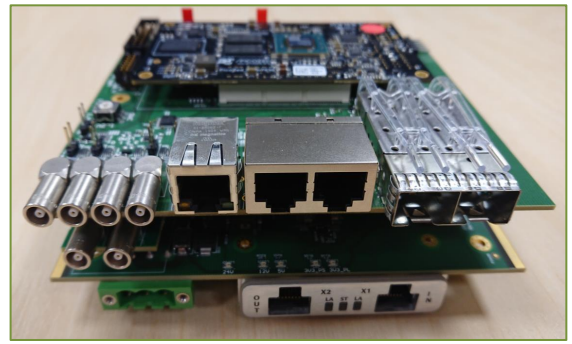
EUROPEAN SPALLATION SOURCE

DEVELOPMENT OF AN FPGA-BASED I/O AND CONTROL SYSTEM FOR ESS/ERIC

Testonica

ESS/ERIC Projects at TalTech

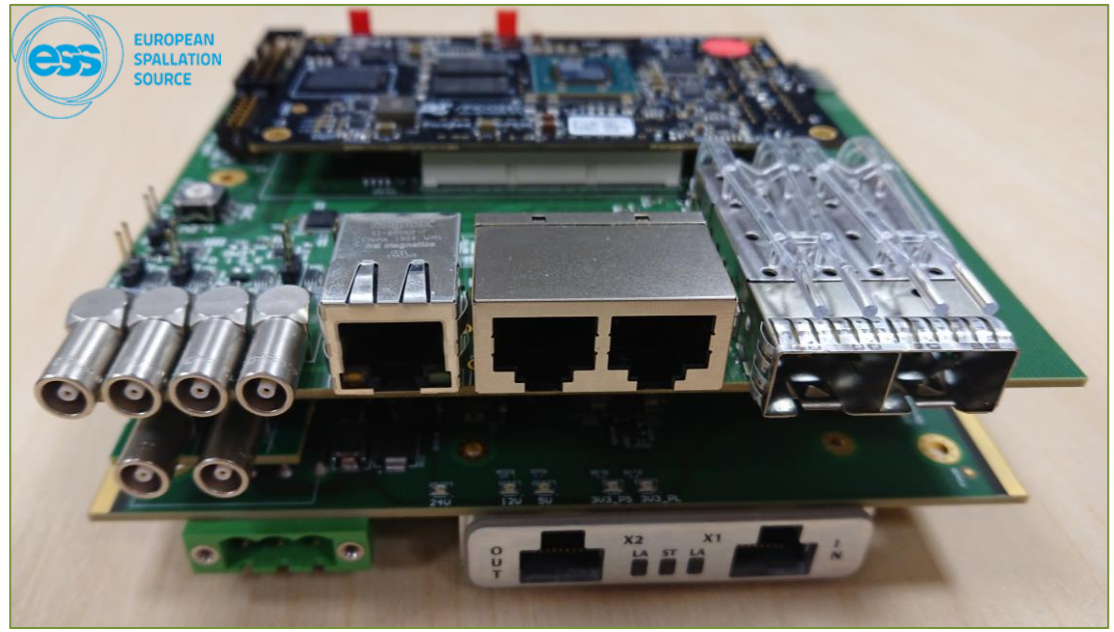
- Embedded control SW, driver extensions, FPGA design and test strategy development in 3 projects (2016-2021):
  - Development FPGA-Based I/O and Control System
  - Embedded software development and HW design
  - Implementation of an EtherCAT slave card

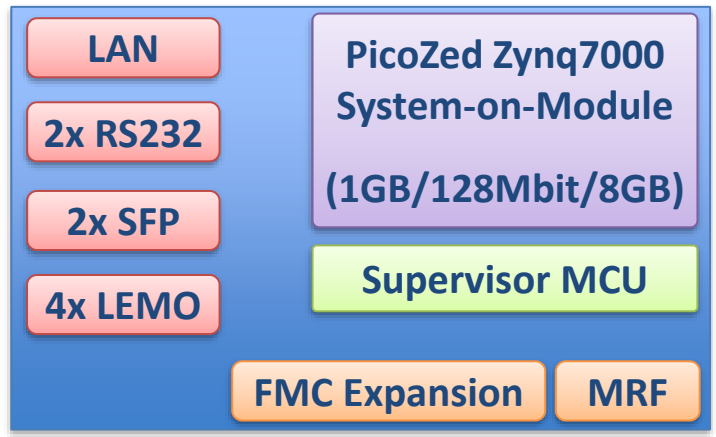


- Project is run and coordinated by TalTech
- Testonica provides consultancy and engineering support

FPGA-Based I/O and Control System

- Technical Specifications
  - Zynq7000 SoC-FPGA
  - System-on-Module (SoM) based
  - Ready-made Linux SW package
  - 1GB DDR3 memory
  - 128Mbit QSPI Flash (boot)
  - 8GB eMMC Flash (application)
- Interfaces
  - +24V DC, passive cooling
  - Gigabit Ethernet
  - 2x SFP (up to 6.6Gbps)
  - 2x RS232 UART (RJ45)
  - 4x LEMO connectors
  - FMC slot (1.2V/1.5V/1.8V)
  - MRF expansion slot
  - JTAG interface





Summary

- Custom BERT Equipment – 2011
- Tau lepton decay triggering algorithm – 2020
- ESS/ERIC: FPGA-Based I/O and Control System

Thank You!

We **love** solving problems

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