CMS HL-LHC Tracker Upgrade

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on behalf of the CMS Collaboration

Vilnius University

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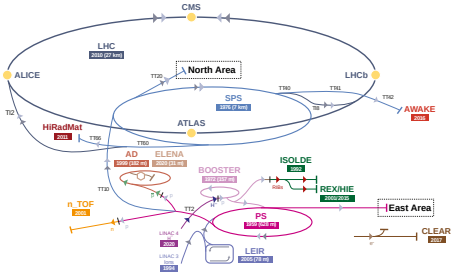
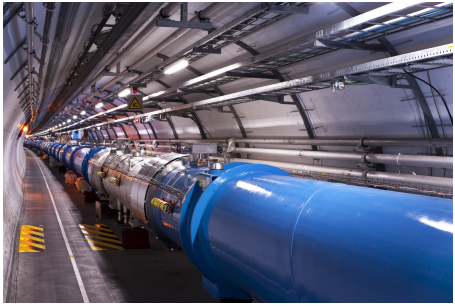
Introduction

Experimental Infrastructure at CERN





Currently: 6.5 TeV @ pile up[1]: $\sim$35, peak lumi[2]: $2.1 \cdot 10^{34}\ \frac{\text{Hz}}{\text{cm}^2}$ (design: $10^{34}\ \frac{\text{Hz}}{\text{cm}^2}$)

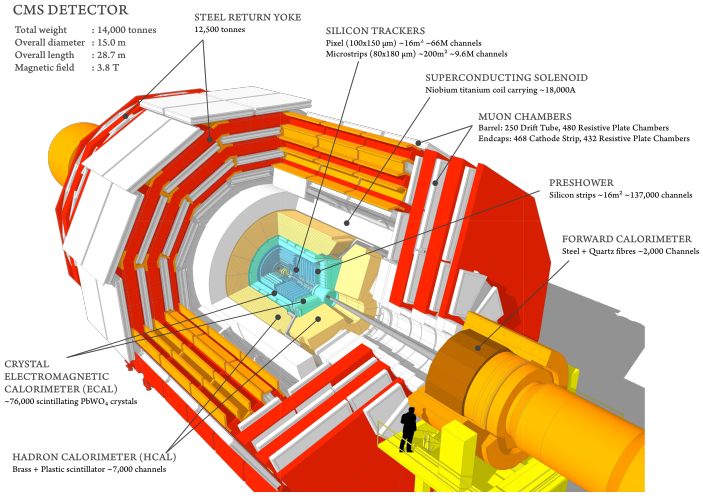
HL-LHC: 7 TeV @ pile up: 140–200, peak lumi: $5\text{–}7.5 \cdot 10^{34}\ \frac{\text{Hz}}{\text{cm}^2} \Rightarrow$ data rate $10\times$

[1] Number of instataneous collisions

[2] $<$7.7 T @ 1.9 K, $\sim$2800 bunches $\times\ 10^{11}$ protons

Detector: Compact Muon Solenoid

CMS detector with cut (phase 0)



40 MHz

×

~30 p–p collisions

×

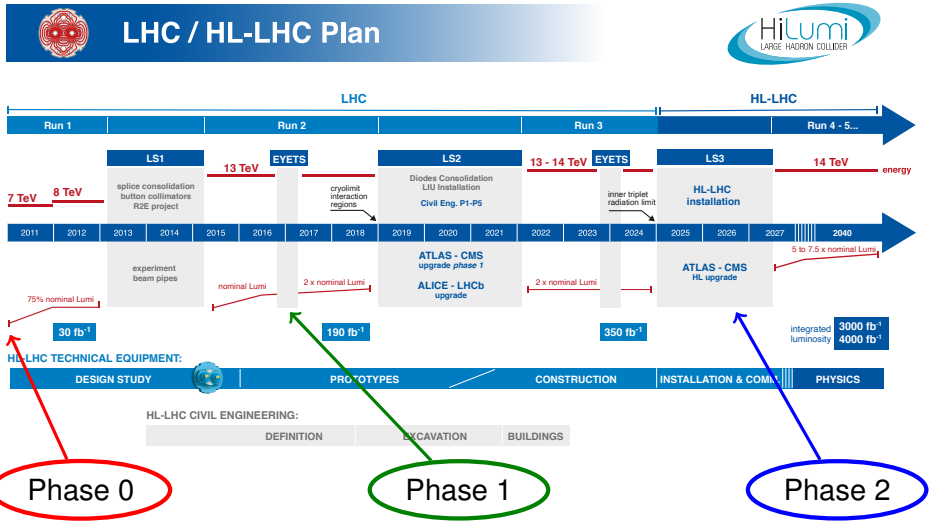
p–p = ~200 **final** partic.

=

~100 Tb/s

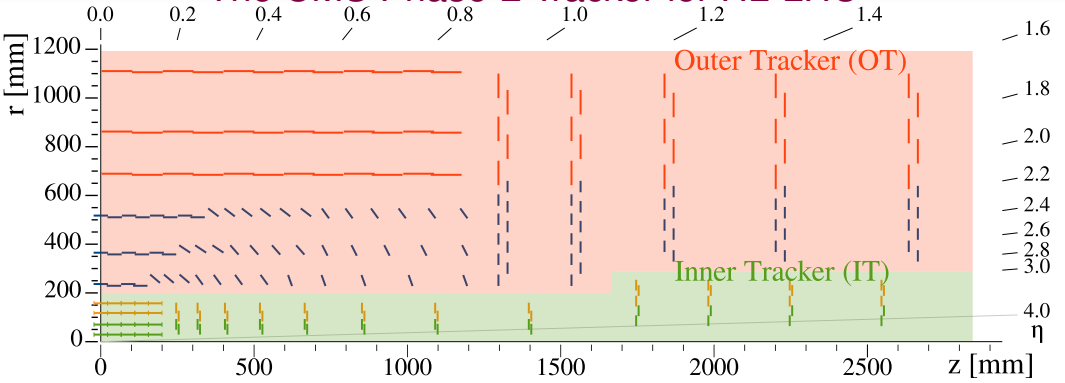
Final particle	Resolution
γ	1.5–5% @ 60 GeV
e	2–4% @ 10 GeV
μ	1–1.5% @ 10 GeV
j	o(10)%

CMS Tracker and HL-LHC



Outlook of Phase-2 Tracker Upgrade

The CMS Phase-2 Tracker for HL-LHC

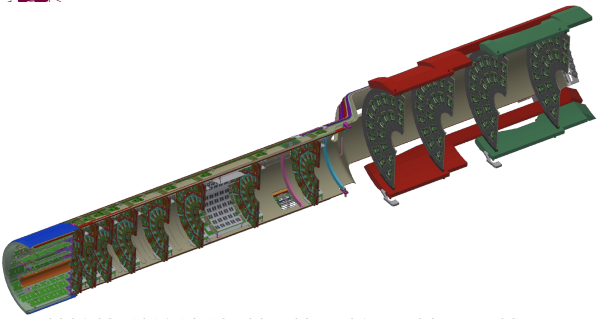


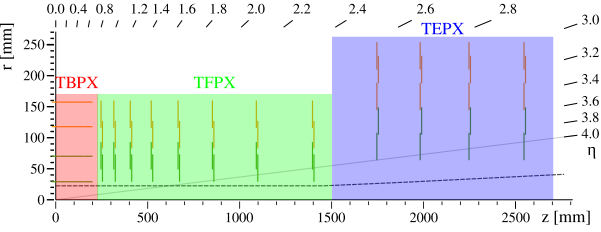
About 220 m^2 of active Si area:

- Outer Tracker: strip–strip and pixel-strip modules
- Inner Tracker: 1x2 pixel-chip and 2x2 pixel-chip modules

Inner Tracker (IT)

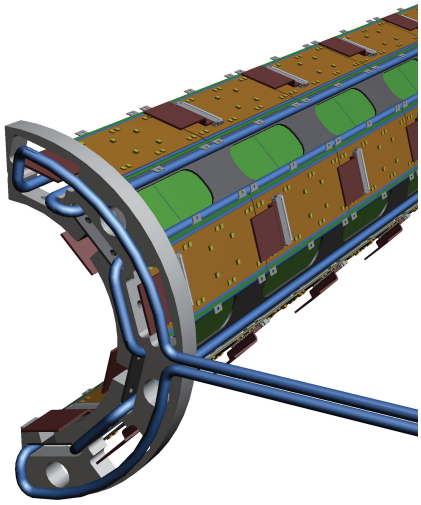
Inner Tracker Overview



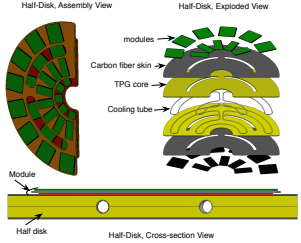


- 3892 modules in total
  - 1156 of 1x2 pixel-chip modules
  - 2736 of 2x2 pixel-chip modules
- 2 billion pixels
- Sensors: 4.9 m^2 $\times$ 150 μm
- Occupancy <0.1%
- TEPX Disk 4 Ring 1 is dedicated to lumi measurements
  - Independent readout and control

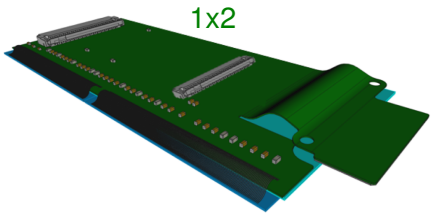
IT Mechanics and Cooling

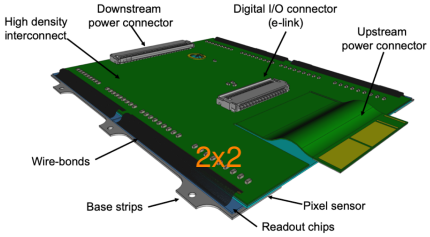


- Shared light carbon-fiber structures and cooling pipes
- TBPX: follows phase-1 ladder design.
- TFPX&TEPX: rings of D-shaped planar structures (no turbine)
- Low-mass dual-phase CO_2 cooling (nominal $-35°C$, operated @$< -20°C$)
  - $\sim$50 kW cooling capacity



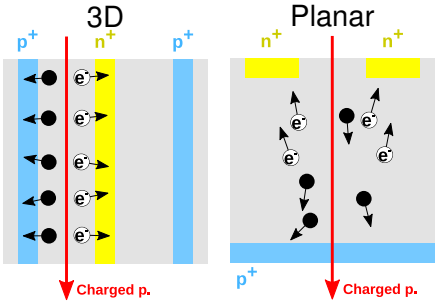
IT Modules





- Two module types: 1x2 and 2x2 chips per sensor
  - 1x2: two inner rings and layers
- Readout chips (ROCs) are
  - bump-bonded to sensor;
  - wire-bonded to High Density Interconnect (HDI);
  - the only active components on modules.
- Sensor is glued to HDI.
- HDI: flexible PCB to distribute IO and power.

IT Sensors



Thin planar n-in-p sensors:

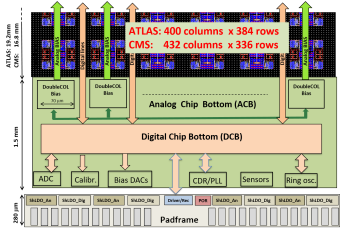
- 150-μm thick
- Bias up to 1 kV
- Need spark protection between ROC and sensor
- Baseline choice

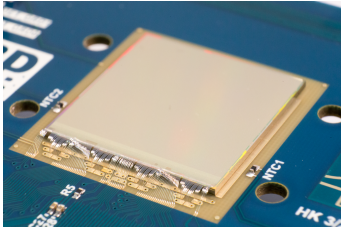
3D sensors:

- Potentially more radiation hard
- More complex fabrication, larger capacitance
- An option for innermost layers

IT Readout Chip (ROC)

RD53B Floorplan





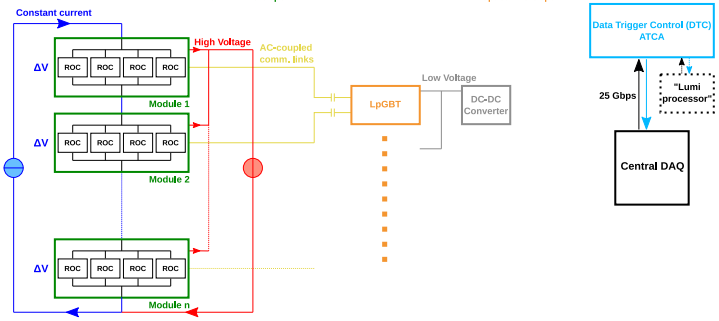
RD53B on single-chip test card

- Developed by RD53 Collaboration
  - Initially for ATLAS & CMS
- 65 nm CMOS
- Radiation hard $\geq$500 Mrad
- First prototype R53A tested and funtional @1 Grad

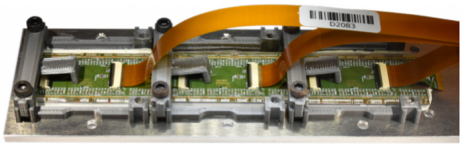
Some RD53 features:

- Cell: 50 μm $\times$ 50 μm
- Shunt LDO for serial powering
- Low threshold $o(10^3)$ e$^-$
- 160 Mbps control, $\leq$4x1.28 Gbps output links

IT Powering and Readout



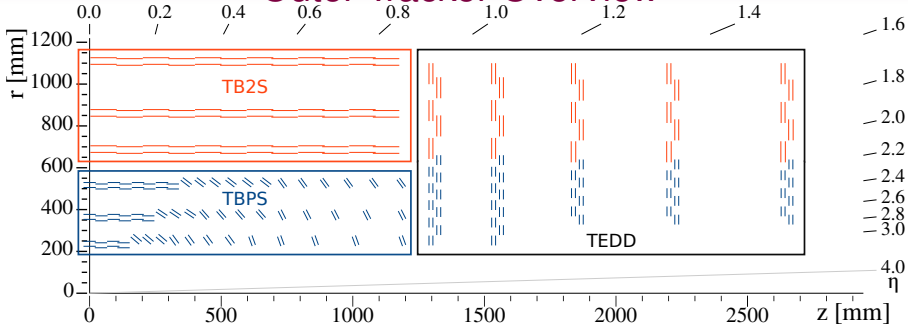
Serial powered chain of 2x2 digital modules



- Serial powering with bypass
  - Up to 12 modules per chain
- High power demand:
  - Serial: ∼55 kW
  - HV: ∼2.5 kW
  - Optoelectronics: ∼2.3 kW
  - Preheaters: ∼3.7 kW
  - Total: ∼63.5 kW
- Portcard: 2x LpGBT, 2x VTRx+
- $\leq$6 e-links per LpGBT
- ∼750 portcards

Outer Tracker (OT)

Outer Tracker Overview

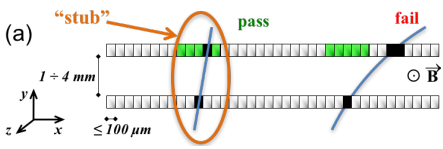


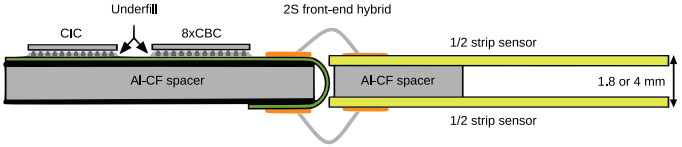
- ∼13 200 modules in total
  - TB2S: Tracker Barrel Strip–Strip
  - TBPS: Tracker Barrel Pixel–Strip
  - TEDD: Tracker Endcap Double Disk (2S&PS)
- 43 M strips (190 m^2) and 170 M macropixels (25 m^2)
- Tilted geometry for performance (⇒tracking)

- Occupancy <1%
- Tracking at Level-1 trigger

OT Tracking at Level-1 Trigger

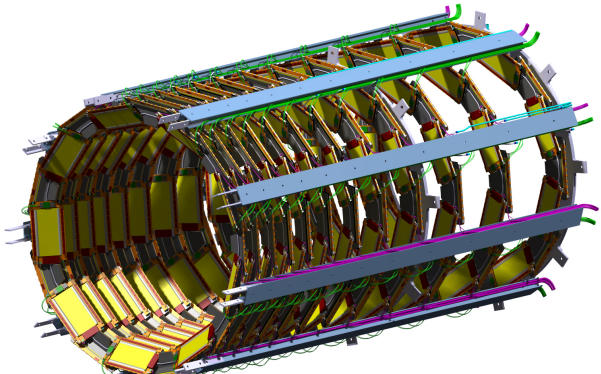
- Needs quick hardware-level decisions
- Necessary for high nr. of instantaneous interactions
- Modules reject low p_{T}, thus module has:
  - Sensor sandwich
  - Integrated logic in ASIC for “stubs”
  - Different sensor spacing due to geometry (while providing $p_{\mathrm{T}} > 2$ GeV)
- Tilted geometry helps (next slide)

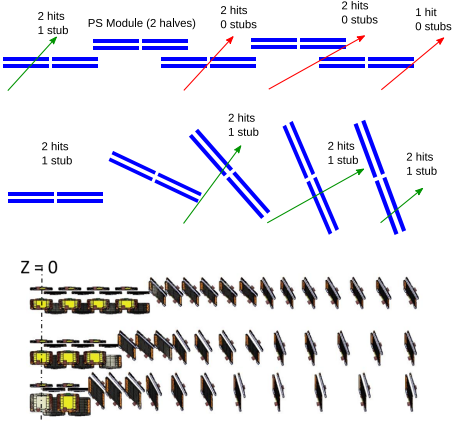




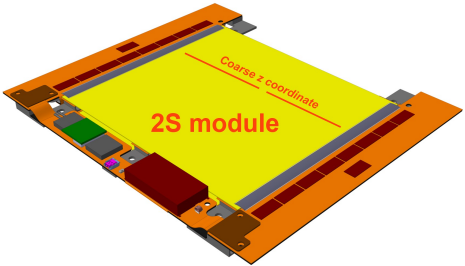
OT Geometry & Mechanics

- Stubs only for same-half crossing
- Tilted geometry helps with efficiency&cost
- Two-phase CO_2 cooling as in IT





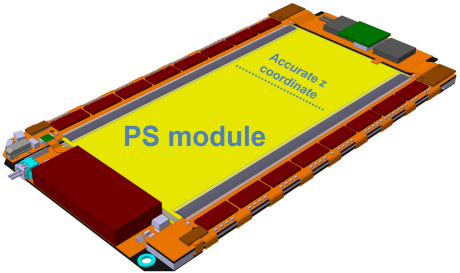
OT Module Topologies



- 2 Strip sensors
  2x 1016 strips (each 5 cm x 90 μm)
- 90 cm^2 active area
- Sensor spacer: 1.8 and 4.0 mm

2x Front-end hybrids

1x Service hybrid (optoelectronics & power)

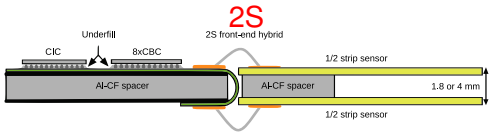


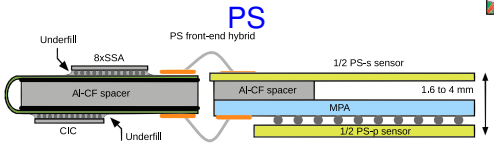
- MacroPixels: 32 x 960 strips (1.5 mm x 100 μm)
- Strip sensor: 2x 960 strips (2.5 cm x 100 μm)
- 45 cm^2 active area
- Sensor spacer: 1.6, 2.6, and 4.0 mm

2x Front-end hybrids

ea.1x Power and Readout hybrids

OT On-Module Electronics





CMS Binary Chip (CBC) ASIC:

- 130 nm CMOS
- Serves both sensors
- Performs stub finding
- 254 ch. (127 from top+bottom sensor)

Macro-Pixel ASIC (MPA), Short-Strip ASIC (SSA):

- 65 nm CMOS
- Stub finding by MPA
- Cluster and L1 from SSA $\rightarrow$ MPA to match in space and time

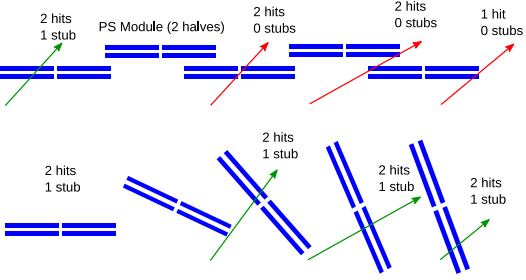
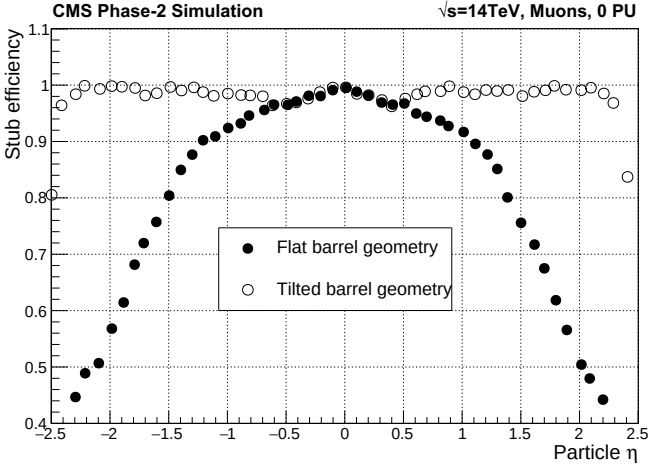
In 2S and PS, Concentrator Integrated Circuit (CIC):

- 65 nm CMOS
- Receives L1 and readout data
- “Hub” to service hybrids

Summary

Summary

- Ambitious project among CMS Phase 2 upgrades
- Critical optimizations due to more instantaneous collisions and integr. lumi
- New: Level-1 tracking and continuous lumi measurements

Backup

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