Update on FPGA Testing

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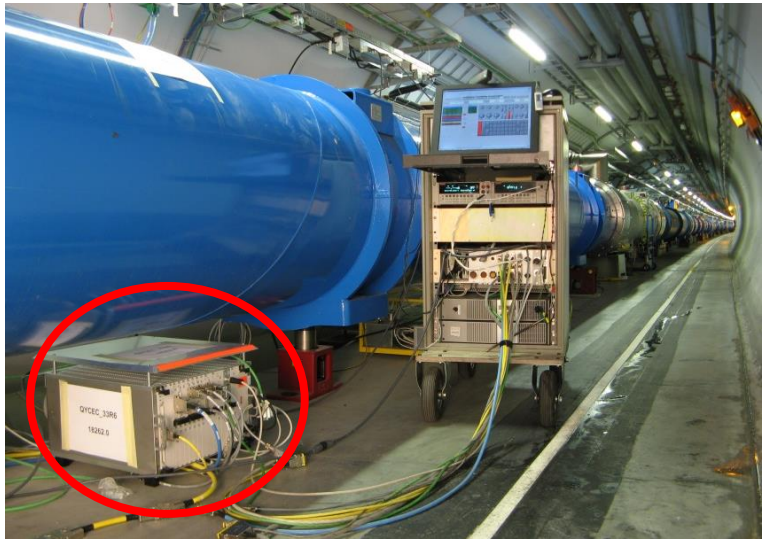
Motivations

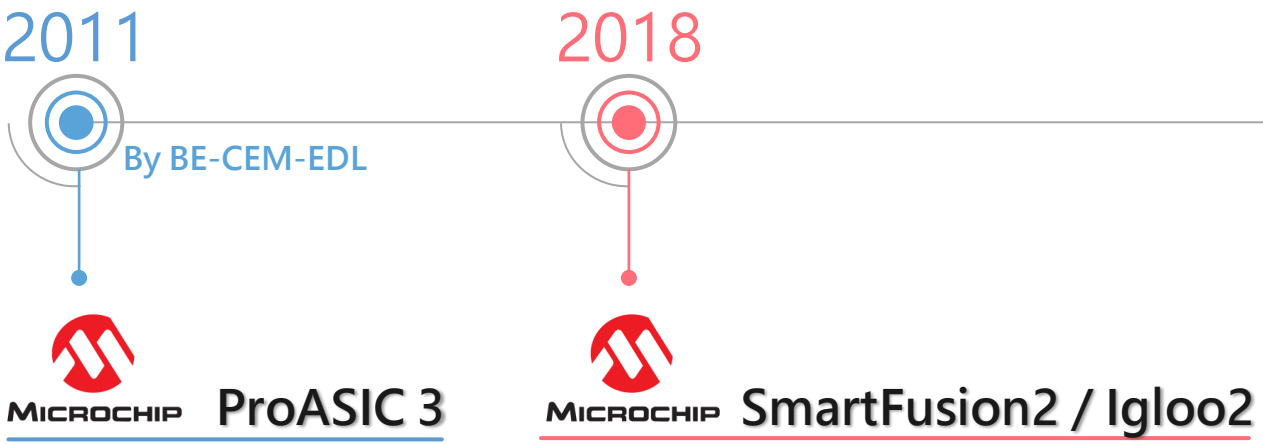
- A large number of electronic systems are exposed to the LHC radiation environments where they can be exposed to high level of doses and fluences
- The digital part of those systems is usually controlled by either microcontrollers, processors and FPGAs
  - FPGAs are usually preferred as they allow:
    - High Speed of operation
    - High Capacity for logic designs
    - Numerous I/Os compatible with different protocols (SERDES, LVDS, etc..)
    - Re-programmability
  - FPGAs are ones of the most complex component to be tested under radiation
  - FPGA qualifications for CERN application might require several years of work



@ Courtesy of the TE/MPE Group

Past Achievements

BE-CEM-ERP Qualification Timeline:



FPGAs Under study

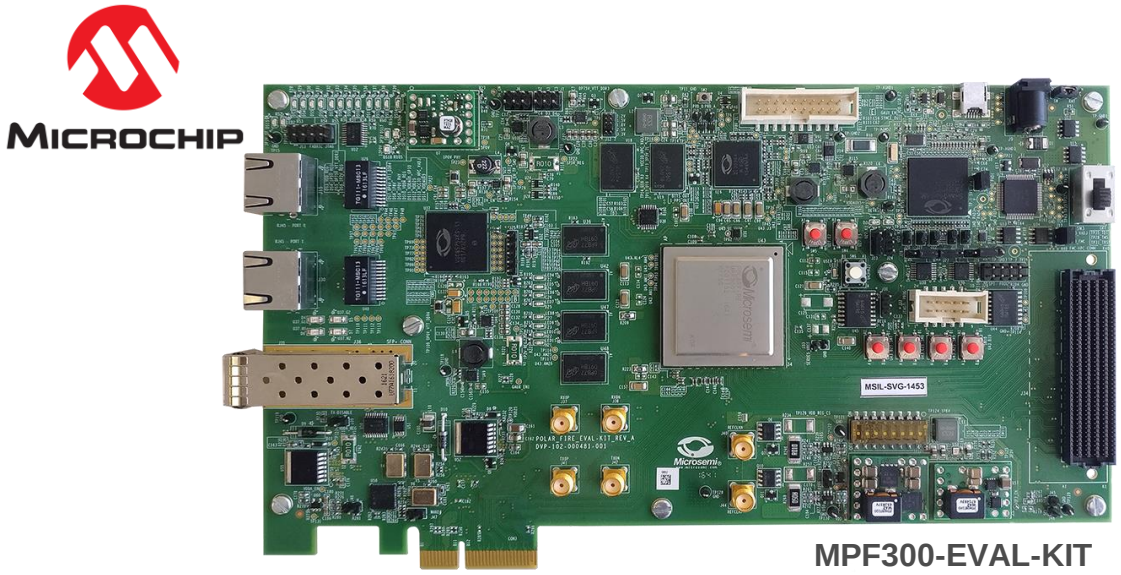
NG-MEDIUM (NX1H25S) from NanoXplore:

- **SRAM-Based FPGA:**
- STM C65 (65nm **RadHard** ST process)
- **Configuration Memory Integrity Check (CMIC) engine**
  - **Configuration Memory sensitive to SEU**
  - **Usually Higher TID lifetime than Flash-based**

NG-MEDIUM-EVAL-KIT

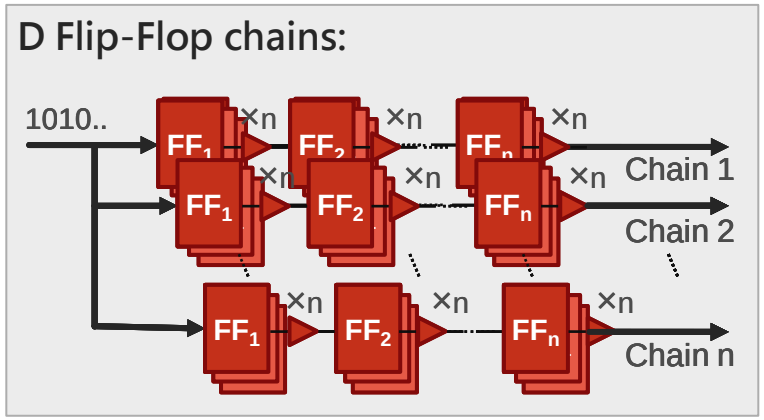
PolarFire (MPF300TS) from Microsemi:

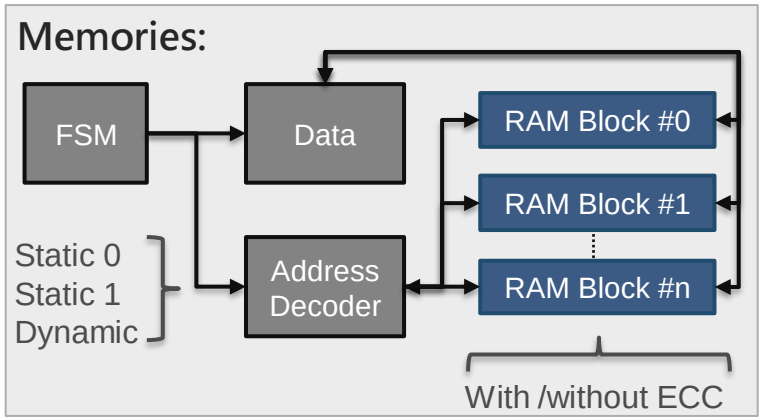
- **28nm SONOS technology**
- **Flash-Based FPGA:**
  - **Low Configuration Memory sensitivity to SEU**
  - **Usually lower TID lifetime than SRAM-based**

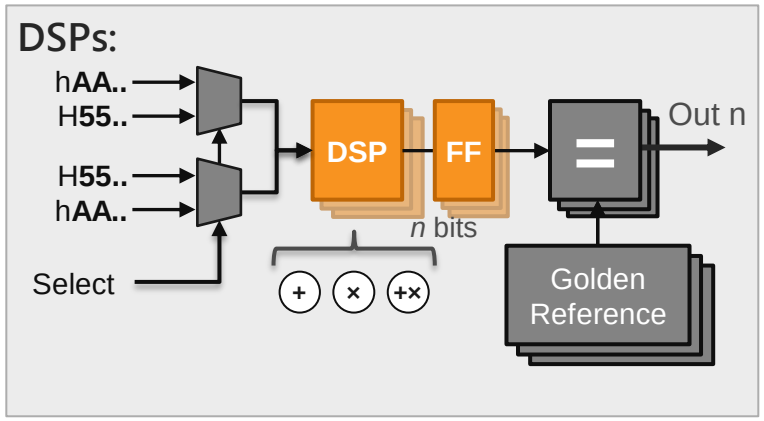


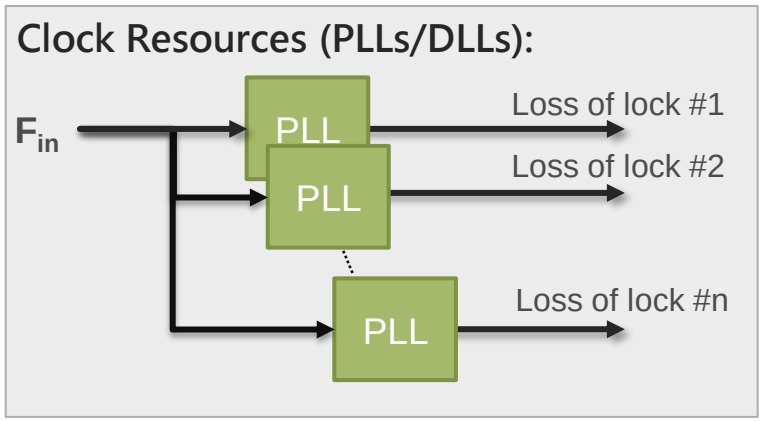
MPF300-EVAL-KIT

Standard Test Structures



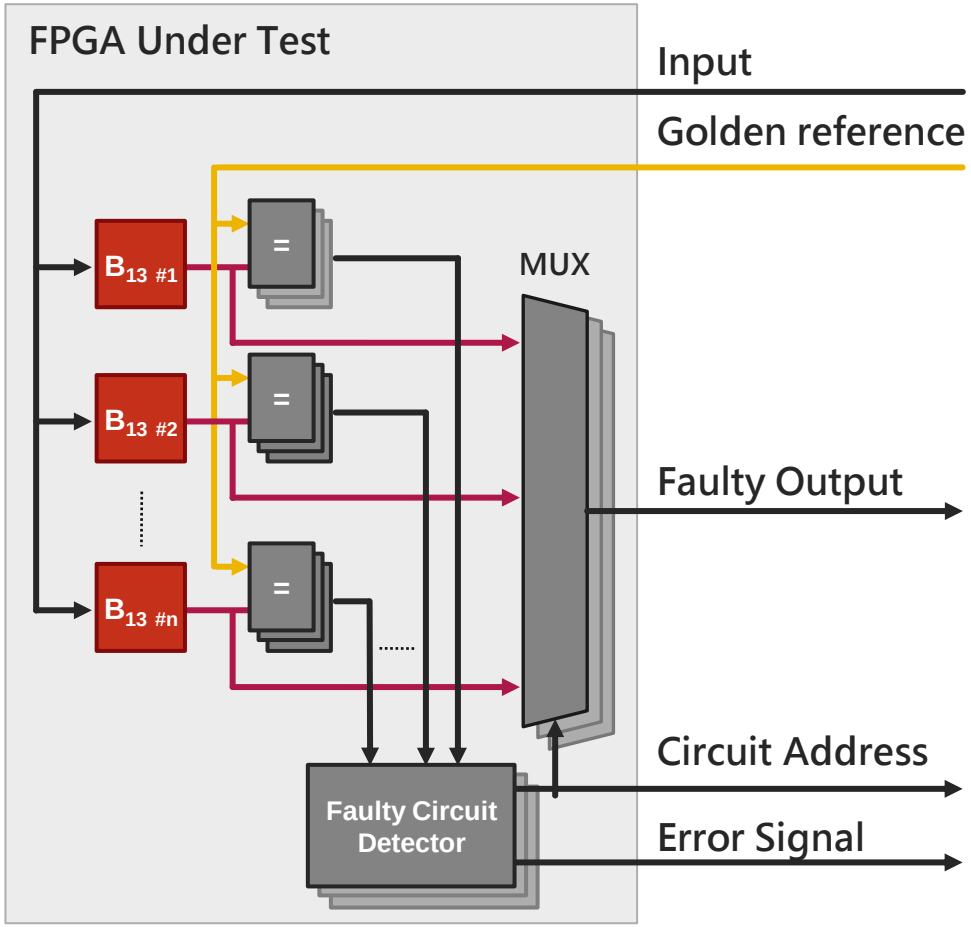






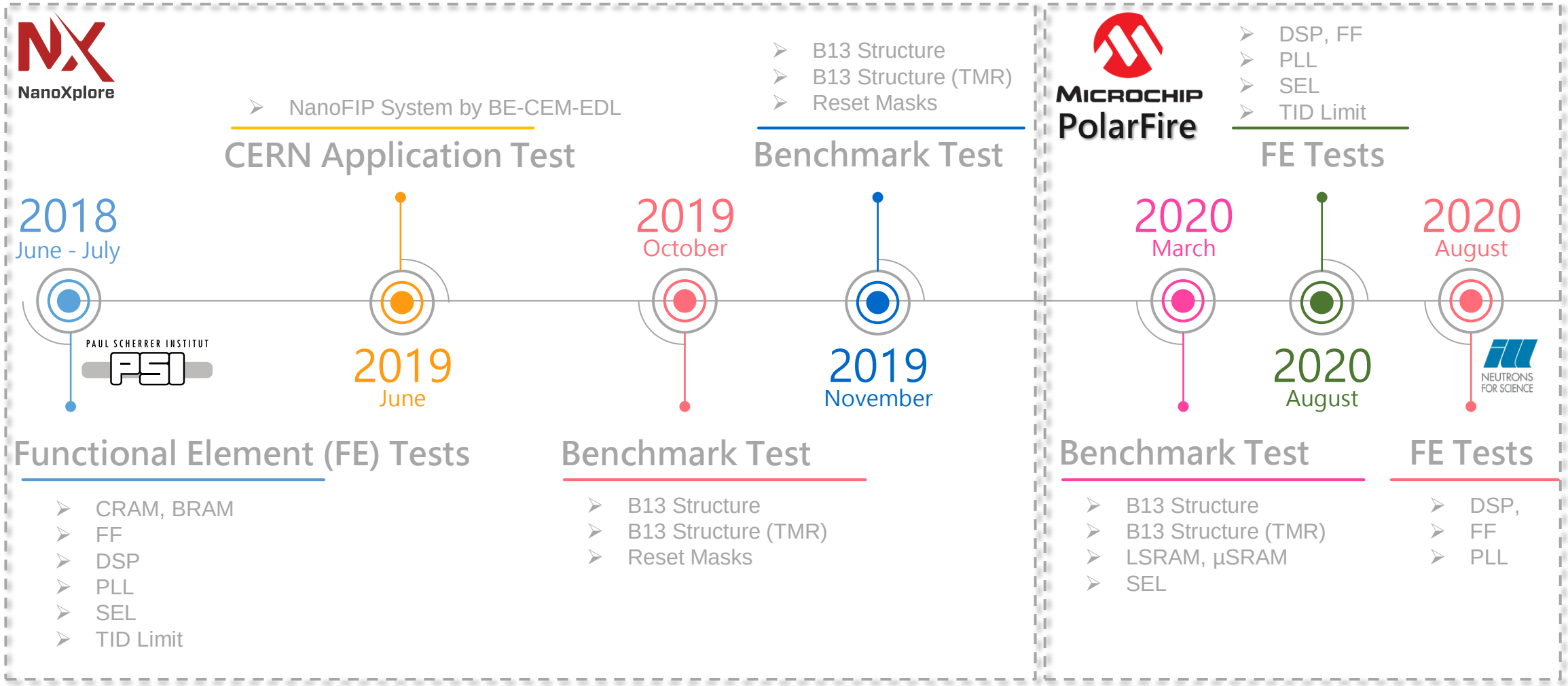
Benchmark Test Structure

- **Benchmark circuit employed is from the ITC'99 suite [1&2]** in collaboration with Politecnico di Torino
- It provides fully synthesizable circuits that can be used as reference circuits to evaluate and compare FPGA sensitivities
- **We used the B13 circuit**, which is the most used one in the suite
- **The B13 is a pure FSM circuit** that is composed of: 339 gates, 53 FF and its input/output interface has 10 bits
- **The output of each circuit is compared with a golden circuit** running on the Zynq board of the comparators are sent to the Zynq through FMC.
- **Circuit input signals are fed by a linear feedback shift register** (LFSR) generating random signals
- In case of error the Zynq reset all the structures

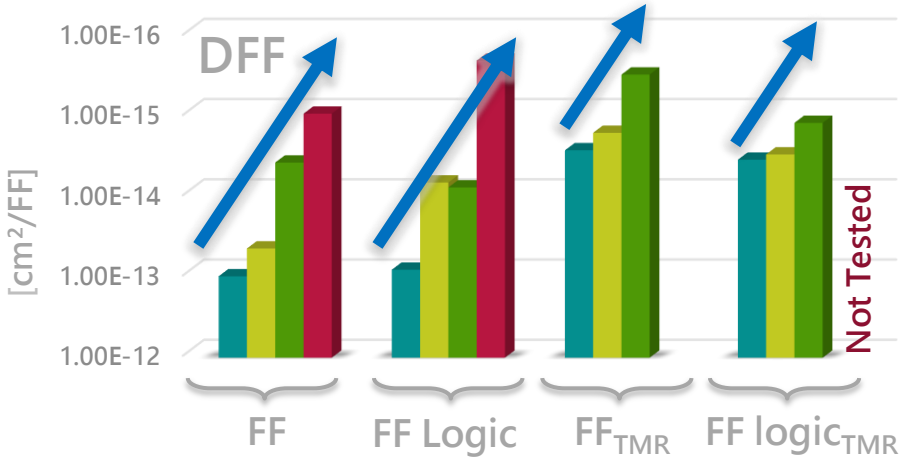


B13 Test design

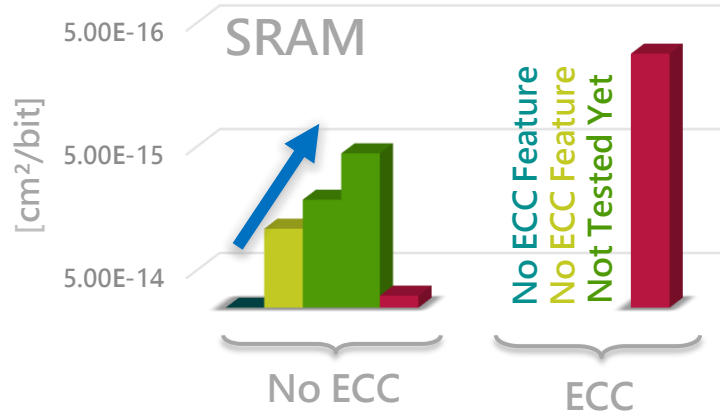
Qualification Timeline

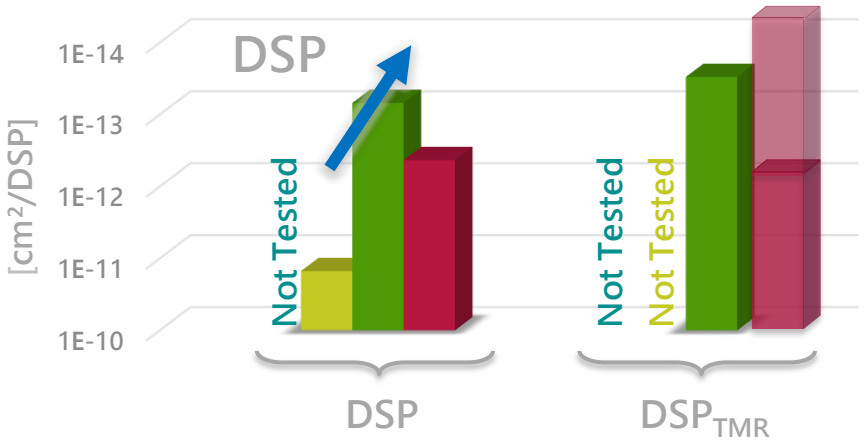


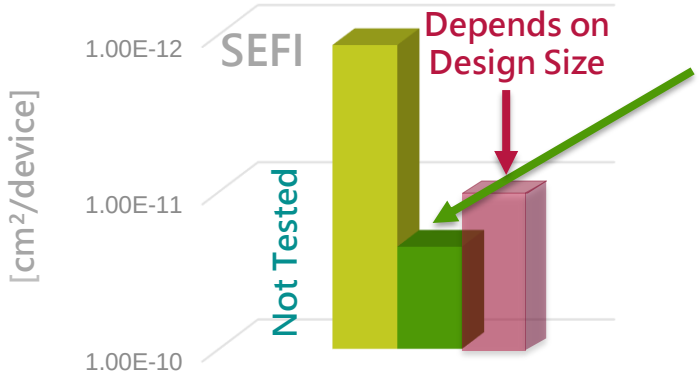
FPGA FE sensitivities comparison



Radiation Tolerance increased with new FPGAs







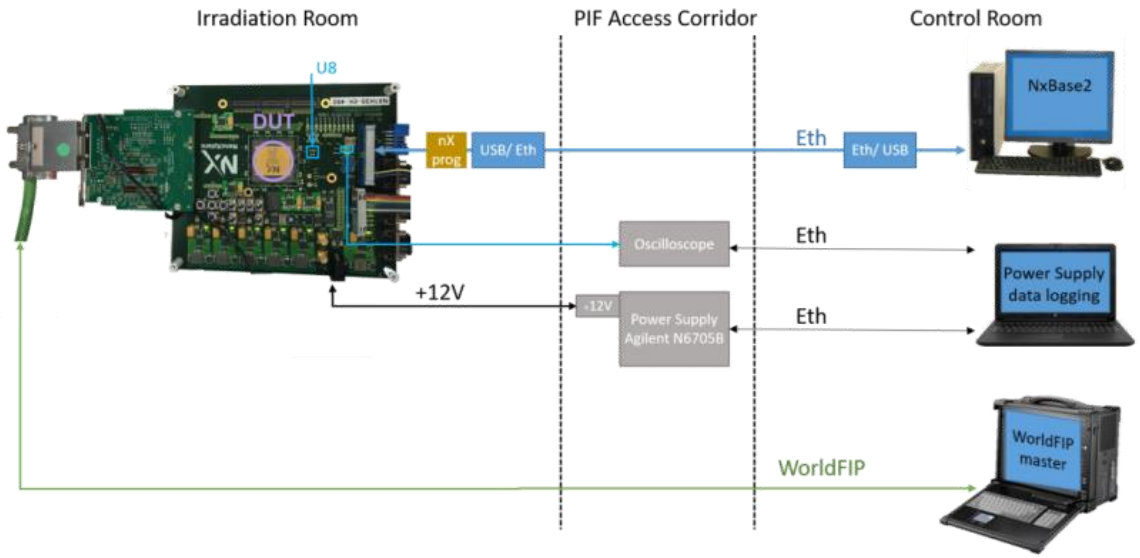
ProASIC SmartFusion PolarFire NG-Medium

Programmability:

- No loose up to 200 Gy (not tested above)
- No loose up to 3 kGy

NGMedium: NanoFIP Application Test

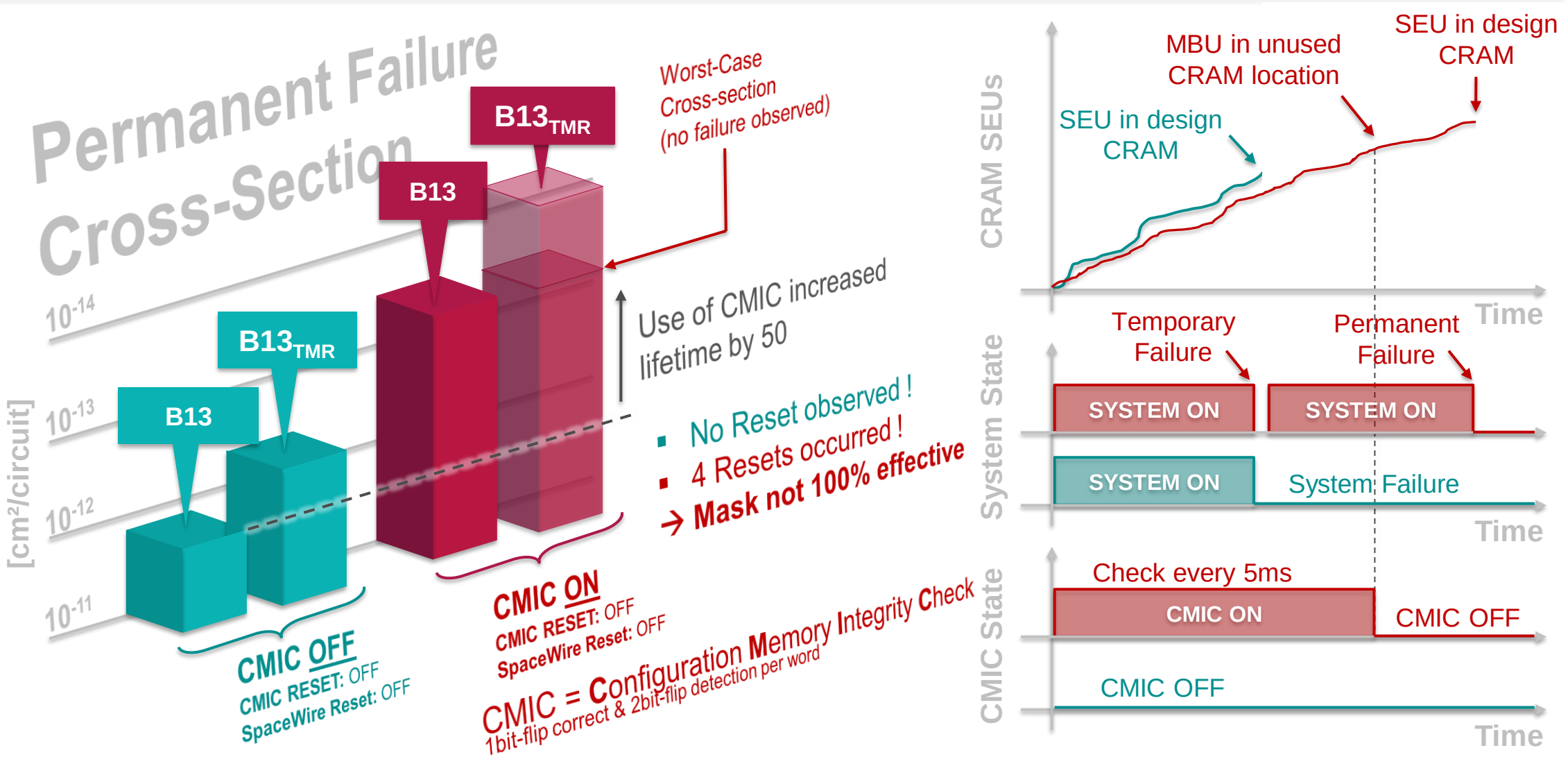
- Test of the **NanoFIP** design implementing the **WorldFIP** communication bus widely used at CERN for slow instrumentation control. This test was performed by the BE-CEM-EDL section.



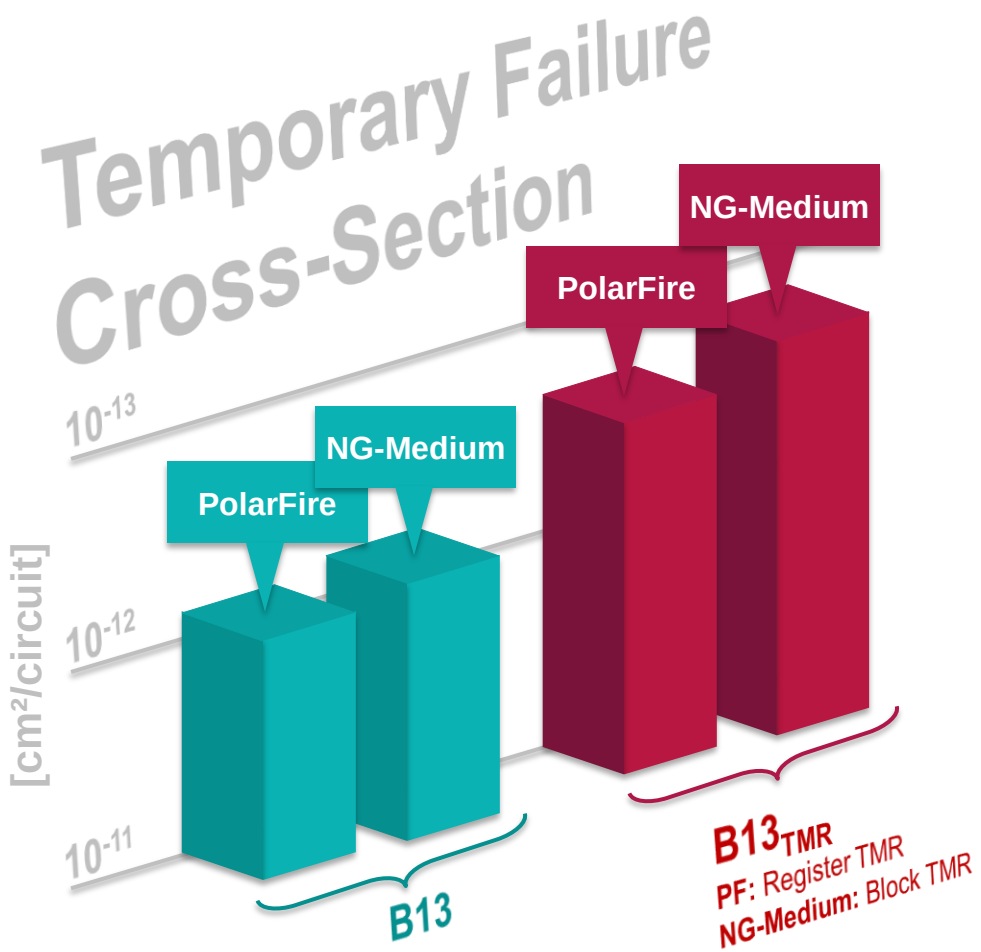
→ Unexpected early permanent failures observed during the test with a cross-section ranging from **$1.4 \cdot 10^{-11}$ down to $2.2 \cdot 10^{-12}$ cm²/device**

→ After discussion with NanoXplore it has been pointed out that some automatic reset schemes could have impacted the failure rate: by default a single error detected on the SpaceWire bus or a double error detected by the CMIC will lead the FPGA to reset itself, loosing the configuration

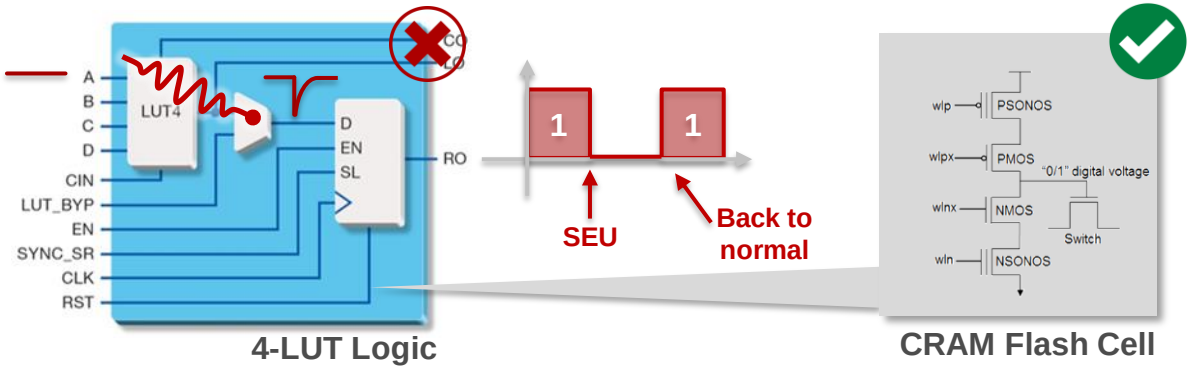
NGMedium: Reset Masks Results



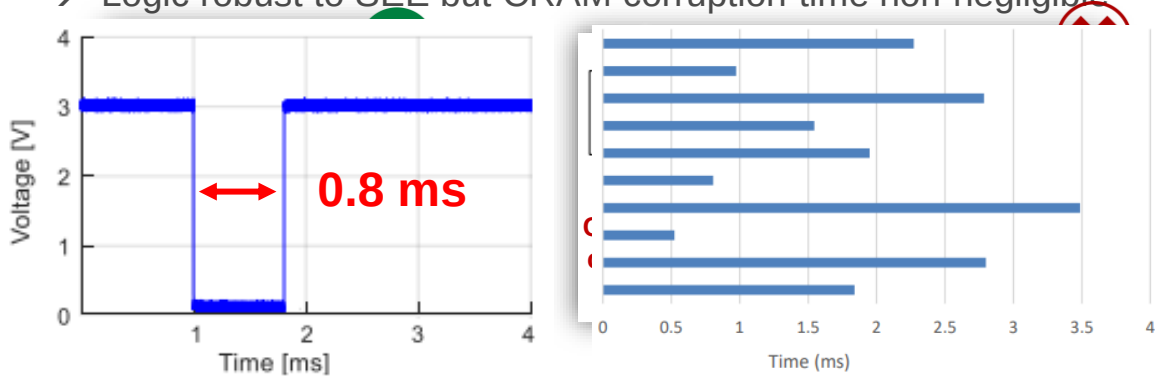
NGMedium Vs PolarFire: Testbench response



- Same failure rate but different causes:
  - **PolarFire:**
    - → SET captured in logic while CRAM immune



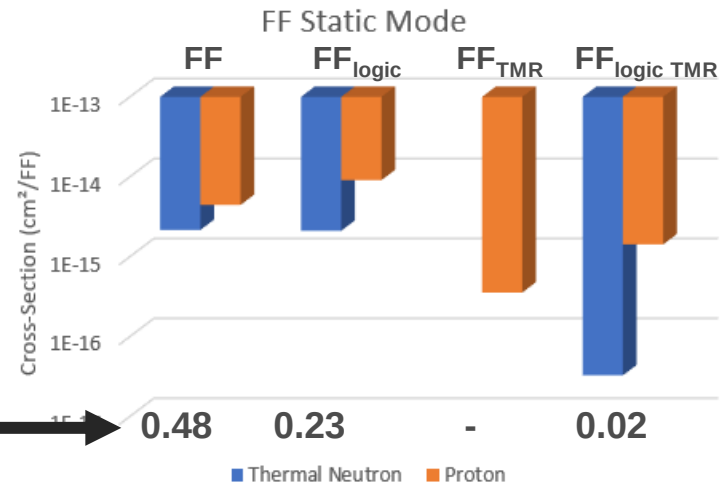
  - **NG-Medium:**
    - → Logic robust to SEE but CRAM corruption time non-negligible

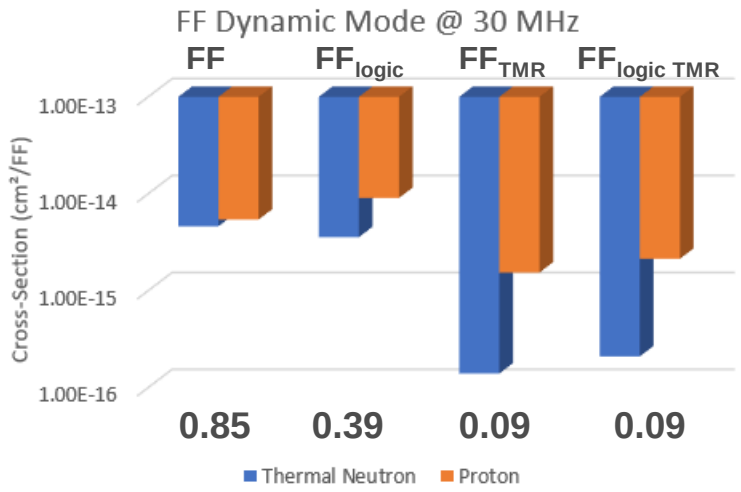


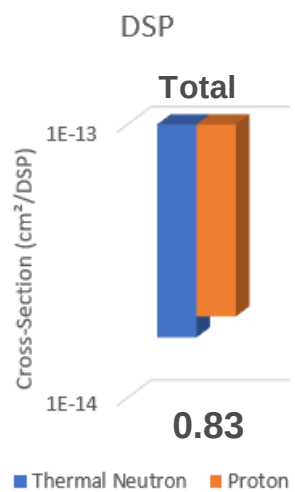
PolarFire: Proton vs Thermal neutrons

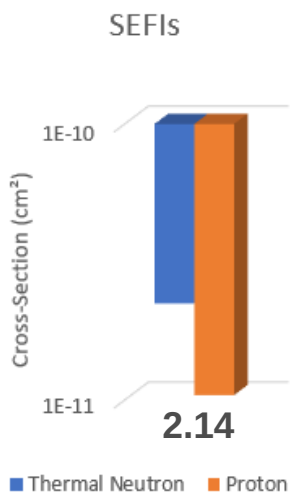
➢Preliminary results:

$\frac{\sigma_{HEH}}{\sigma_{Th}}$









➢Without logic the thermal neutron cross-sections are quite close to the proton ones for FF and DSPs

➢The SET capture probability seems lower with thermal neutrons

➢High SEFIs cross-section with thermal neutrons

➢Thermal neutrons should be considered for the SEE prediction in operation even for low R-Factors

➢More test planned in May 2020 (SRAM (w/wt ECC), B13 (w/wt TMR), DSP chains)

References & Resources

- ITC99' Benchmark Suite
  1. **Official Homepage:** https://www.cerc.utexas.edu/itc99-benchmarks/bench.html
  2. **Gitlab:** https://github.com/squillero/itc99-poli
- NG-Medium Radiation Test reports:
  3. **Functional Element Radiation report** [EDMS: 2227145], G. Tsiligiannis, link: https://edms.cern.ch/ui/file/2227145/1/NanoXploreRadReport_docx_cpdf.pdf
  4. **NanoFIP Radiation report** [EDMS: 2221380], E. Gousiou, link: https://edms.cern.ch/ui/file/2221380/1/PSI_Radiation_Test_Report_nX_20190705_docx_cpdf.pdf
  5. **IT99' Benchmark Radiation report** [EDMS: 2261505], A. Scialdone, R. Ferraro, link: https://edms.cern.ch/ui/file/2261505/1/PSI_Test_Reports-NanoXplore_v3_docx_cpdf.pdf
  6. **IT99' Benchmark Radiation report** [EDMS: 2319932], A. Scialdone, R. Ferraro, link: https://edms.cern.ch/ui/file/2319932/1/PSI_Test_Reports_November-NanoXplore.pdf
- PolarFire Test reports:
  7. **PSI Radiation report** [EDMS: 2475661], R. Ferraro A. Scialdone, link: https://edms.cern.ch/ui/#!master/navigator/document?P:1382953417:100764438:subDocs
  8. **ILL Radiation report** Will be published soon.

Conclusions

- Qualification of FPGA is a complex and long process but necessary and worth it
- Current project developments are profiting from past qualifications (SmartFution 2 and Igloo 2)
- New FPGA landscape bringing new performances possibilities pushed for new FPGA qualifications
- NG-Medium deeply qualified showed to be of a great interest in terms of TID lifetime and single elements response but actual design implementation and CMIC working operation are limiting the use
- Preliminary results of the PolarFire showed also great results, the huge gain of lifetime and the reduced functional element sensitivity will give new system design possibility
- Thermal neutron sensitivity non-negligible, to be fully assessed
- The PolarFire is still under qualification more tests are planned to complete it

Thank you for
your attention!

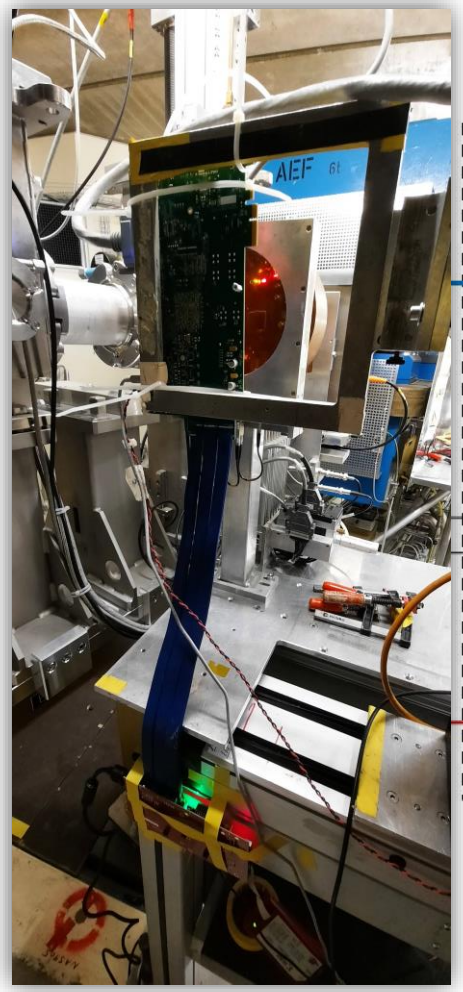
CERN

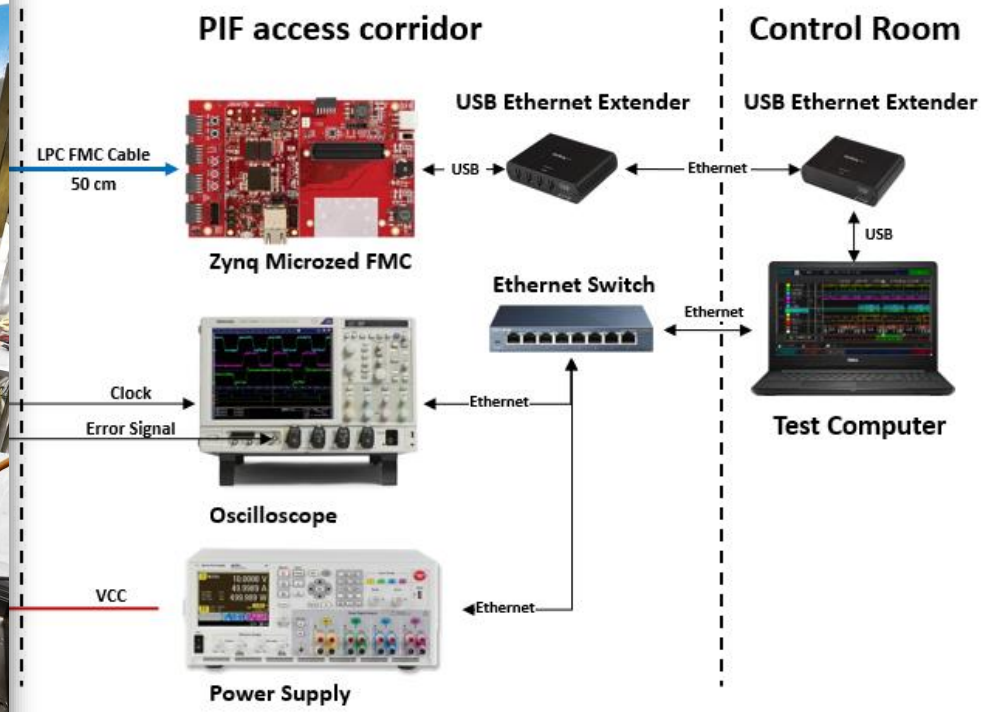
R2E

Controls
Electronics &
Mechatronics

Improved Test Setup

- FPGA Test setup improved by using a second FPGA (Zynq MicroZed) as tester instead of Built-In Self Tests (BISTs)
  - → Prevents interpreting tester errors as test structure errors
  - → Allows more complex error processing to be performed in the Tester
  - → Use of 50 cm FMC cable between tester and DUT allows protecting the tester from radiation and to reach high frequency test (up to 220 MHz tested)



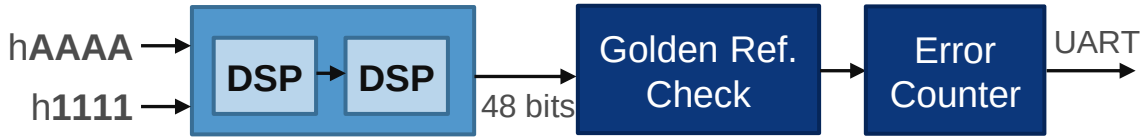


NG-Medium: Functional Elements Test Structures

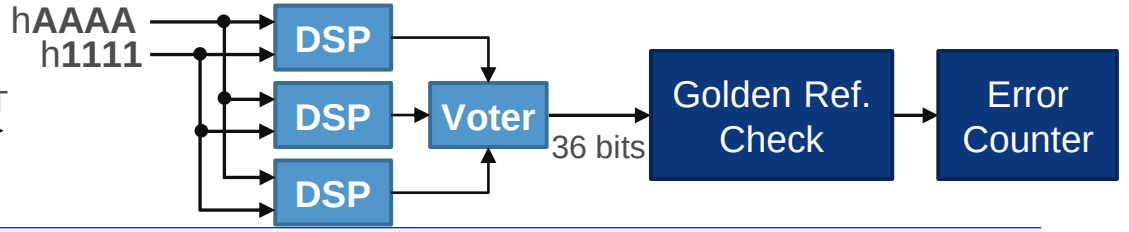
- **CRAM:** 6 Mbits, tested in static, CMIC disabled during test

- **PLL:** Input: 25 MHz, Output: 12.5 MHz, 4 PLLs
- **BRAM:** No ECC (49 kbits per block), Slow & Fast ECC (32 kbits per block)
- **Flip Flops (FFs):** 8 chains of 3072 FFs for each configuration
- **DSPs**: 18-bit multiplication
  - **Simple Multiplication:** 96 DSPs instantiated

  - **Double Multiplication:** 32 double DSPs instantiated



- **Test Protocol during Irradiation:**
  - Same multiplication operation performed continuously
  - Outputs are compared at each clock cycle
  - Each error are sent via serial
- **Triplicated DSP:** 32 DSPs instantiated



NG-Medium: B13 Test Structure

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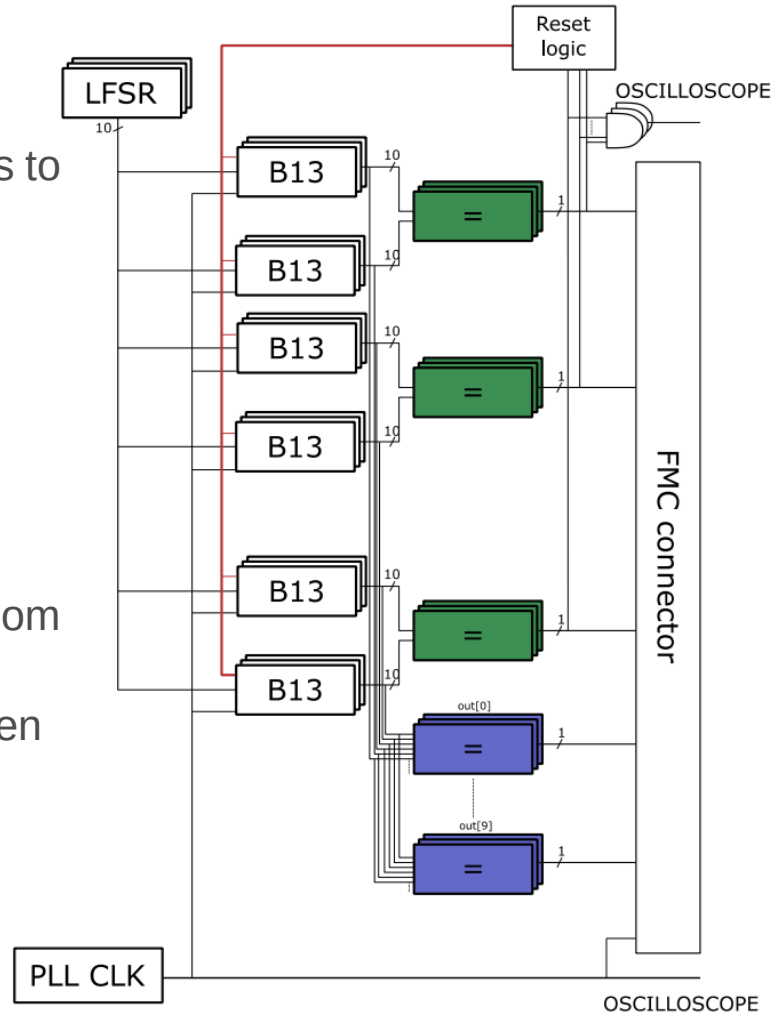
- **The B13 is a pure FSM** and is composed of: 339 gates, 53 FF and its input/output interface has 10 bits
- **These circuits are compared two by two** and the output of the comparators are sent to the Zynq through FMC.
- In case of error the Zynq reset all the structures
- Circuits are fed by a linear feedback shift register (LFSR) generating random inputs
- In addition B13 output bit-to-bit comparators and a global and gate between all the circuit-to-circuit comparators are implemented to gather more information



NG-Medium: Expected failure rate in operation

- Considering the B13 circuit, which is a rather small design compared to typical LHC ones, the annual failure rate in operation would be the following for the High-Luminosity LHC conditions:
  - **Tunnel (IR1 Q1-Triplet): HEH Fluence:** ~$1 \cdot 10^{13}$ HEH.cm^{-2} /year, **TID**: ~ 2 kGy /year
    - **Single** B13 circuit CMIC reset: **~ 0.4** /year
    - **Single** B13 circuit unknow reset: **~ 10** /year
    - **Single** B13 temporary failures: **~ 1.41** /year
  - **Tunnel (9R5 DS area): HEH Fluence:** ~$3 \cdot 10^{12}$ HEH.cm^{-2} /year, **TID**: ~ 100 Gy /year
    - **Single** B13 circuit CMIC reset: **~ 0.07** /year
    - **Single** B13 circuit unknow reset: **~ 3** /year
    - **Single** B13 temporary failures: **~ 0.42** /year

$$N_{SEE\_Failure} = \boldsymbol{N} * \sigma * fluence$$

Number of systems

Example in LHC-DS: 18 cells = 18 units
→ 54 resets/year

NG-Medium: B13 TMR routing example

- **Example of common long input routing for a triplicated circuit:**