DIDT

WP18

HiLumi HL-LHC PROJECT

Greg Daniluk

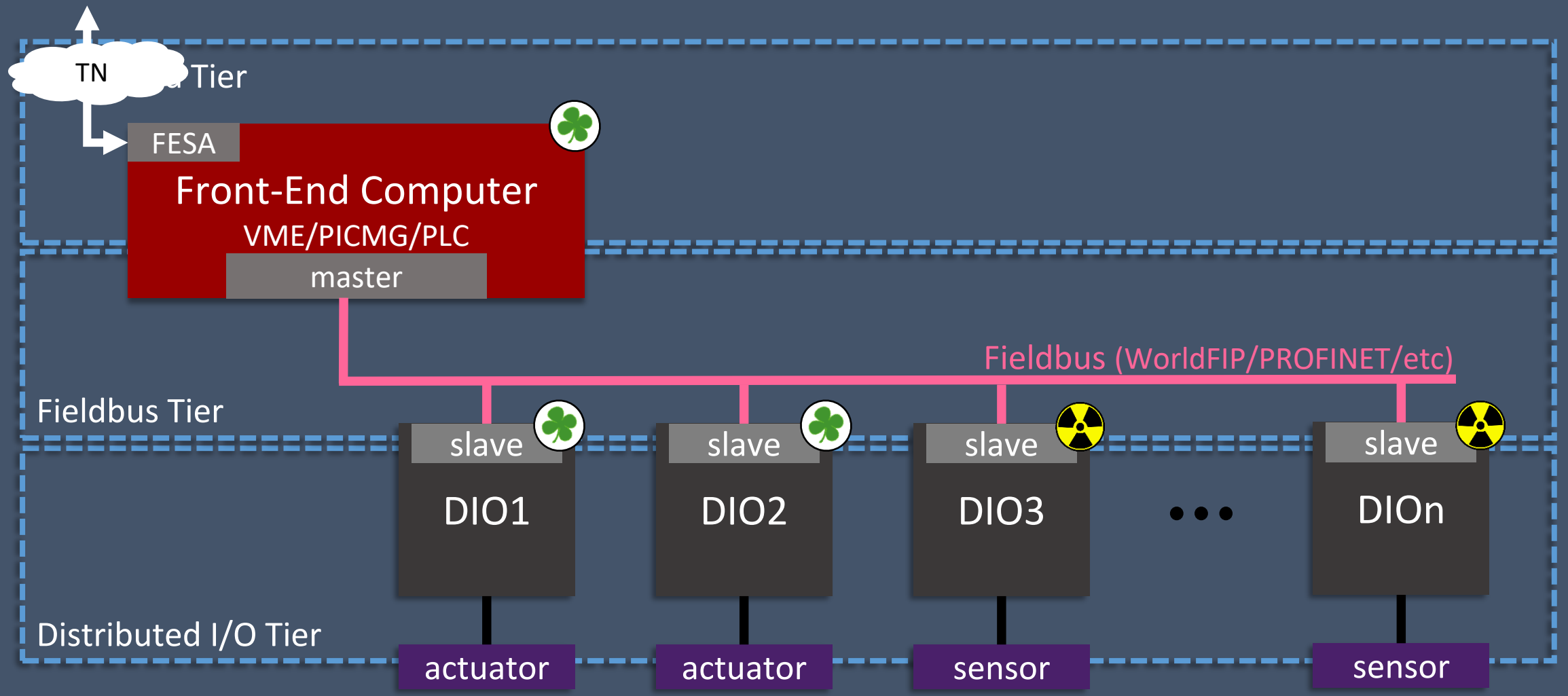
BE-CEM-EDL

R2E

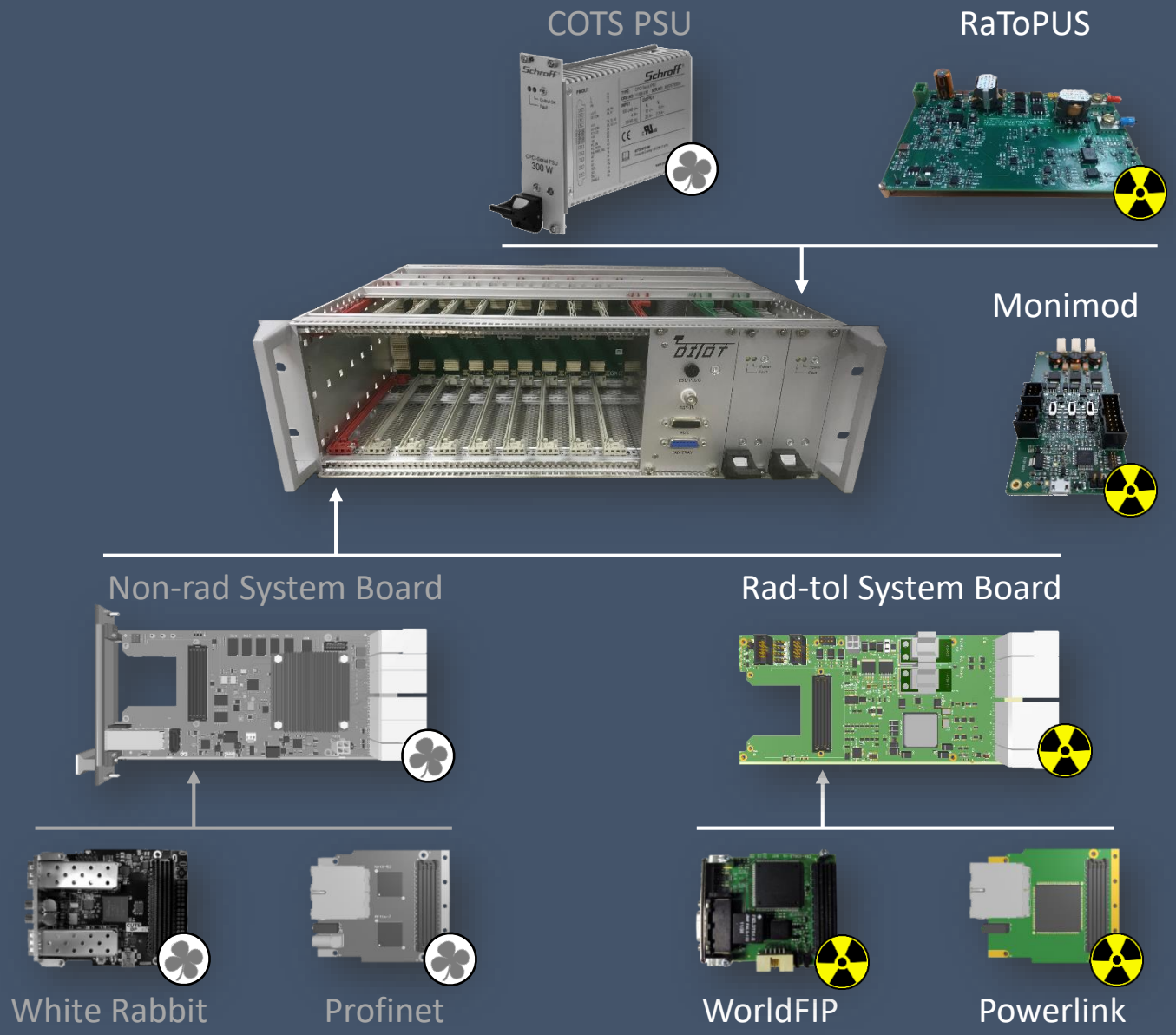
Annual Meeting, 2-3 Feb 2021

Controls Electronics & Mechatronics

Custom electronics architecture



Modular DI/OT Platform

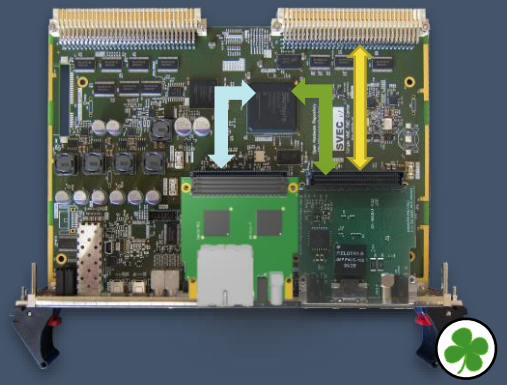


See the talk by Lalit Patnaik

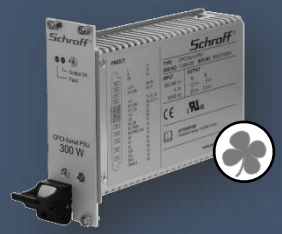
See the talk by Christos Gentsos

Modular DI/OT Platform

ProFIP



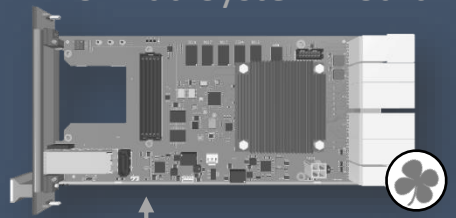
COTS PSU



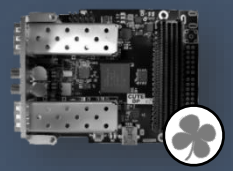
RaToPUS

Monimod

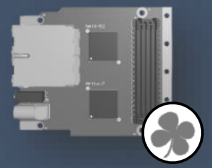
Non-rad System Board



Rad-tol System Board

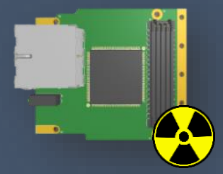


White Rabbit



Profinet

WorldFIP



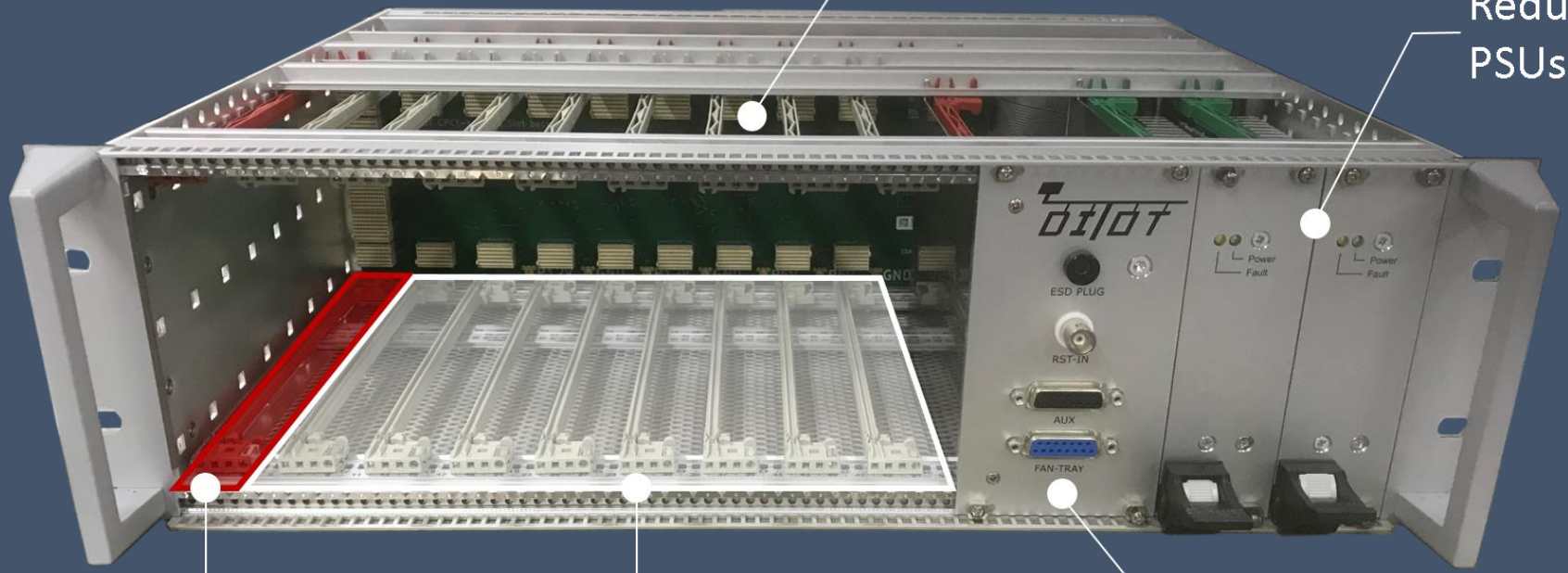
Powerlink

High-reliability strategy

See the talk by Volker Schramm

3U Crate

19” rack variant



System Board

Peripheral Boards
- Application-specific

Front Panel
- Power Cycle Request BNC
- Fan Tray Connector

Produced by:

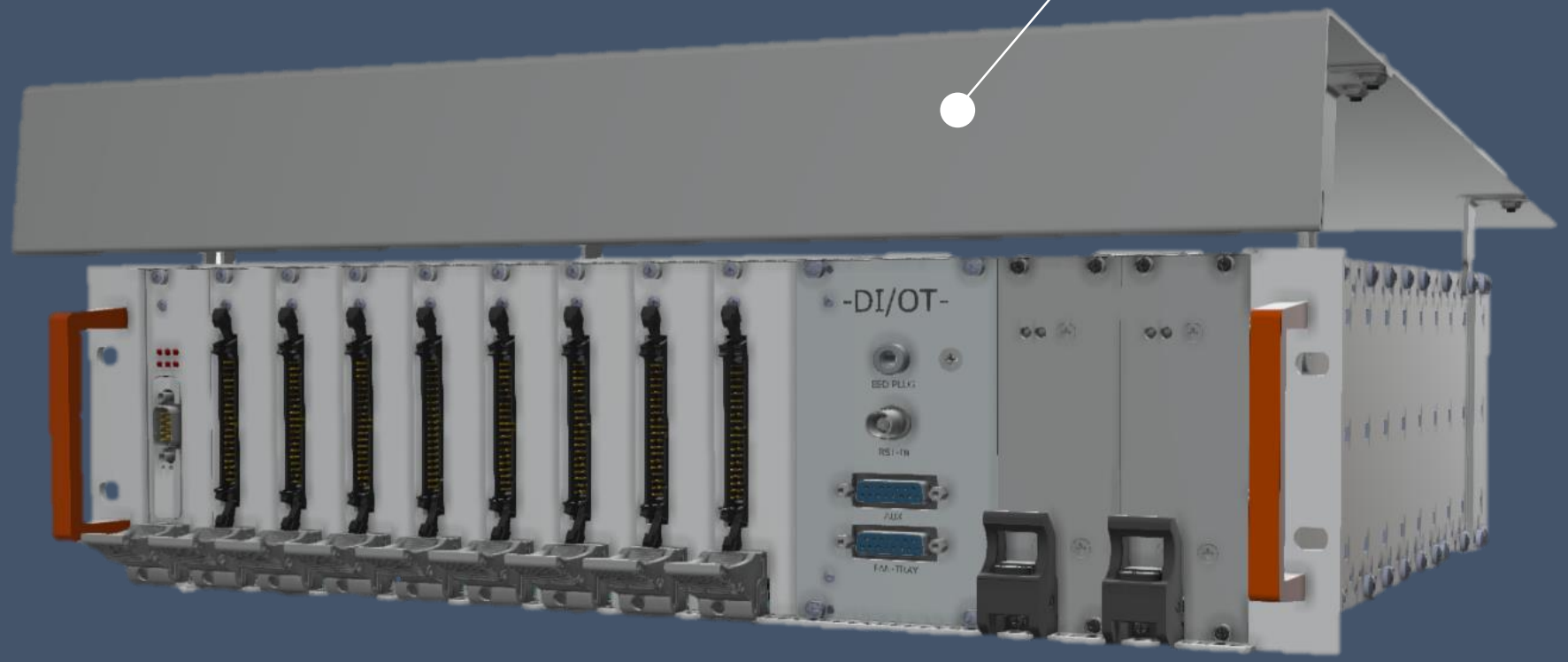
creo TECH Instruments S.A.

ELMA Your Solution Partner

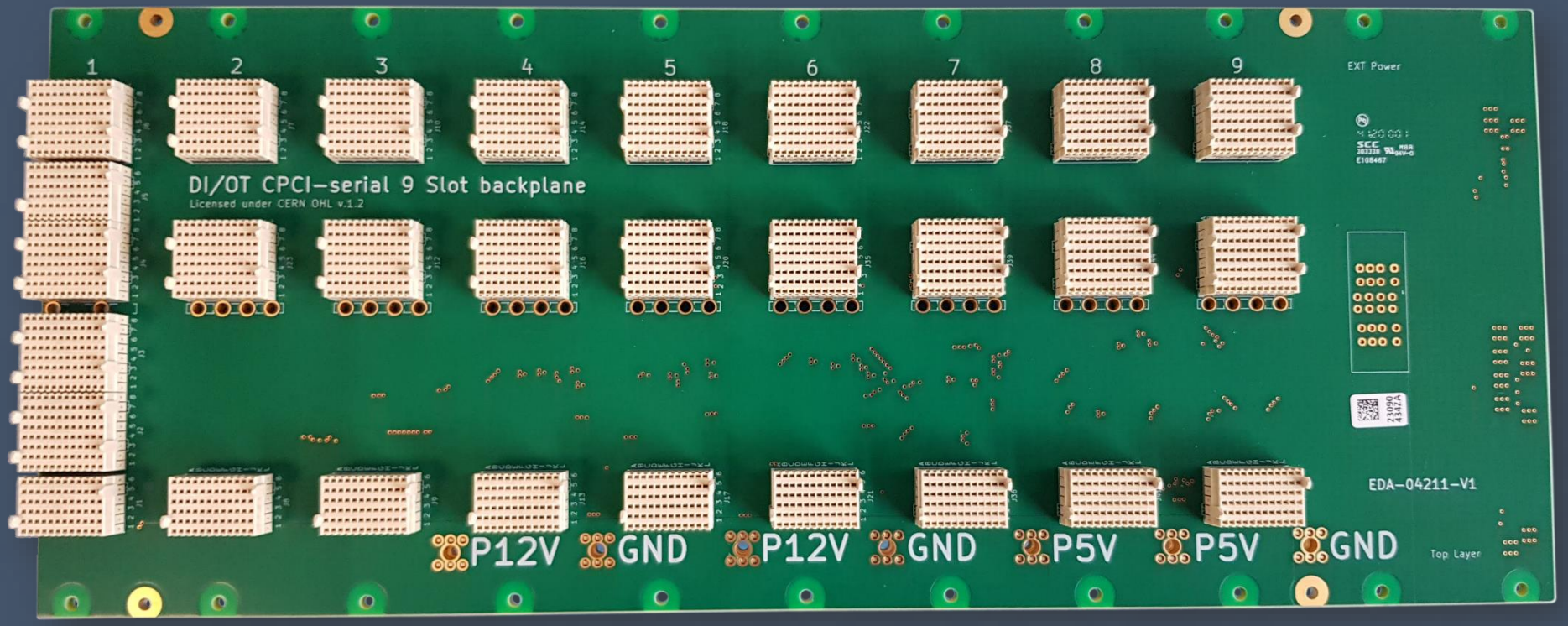
nVent SCHROFF

3U Crate

Tunnel variant



Backplane

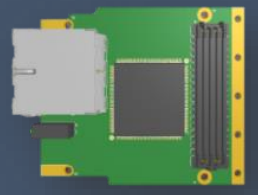


- CPCI-S.0 industrial standard
- 9 slots, fully passive – no radiation testing
- Star of lanes from System to Peripheral Slots
- Free choice of inter-board communication

Fieldbus Mezzanines

WorldFIP
THE EFFECTIVE FIELDBUS

- ProASIC3 with nanoFIP
- Different speed variants up to 2.5Mbps
- Prototypes produced
- … using rad-qualified components



ETHERNET POWERLINK

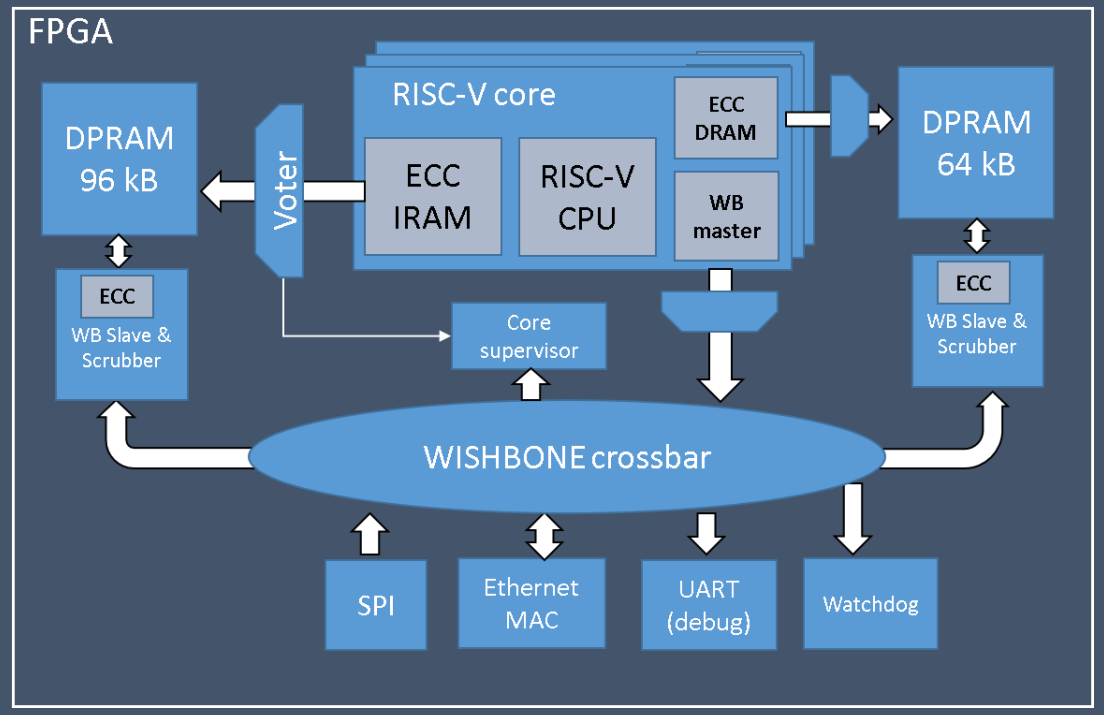
- Igloo2/Smartfusion2
- Max speed 100Mbps
- Rad-tested Ethernet Phy
- Hydra SoC architecture – triplicated RISC-V *(https://ohwr.org/project/hydra)*

Recipe for rad-tol Ethernet

1. Ethernet PHY research by R2E: Microchip KSZ8081 (BER <9e-11: 0-400Gy)
2. HDL architecture: Ethernet MAC, Switch/Hub, processor – Hydra SoC
3. Mitigation techniques:
   - Local TMR: peripherals
   - ECC protection for instruction & data RAM
   - Scrubber for RAM
   - Block TMR: Risc-V processor
   - Manual placement constraints

Tested in PSI in 2020: TID 500Gy; cross-section ~3e-12

4. Ethernet cycle-based data exchange
   - OpenPowerlink software stack in Hydra
   - PSI tests in 2021

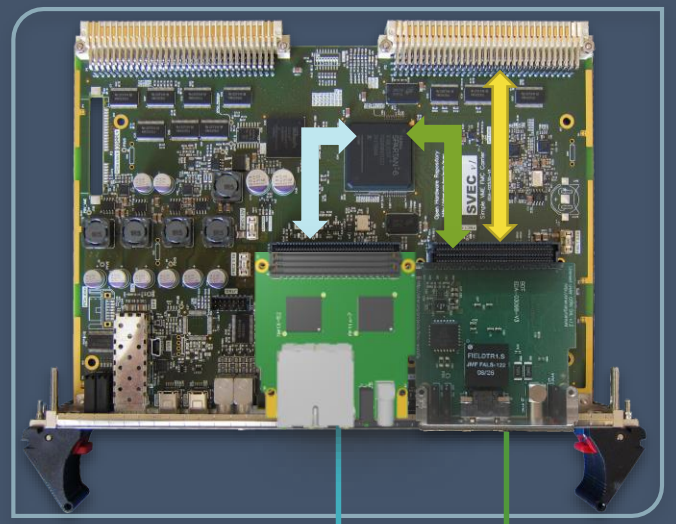


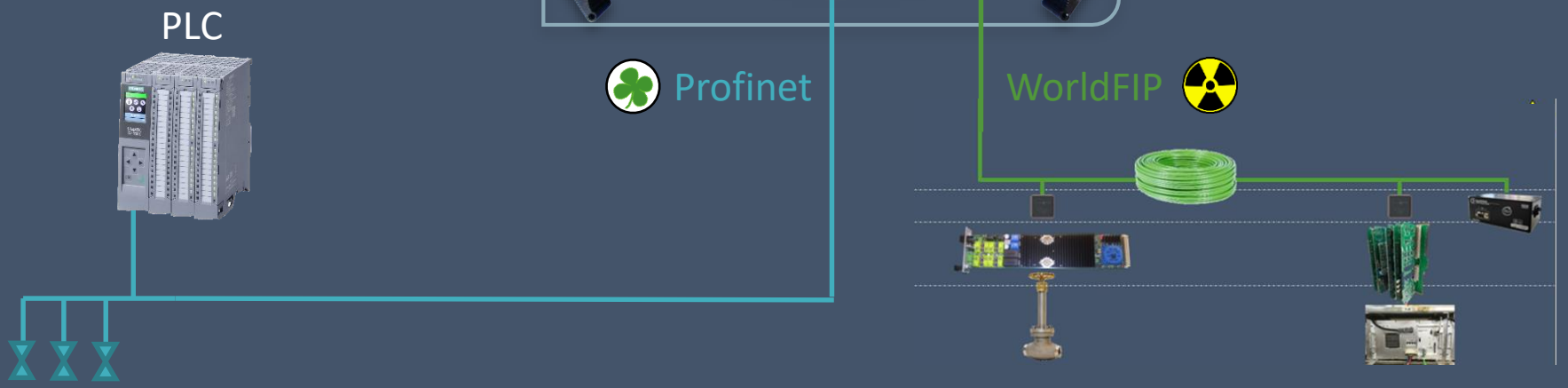
ProFIP

Translator Profinet ↔ WorldFIP

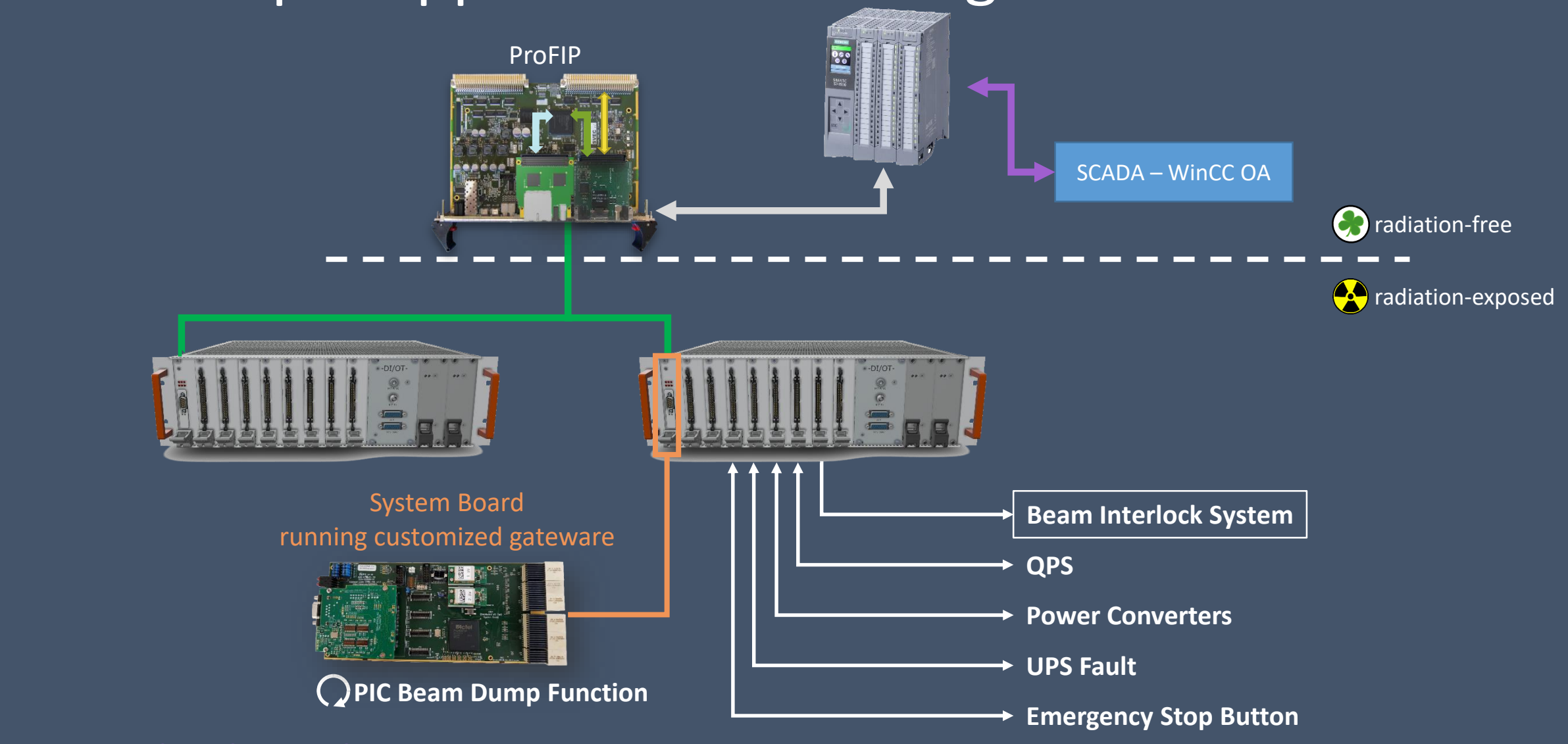
1U VME crate
- Boot-time configuration

FPGA-only translation
- Determinism
- Robustness





Example Application: Powering Interlock Controller



Courtesy of Alain Antoine (TE-MPE-MI)

Locations and radiation levels

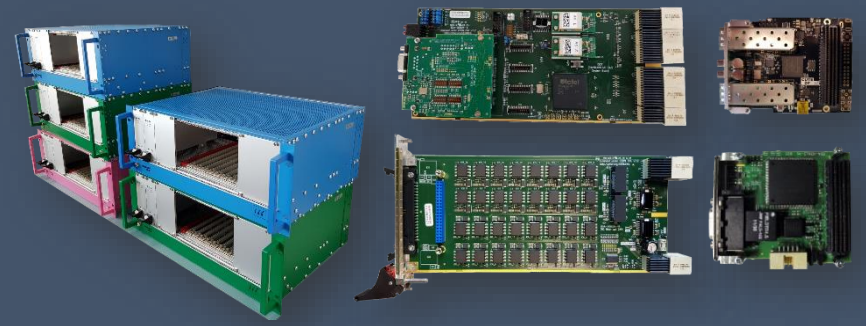
- RRs *3/*7 in P1, P5, P7
- UAs 13/17/53/57
- Transfer lines: Ti2, Ti8, TT41-43

Annual HL-LHC radiation levels[1]

	TID [Gy]	**HEH [cm^{-2}]**	**1MeVn-eq [cm^{-2}]**
RR13-17-53-57 L1	25	$1.4 * 10^{10}$	$7 * 10^{10}$
RR13-17-53-57 L0	15	$1 * 10^{10}$	$7 * 10^{10}$

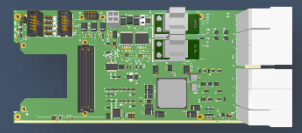
[1] *EDMS No. 2302154 V1.0 Radiation Level Specifications for HL-LHC*

Timeline



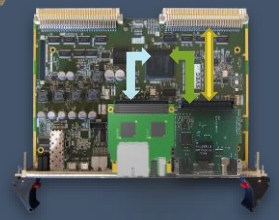
2018 Q4 First **proof of concept** available for lab developments

2020 Q2 **Crate and backplane** designed



2021 Q1 **Rad-tol** System Board prototype

Q3 **RaToPUS** ready



Q4 **ProFIP prototype**

2022 Series **production/procurement** starts

2025 HL-LHC **deployments**

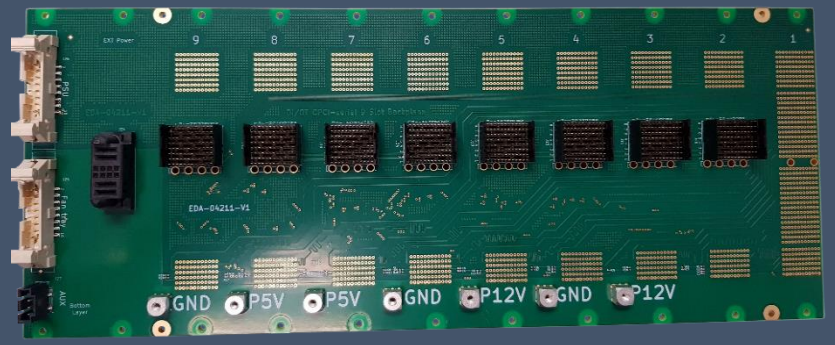
- **Modular** platform for **custom** electronics
- **Radiation-exposed** and **radiation-free** areas
- **Customised** by Peripheral Boards and FPGA firmware
- Interfacing with **custom electronics** and **industrial controls**

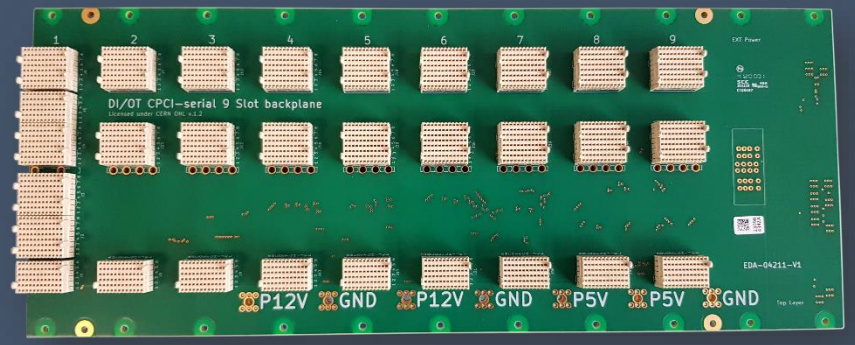
- **Collaboration** between CERN groups and industry for HL-LHC – join us!

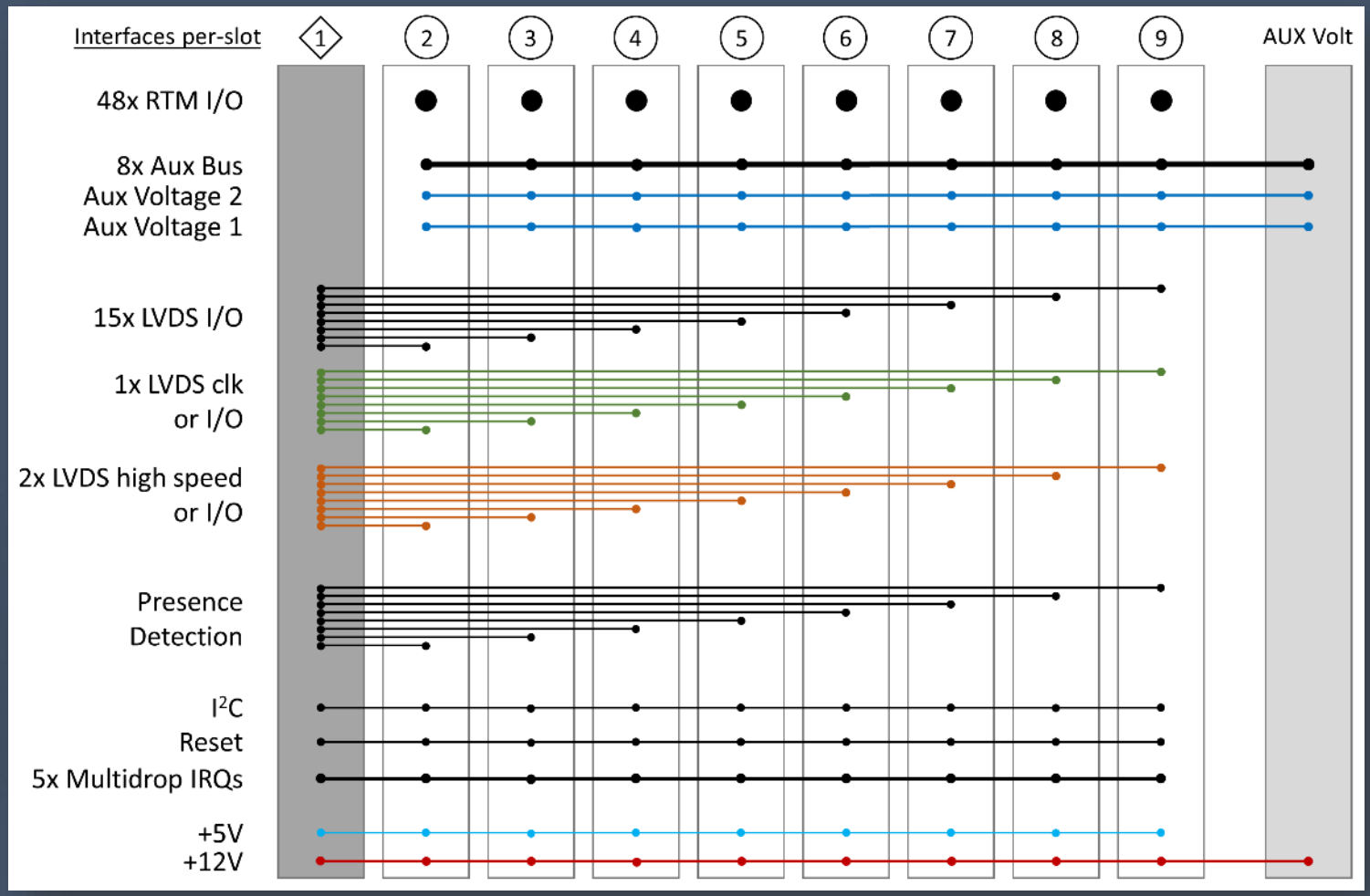
https://ohwr.org/project/diot/wikis

Backup Slides

Backplane

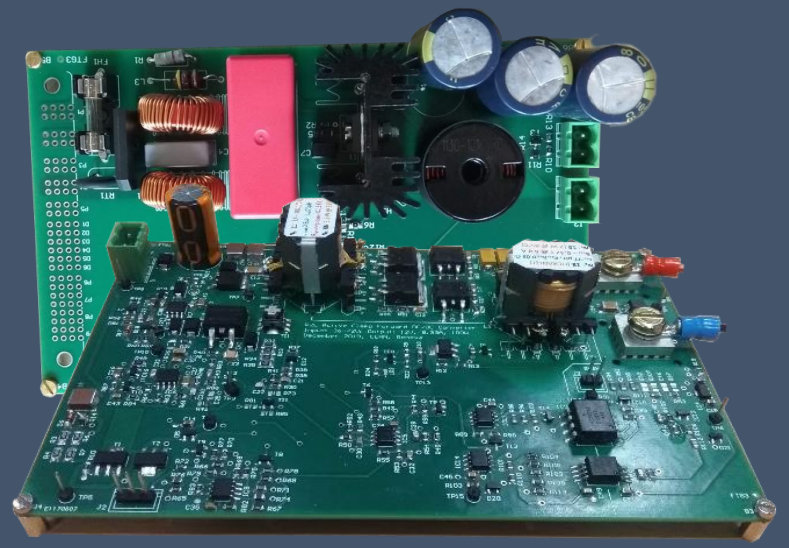

GND
P5V
P5V
GND
P12V
GND
P12V


DI/OT CPCI-serial 9 Slot backplane
P12V
GND
P12V
GND
P5V
P5V
GND

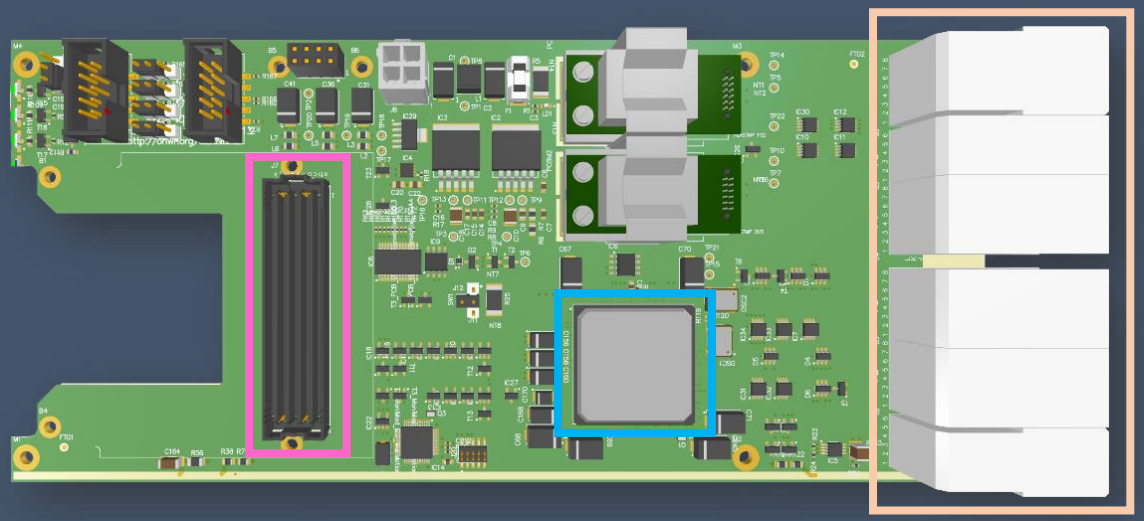

Interfaces per-slot
1
2
3
4
5
6
7
8
9
AUX Volt
48x RTM I/O
8x Aux Bus
Aux Voltage 2
Aux Voltage 1
15x LVDS I/O
1x LVDS clk
or I/O
2x LVDS high speed
or I/O
Presence
Detection
I²C
Reset
5x Multidrop IRQs
+5V
+12V

RaToPUS – rad-tol PSU

- **100W** switched-mode AC/DC
- Design in collaboration with SY-EPC
- DC outputs: **12V (100W); 5V (10W**)
- Compatible with CPCI-S.0 standard
- Standard PMBus monitoring
  - Voltage, current
  - Temperature
- See the talk by Lalit Patnaik



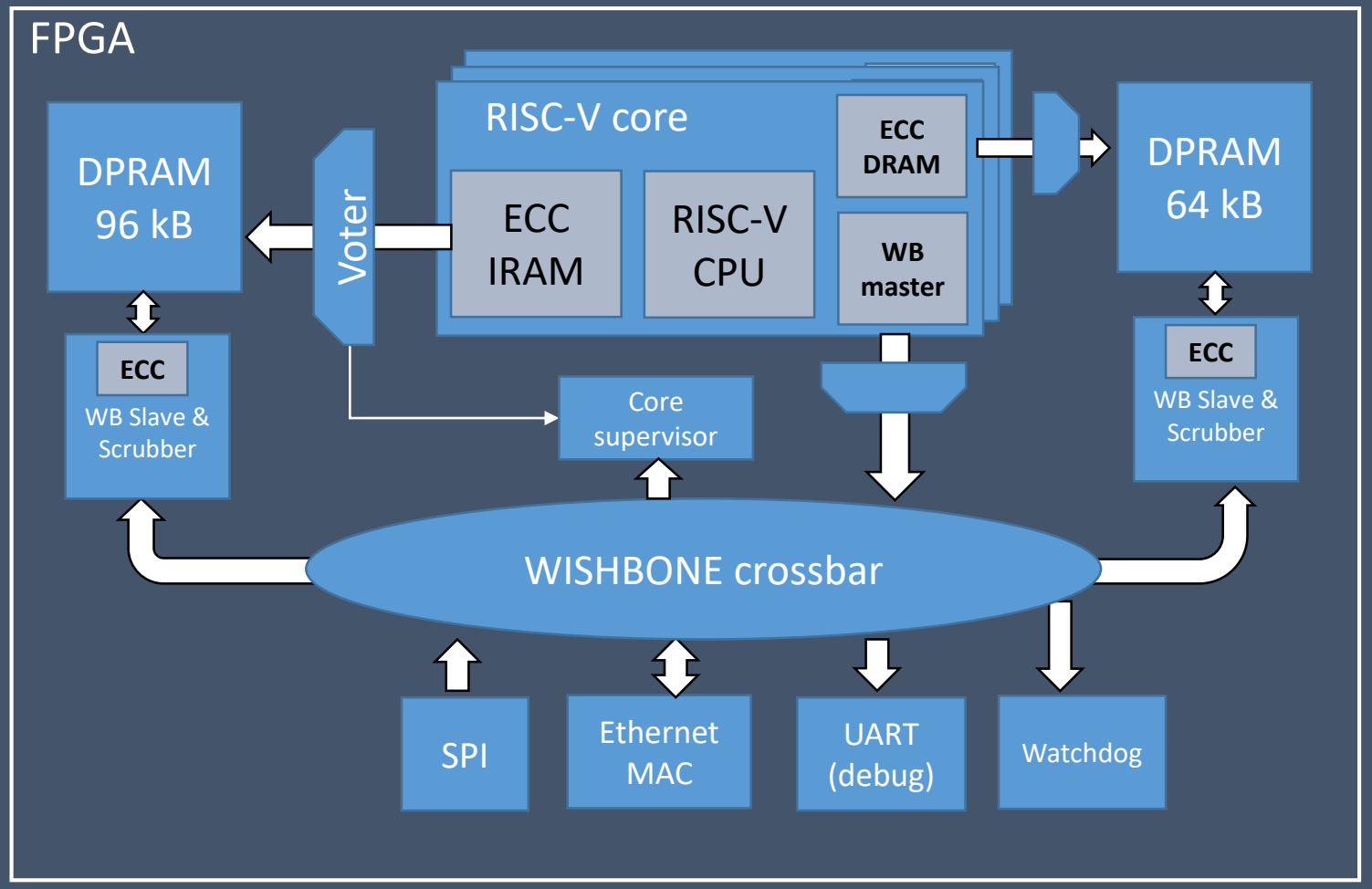
System Board



- Central FPGA board of DI/OT crate
- Fieldbus FMC ↔ Igloo2 FPGA ↔ Peripheral Boards
- Implements crate diagnostics
- See the talk by Christos Gentsos

Hydra SoC Architecture

Generic architecture for FMC Powerlink and rad-tol System Board



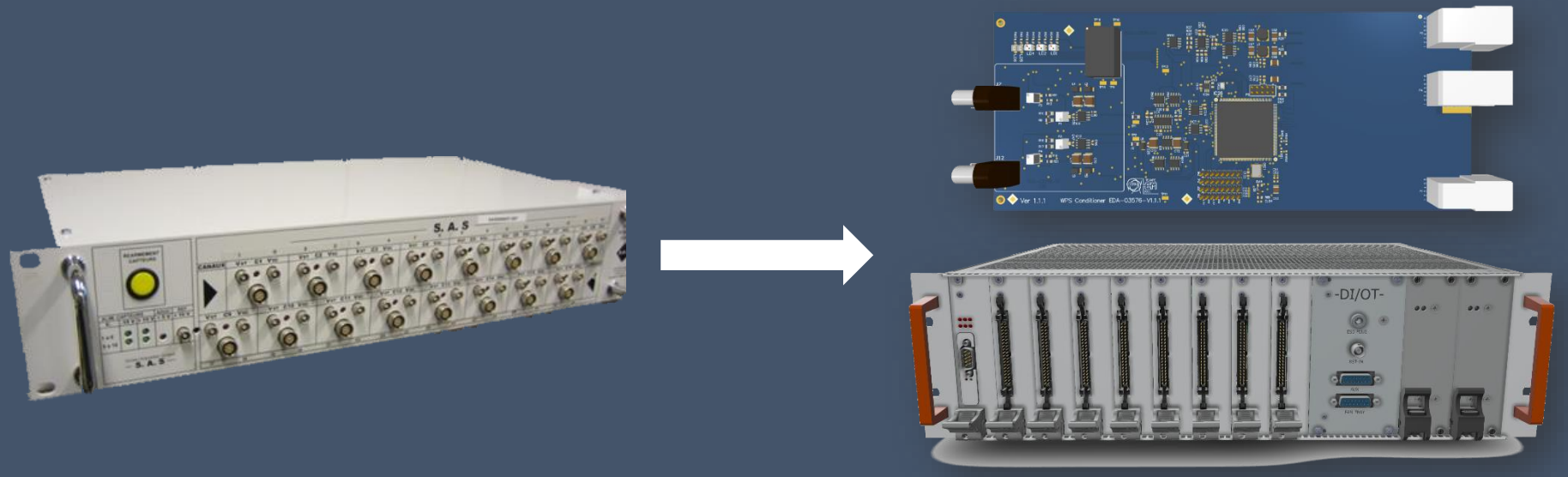
- Triplicated RISC-V
  - 50MHz
  - Watchdog
- ECC RAM in the FPGA
  - 96 kB code
  - 64 kB data
- Interfaces
  - SPI
  - UART
  - Ethernet MAC with DMA

Full Remote Alignment System (BE-GM)

Micrometric remote alignment of LSS* in IP1 and IP5 for HL-LHC

Survey:

- Readout of precise positioning sensors
- 4x more systems than currently
- DI/OT crates in radiation communicating over WorldFIP

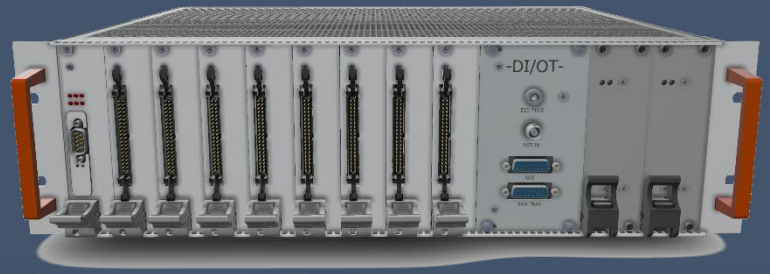


*LSS = Long Straight Section

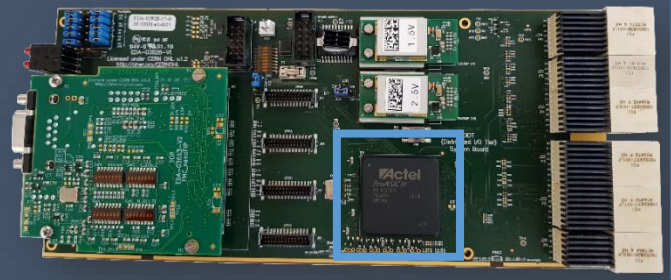
Courtesy of M.Sosin (BE-GM-HPA)

Fast Interlocks

- When ~1us reaction times are required
- When PLCs are not fast enough



Configuration
Monitoring
Post-mortem



DI/OT backplane

TTL pulse

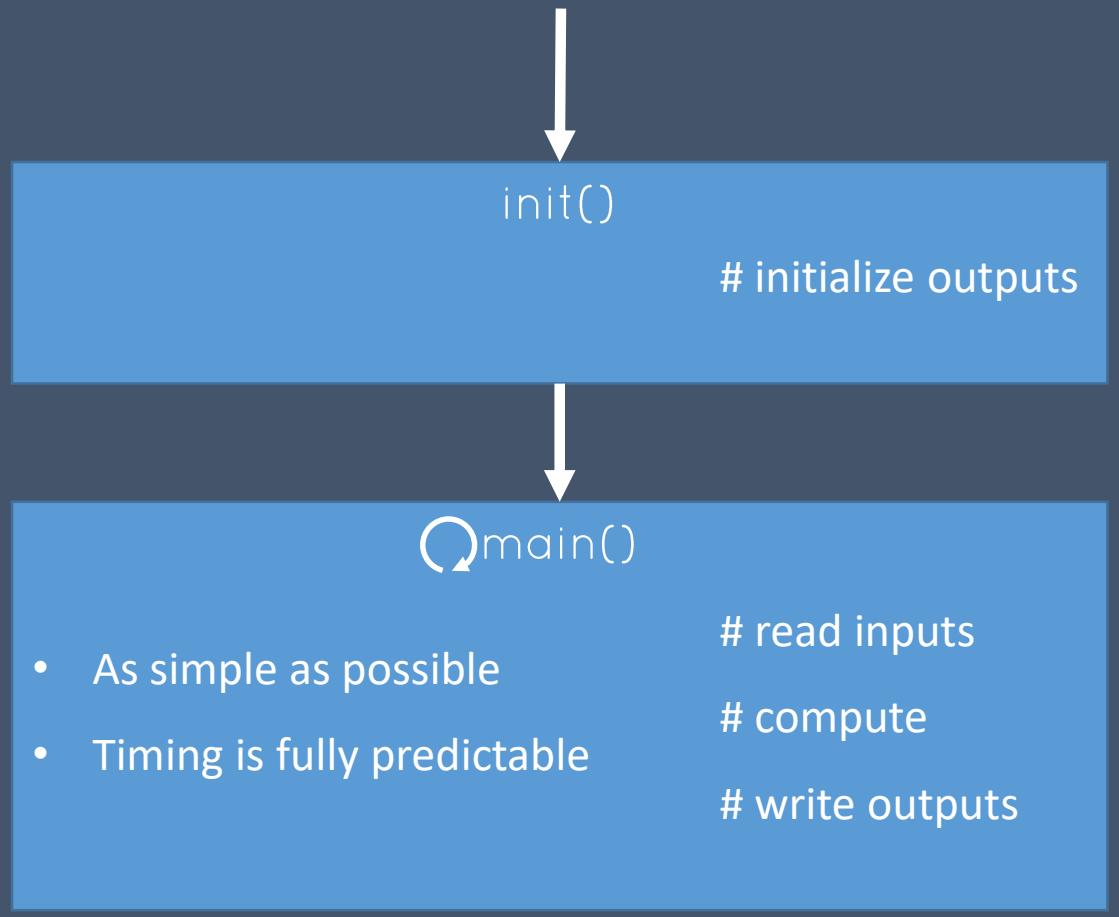
System Board running interlocks algorithm in deterministic soft-CPU

Peripheral Board + DIO FMC

radiation-free

Courtesy of Tristan Gingold (BE-CO)

DI/OT fast interlocks: application




```
 1 #include <stdint.h>
 2 #include "plc_urv_regs.h"
 3
 4 #define SLOT pins_5
 5
 6 //              ch0         ch1         ch3         ch2         ch4
 7 #define OEN ((1 << 6) | (1 << 7) | (1 << 8) | (1 << 9) | (0 << 11))
 8
 9 void init (void)
10 {
11   volatile struct plc_urv_regs *regs =
12     (volatile struct plc_urv_regs *)0x00000;
13
14   regs->relays.SLOT = OEN;
15 }
16
17 void main (void)
18 {
19   volatile struct plc_urv_regs *regs =
20     (volatile struct plc_urv_regs *)0x00000;
21
22   while (1) {
23     unsigned v = regs->loops.SLOT;
24
25     v = !! (v & 0x27);
26     regs->relays.SLOT = (v << 4) | OEN;
27   }
28 }
29
```

DI/OT fast interlocks: user experience

```
# build fip_urv tool
$ make

# build Fast Interlocks application
$ make PROG=plc_dio

# load Fast Interlocks binary over WorldFIP
$ fip_urv load plc_dio.elf

# start CPU
$ fip_urv plc on
```