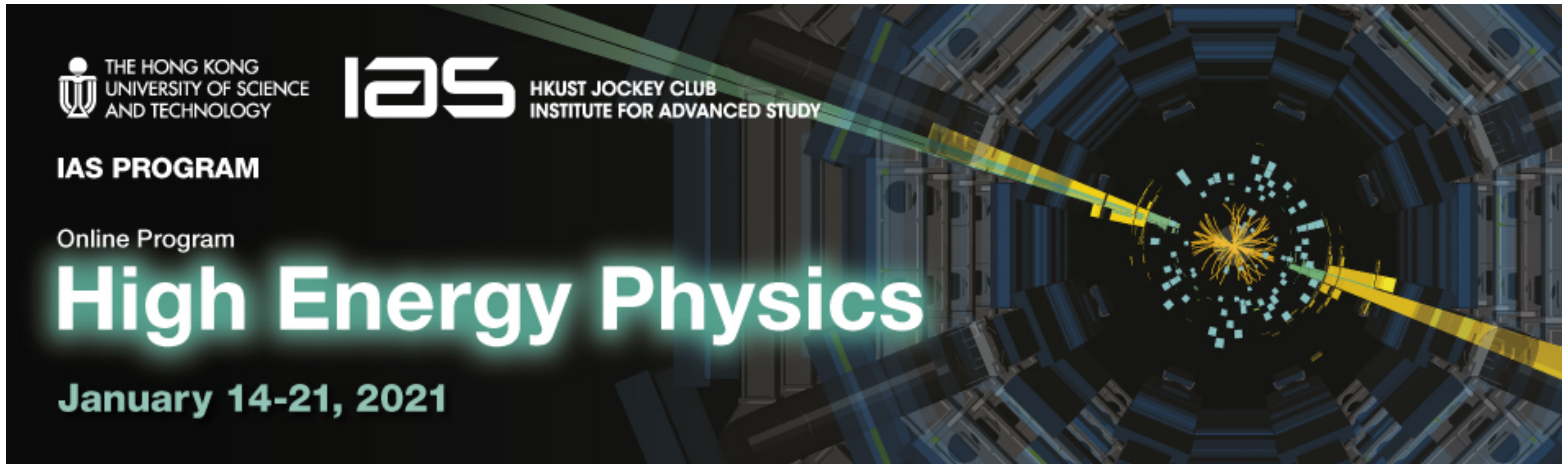
# Novel Ideas in Silicon Tracking Detector (ALICE)

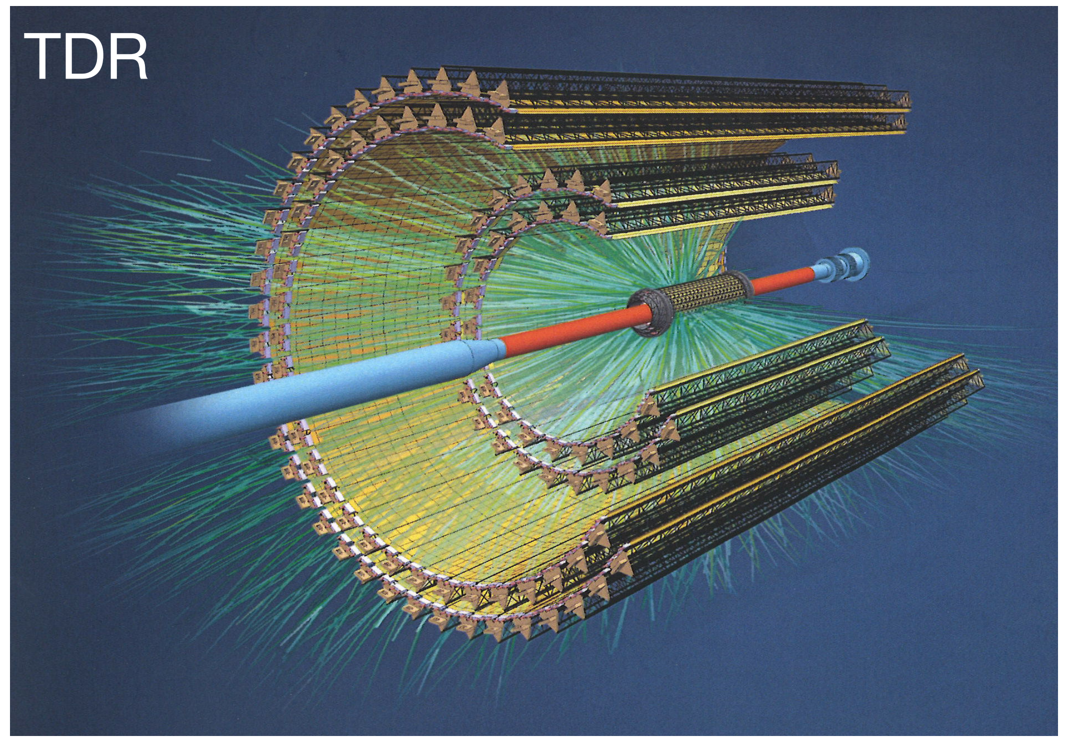
**IAS Program on High Energy Physics (HEP 2021)**
**14-21 January 2021**

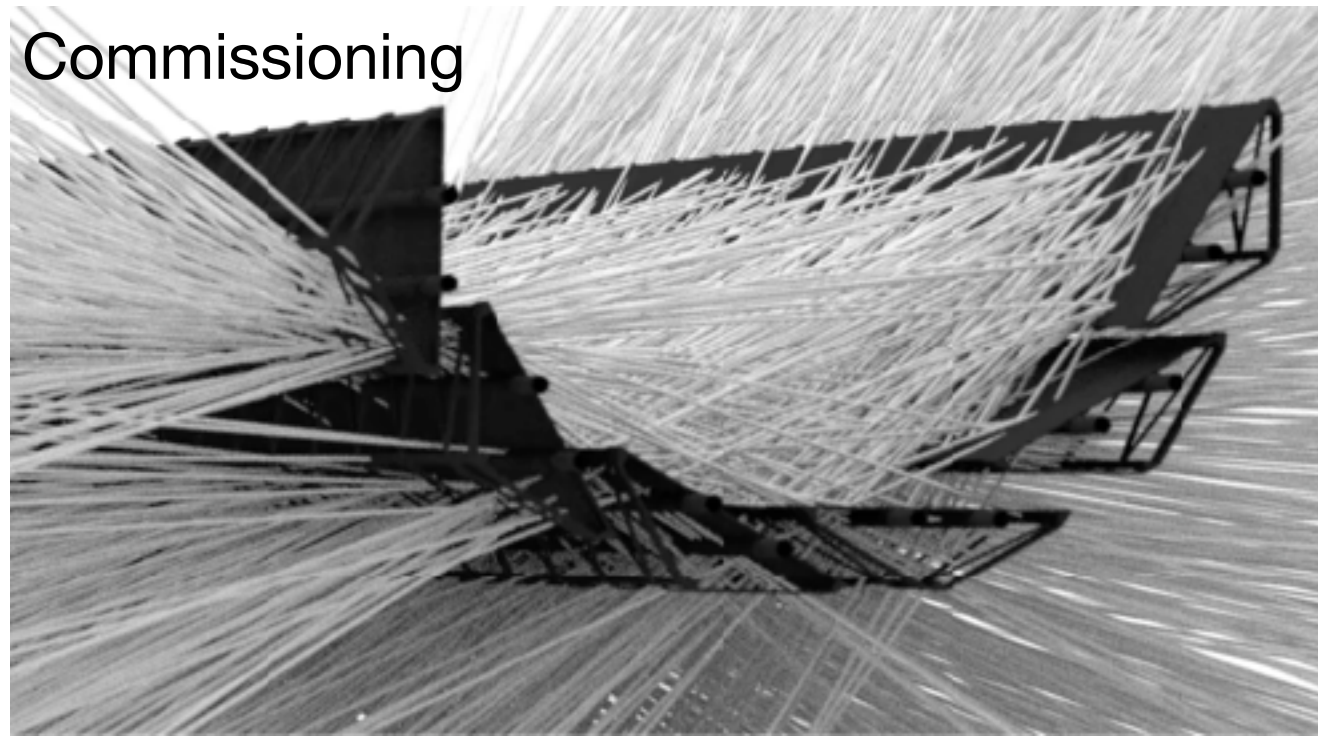
**Magnus Mager (CERN)**
***on behalf of the***
***ALICE collaboration***



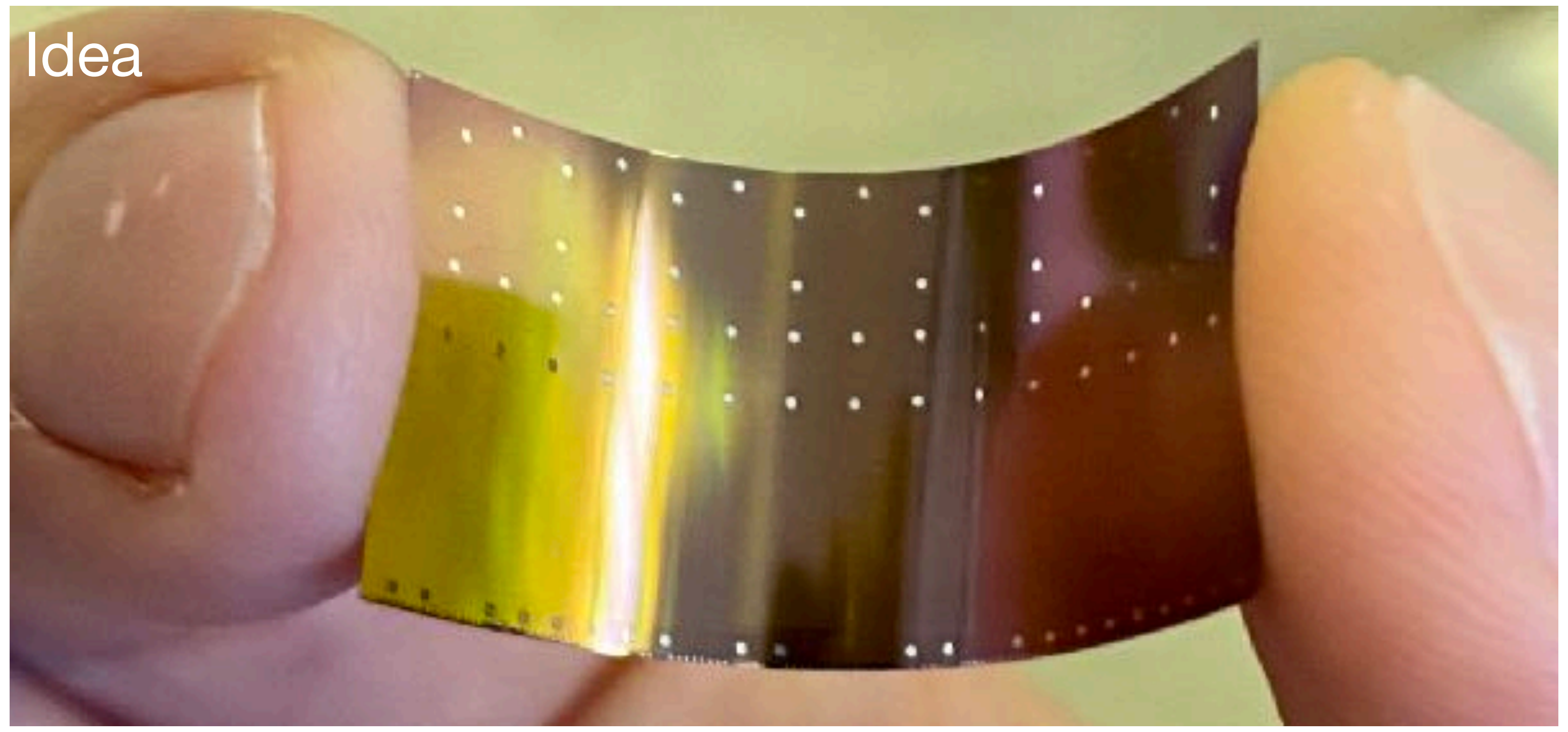
# Outline

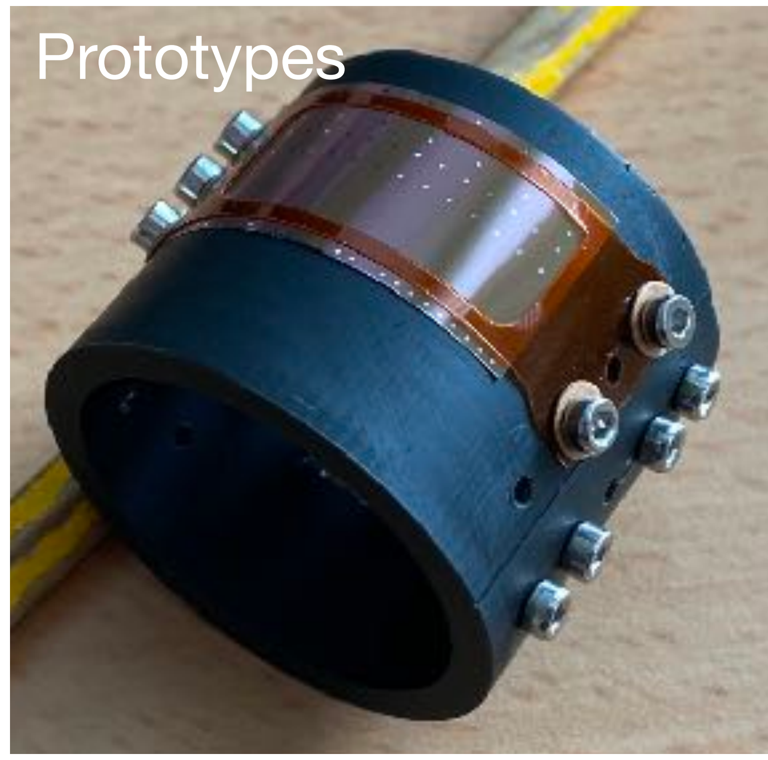
- ITS2 (LHC LS2, i.e. now)
  - Detector layout
  - ALPIDE chip
  - Highlights from commissioning



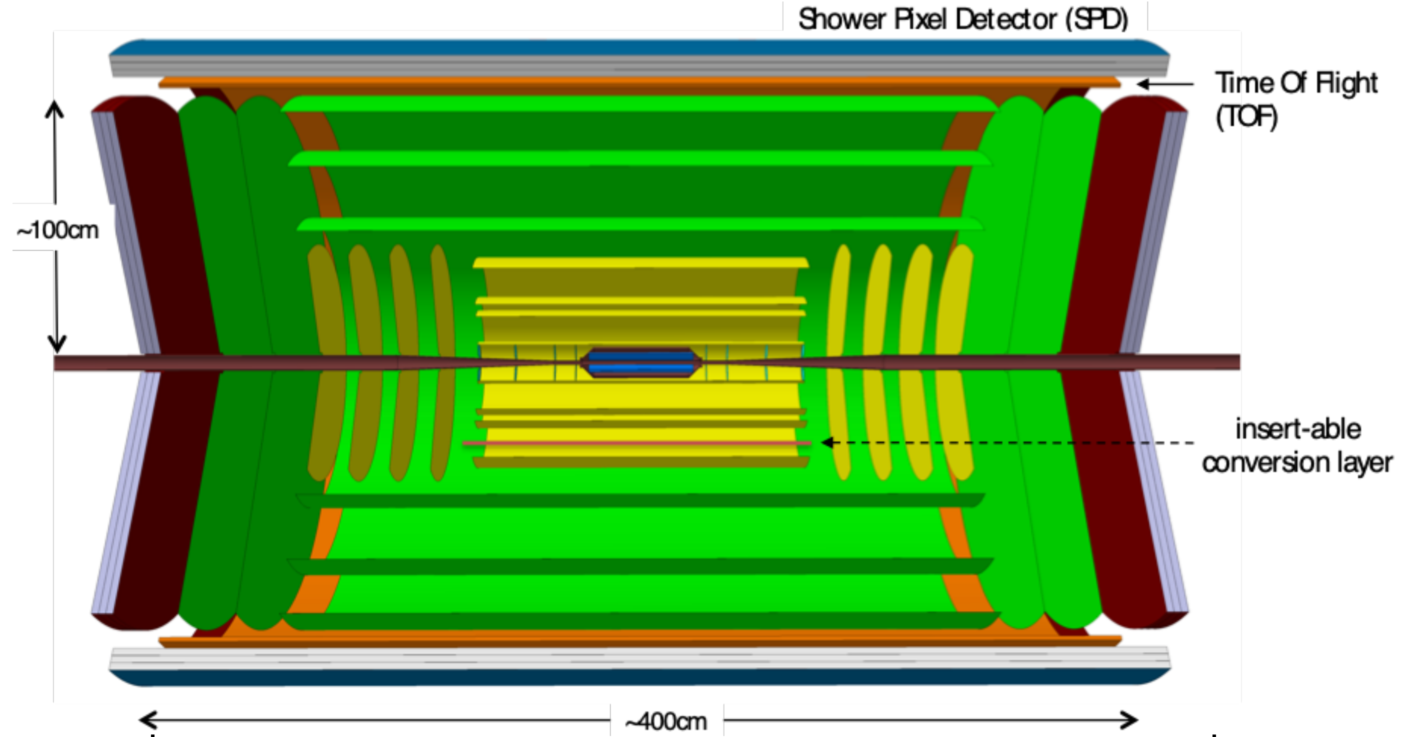




- **ITS3 (LHC LS3, i.e. soon)**
  - Detector concept + predicted performance
  - R&D on bent MAPS

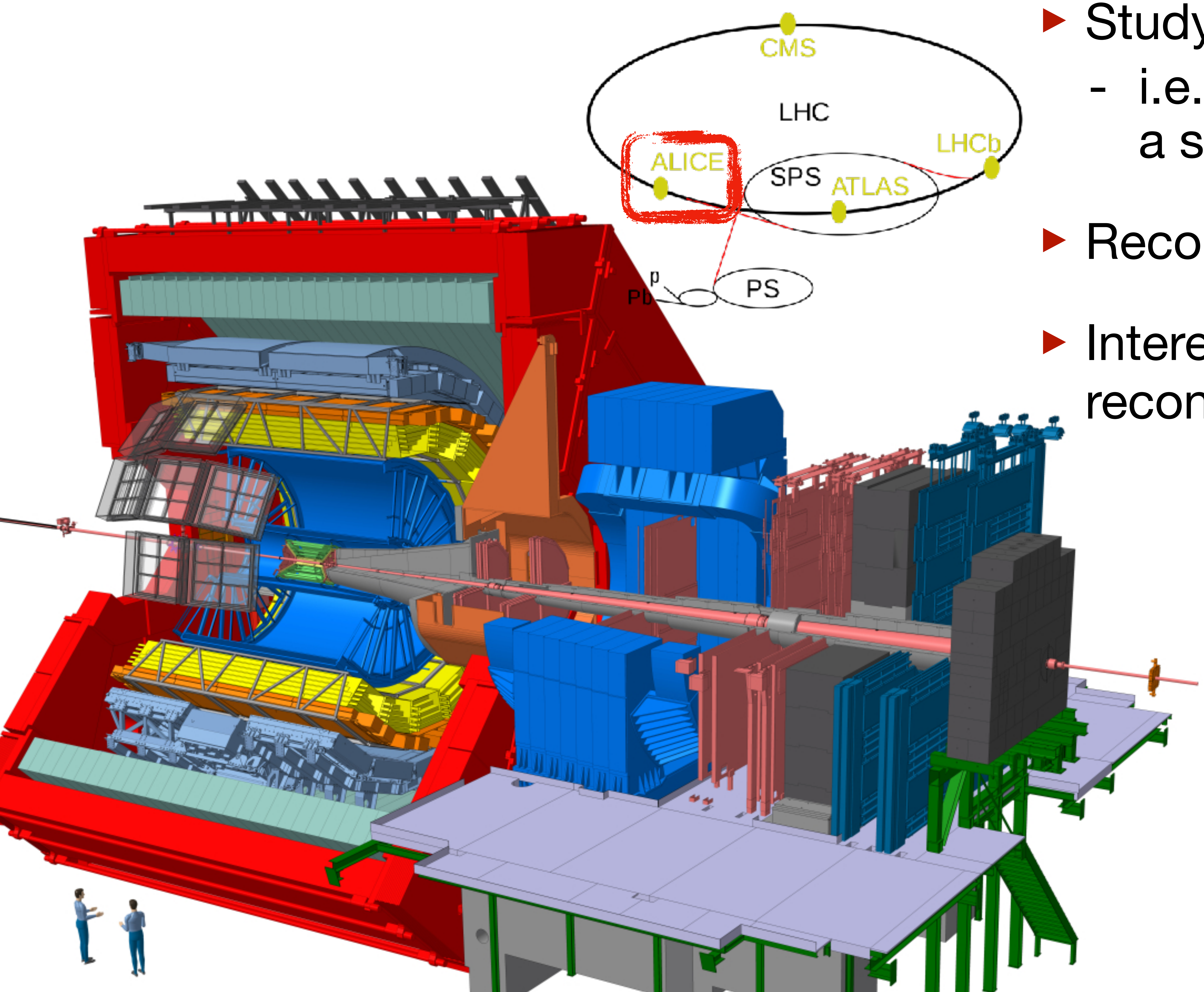


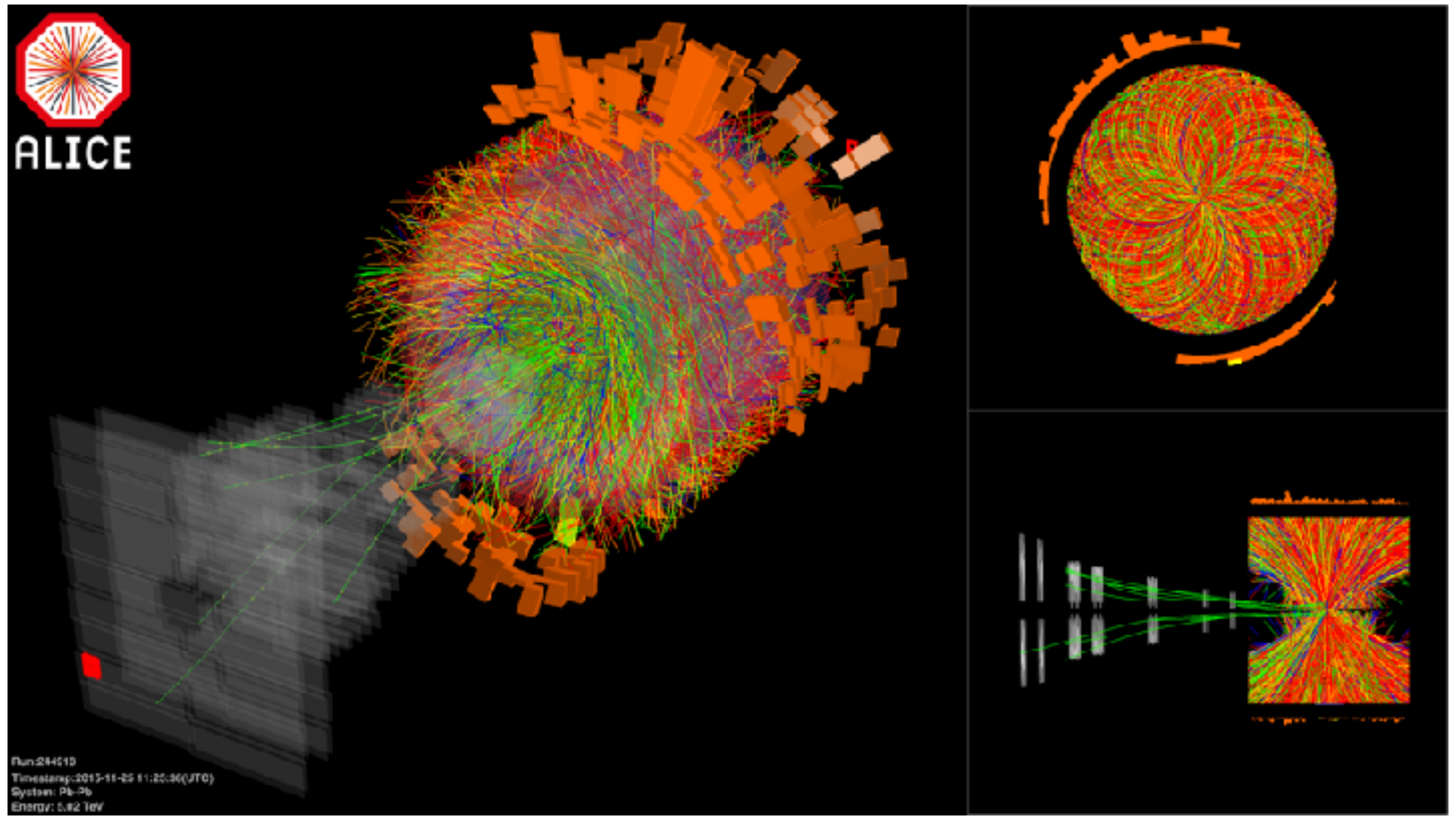

- ALICE 3 (LHC Run 5+)
  - Future Heavy-Ion experiment at LHC
  - Full-silicon detector



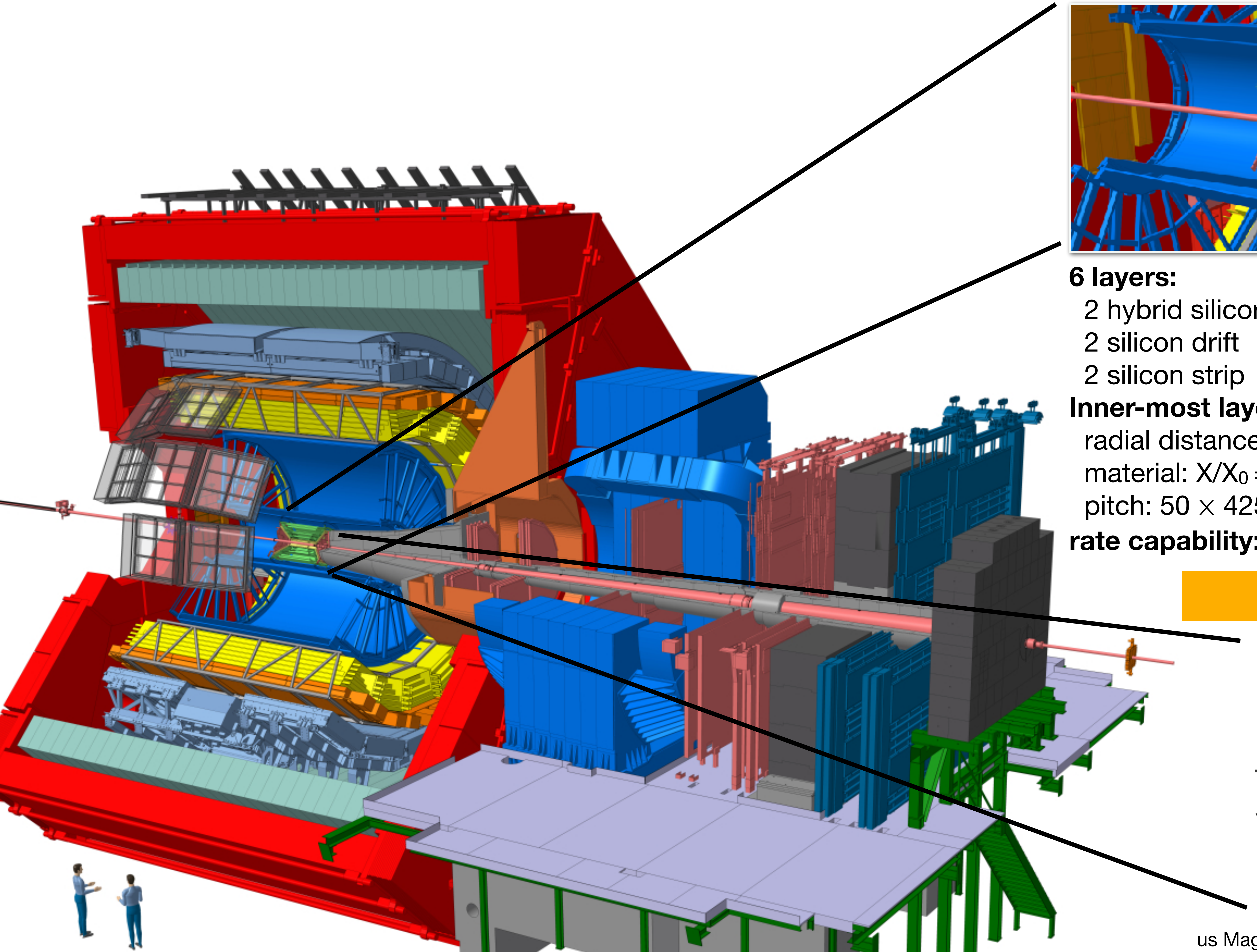
# ALICE
## Detector and main goals



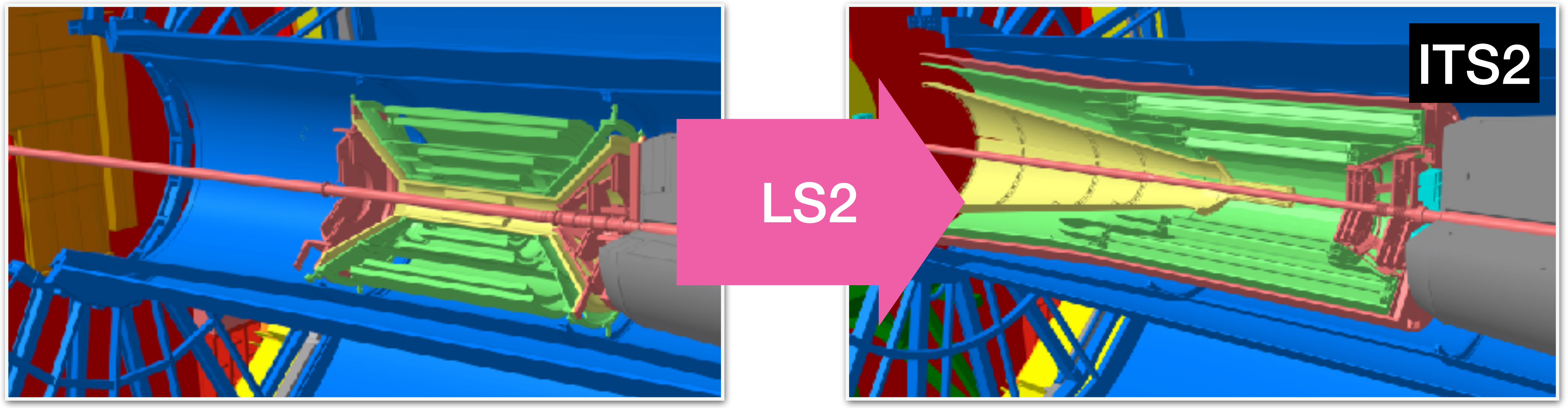

- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum (≲1 GeV/c) particle reconstruction



# ALICE today
## LS2 upgrades with MAPS



### Inner Tracking System




**6 layers:**
2 hybrid silicon pixel
2 silicon drift
2 silicon strip

**Inner-most layer:**
radial distance: 39 mm
material: $X/X_0 = 1.14\%$
pitch: $50 \times 425\ \mu m^2$

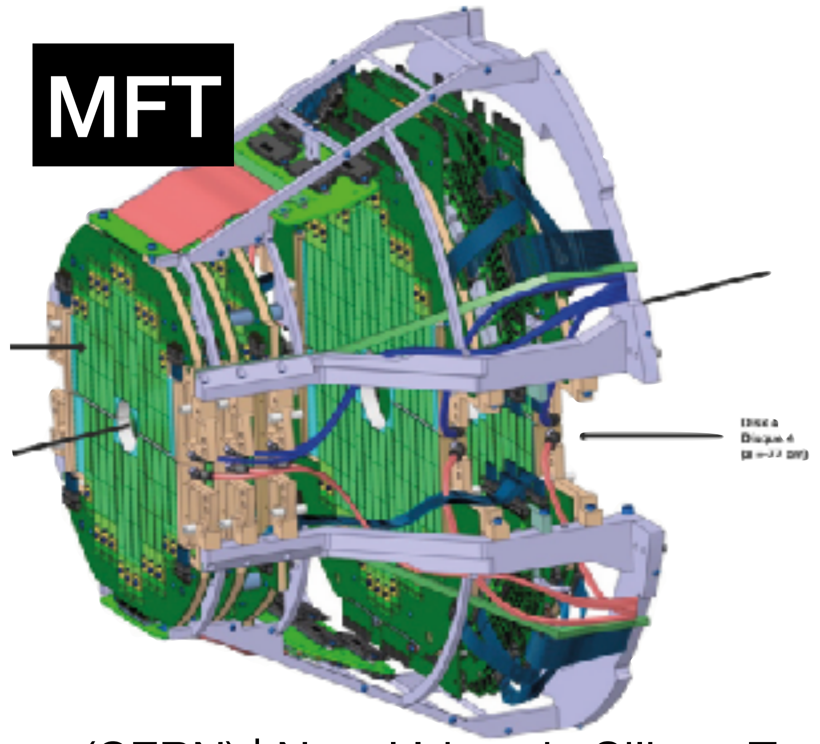
**rate capability:** 1 kHz

**7 layers:**
all MAPS

**Inner-most layer:**
radial distance: 23 mm
material: $X/X_0 = 0.3\%$
pitch: $O(30 \times 30\ \mu m^2)$

**rate capability:** 100 kHz (Pb-Pb)

### Muon Forward Tracker

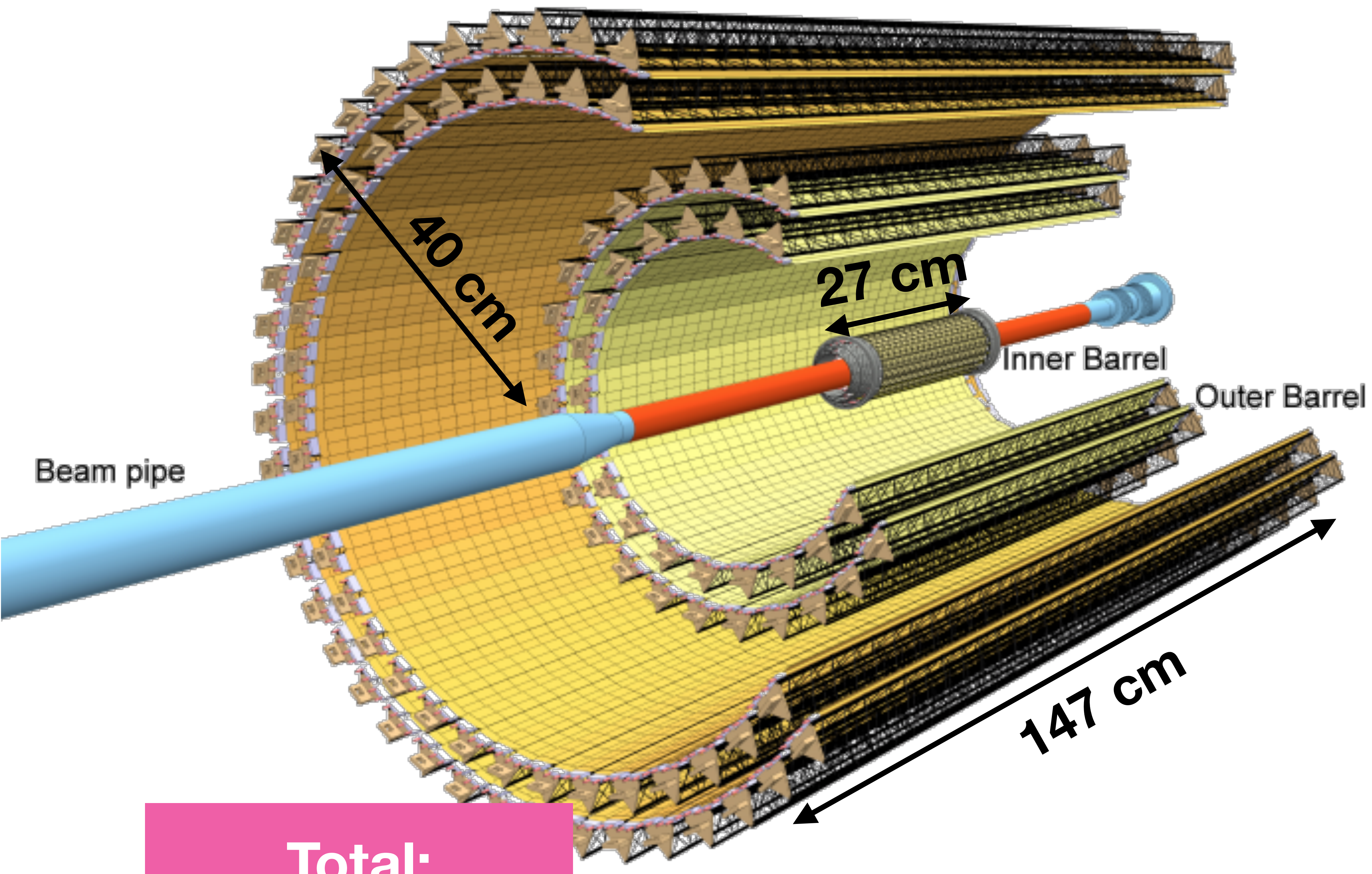



**new detector**

**5 discs, double sided:**
based on same technology as ITS

# ITS2
## Overview of the detector

Layout



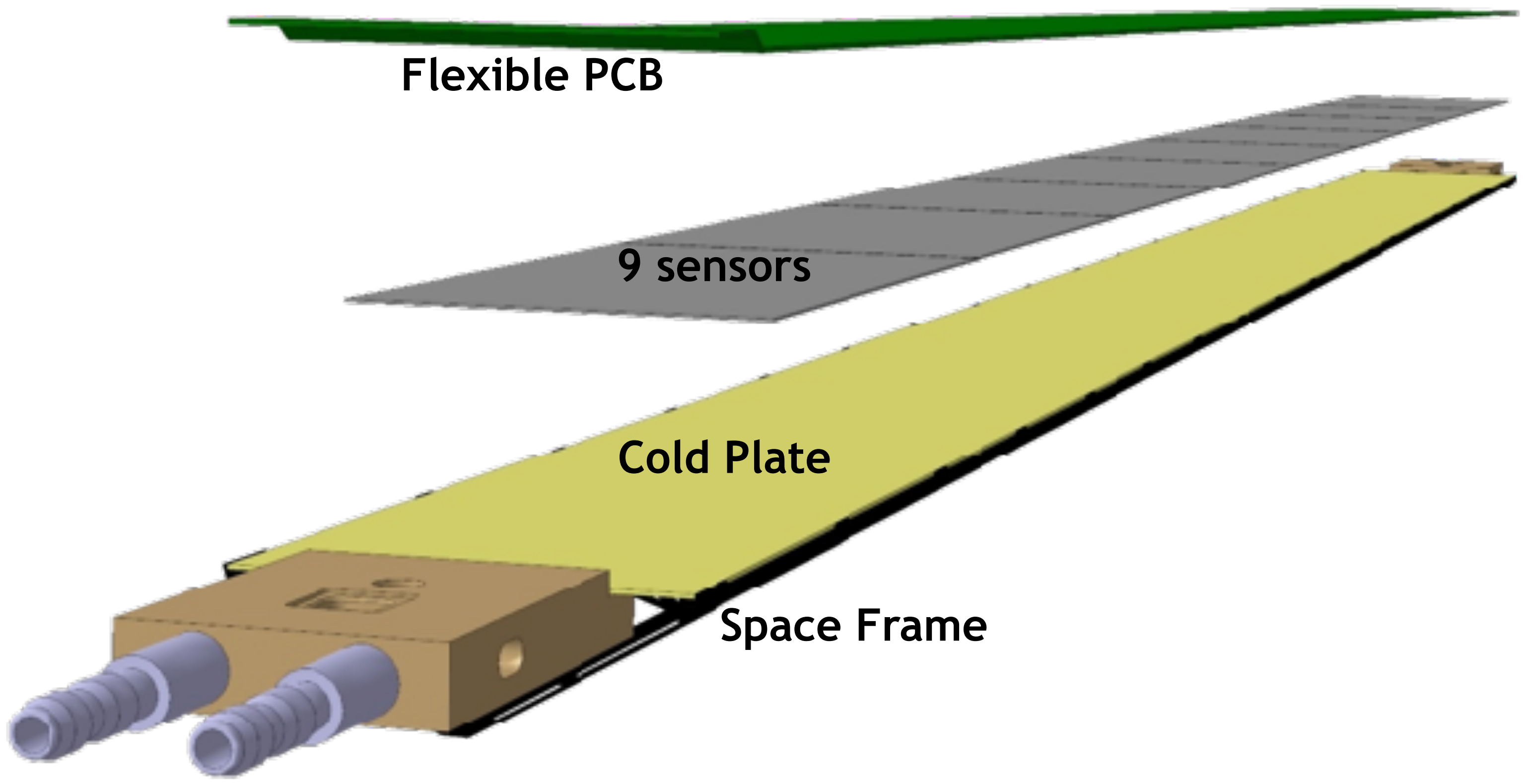

**Total:**
- 24k chips
- 10 m²
- 12.5 GPixel

### Inner Barrel (IB)

**3 Inner Layers: 12+16+20 Staves**
**1 Module / Stave**

**9 sensors per Module**

**96 Modules to be produced**
**(2 Inner Barrels + spares)**

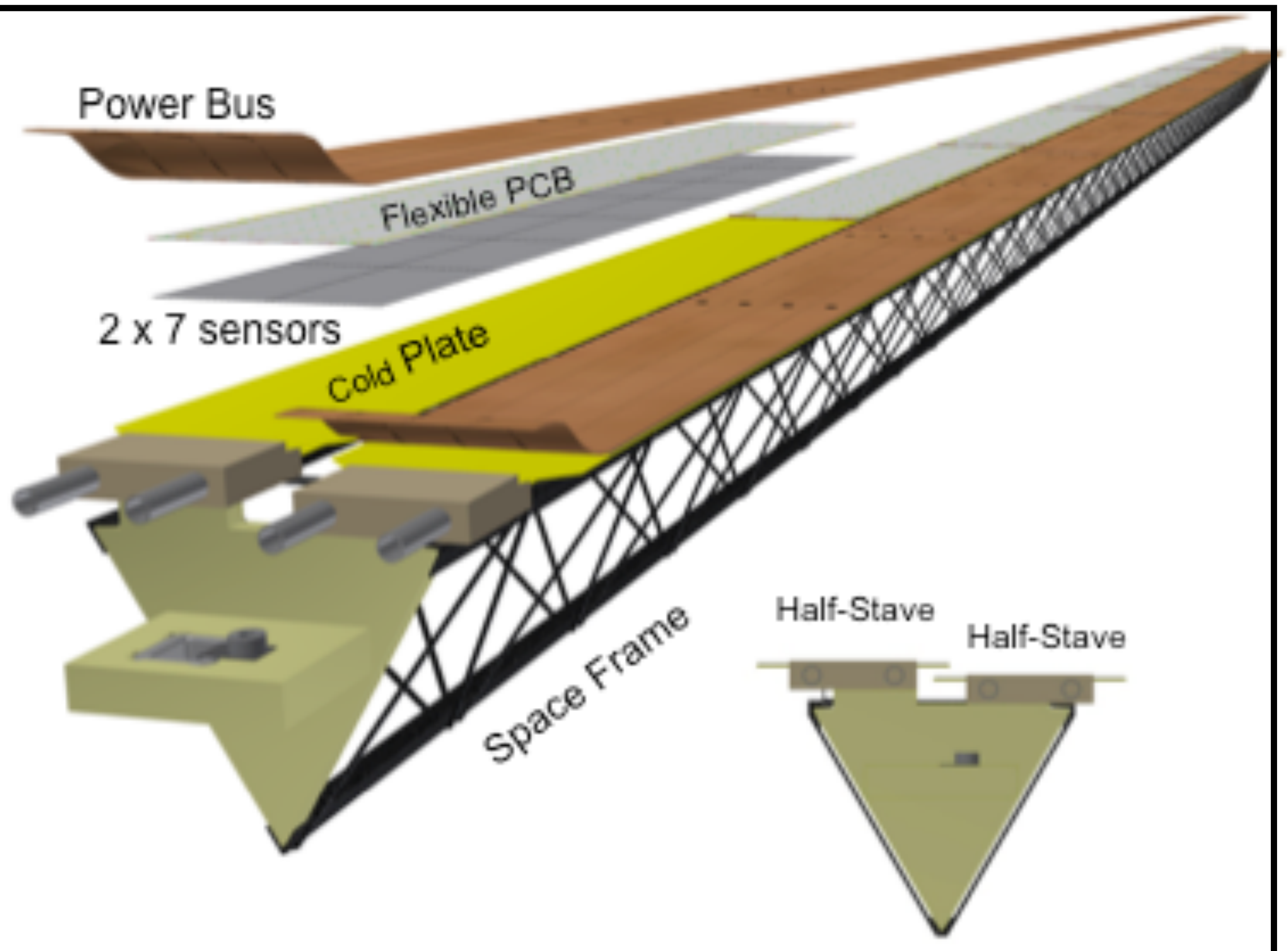



### Outer Barrel (OB)

**2 Middle Layers: 30+24 Staves**
**2×4 Modules / Stave**
**2 Outer Layers: 42+48 Staves**
**2×7 Modules / Stave**

**2×7 sensors / Module**
**(Middle and Outer Layers are equipped with the same Module Type)**

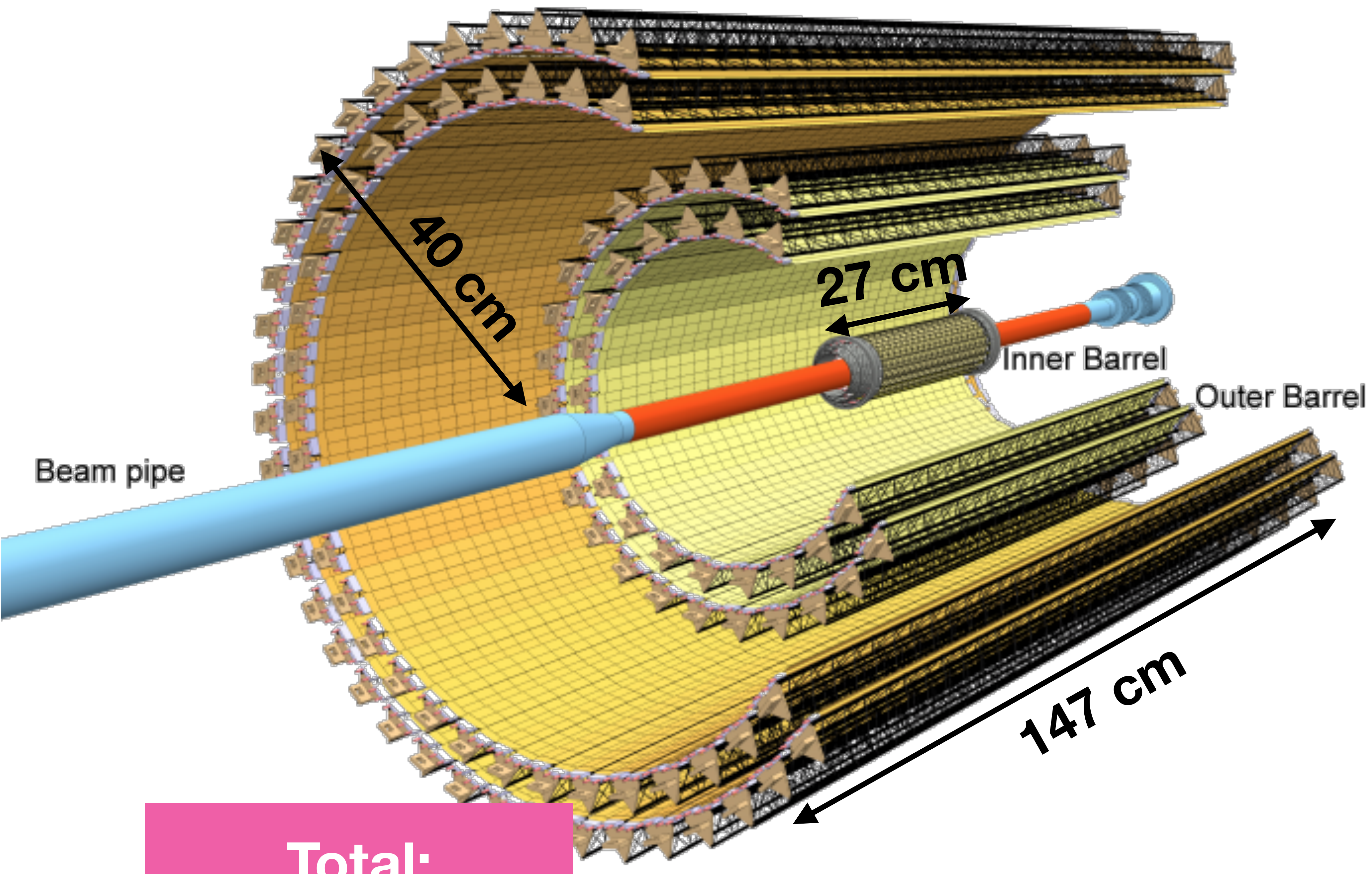
**1880 Modules to be produced**
**(including spares)**



# ITS2

## Overview of the detector

Layout

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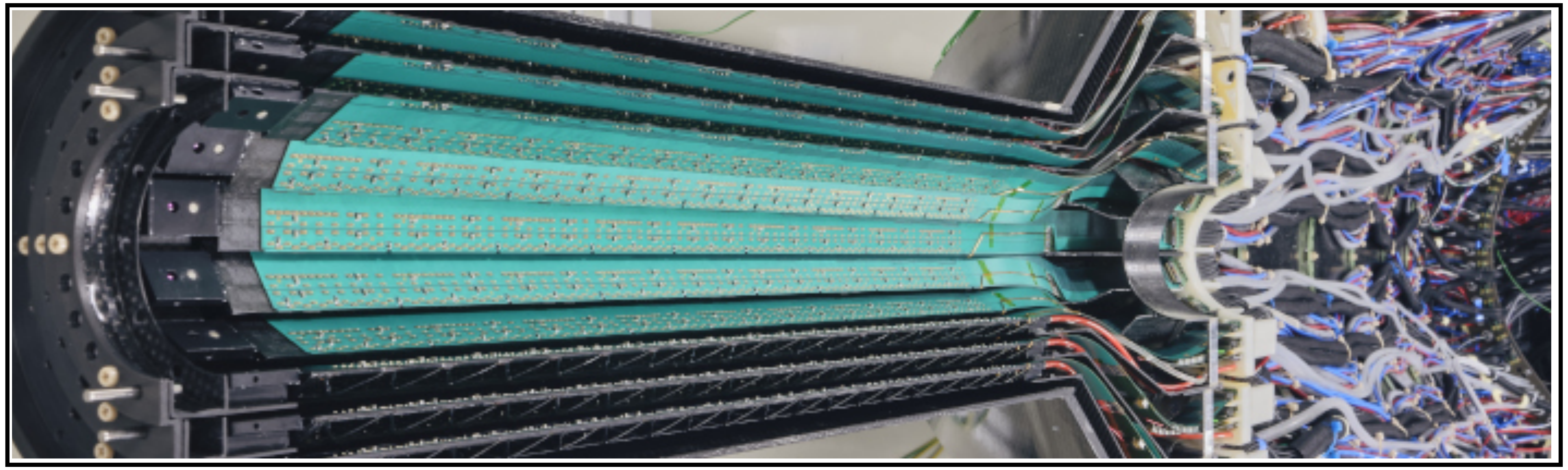
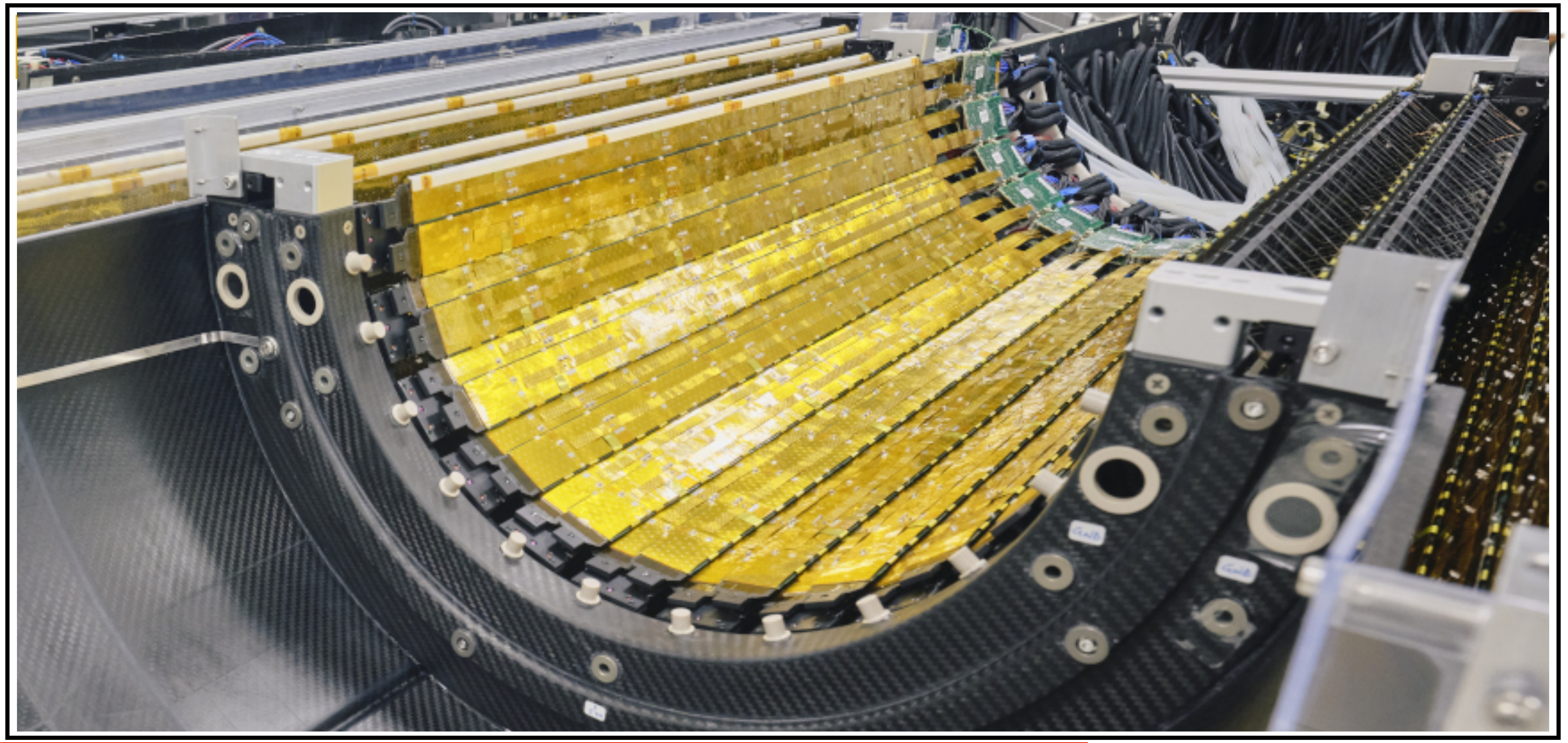
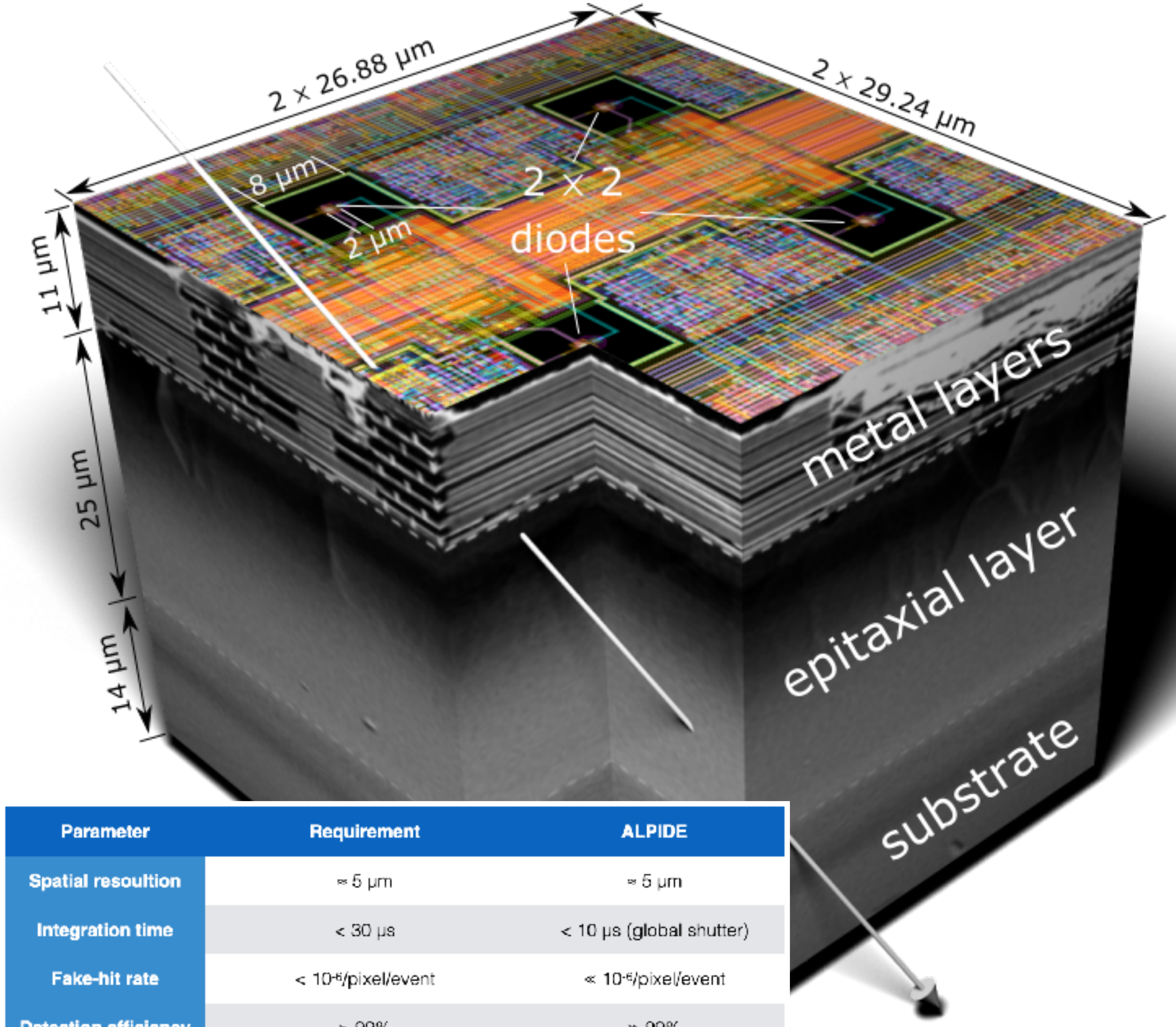




***Good news: it was all built, assembled and tested!***


ALPIDE
524 288 pixels
1.5cm
3cm
AREF

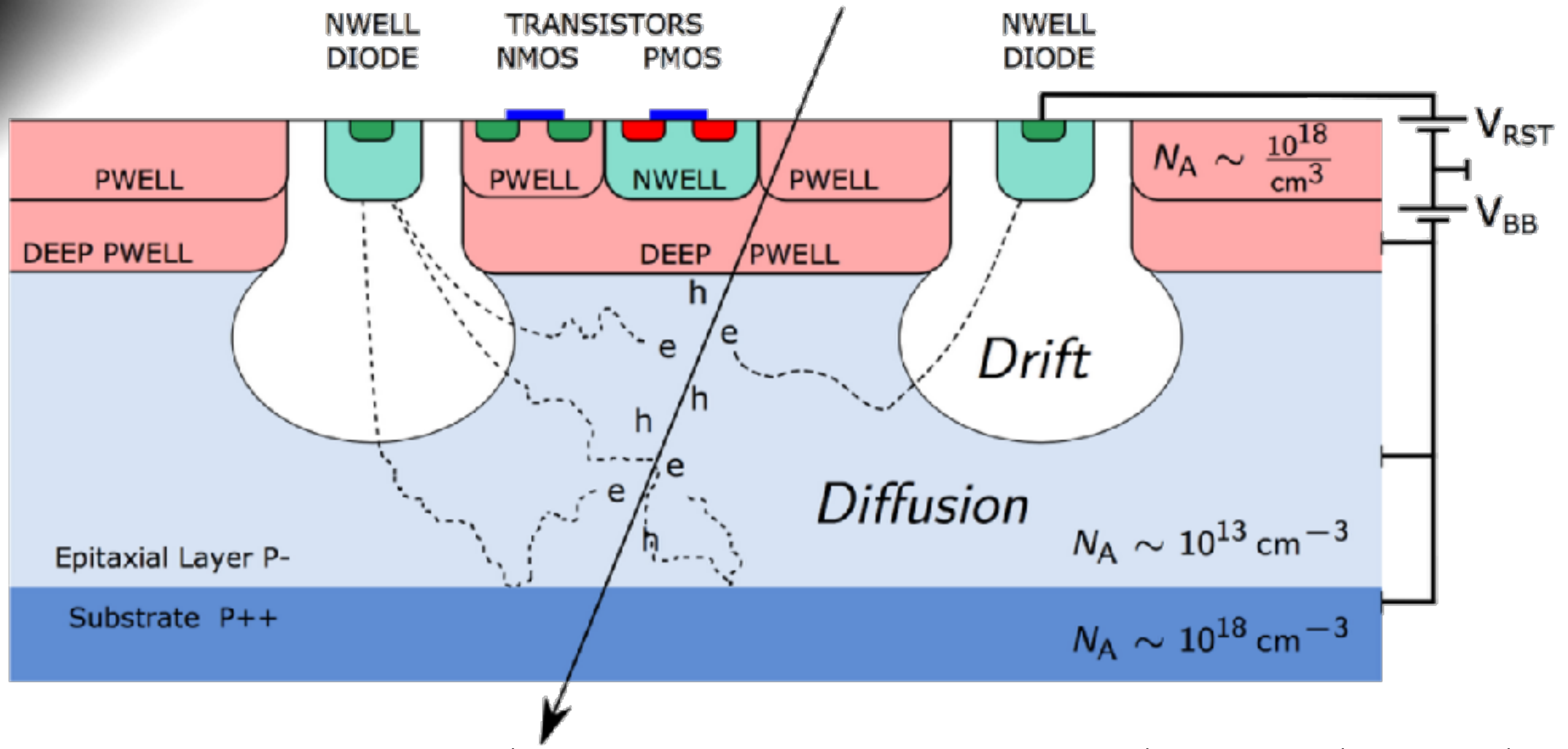
# ALPIDE
## Technology




| Parameter | Requirement | ALPIDE |
|---|---|---|
| Spatial resoultion | ≈ 5 µm | ≈ 5 µm |
| Integration time | < 30 µs | < 10 µs (global shutter) |
| Fake-hit rate | < $10^{-6}$/pixel/event | ≪ $10^{-6}$/pixel/event |
| Detection efficiency | > 99% | ≫ 99% |
| Power consumption | < 100 mW/cm² | < 40 mW/cm² |
| Radiation hardness* | > 2.7 Mrad (IB), 100 krad (OB) (TID) > $1.7 \times 10^{13}$ 1 MeV $n_{eq}$ (NIEL) | OK |

* including safety factor of 10

- **Process:** TowerJazz 180 nm CIS
  - deep p-well to allow CMOS circuitry inside matrix
  - reverse-substrate bias
- **Detection layer:** 25 µm high-resistive (>1 kΩcm) epitaxial layer
- **Thickness:** 100 µm (OB) or 50 µm (IB)

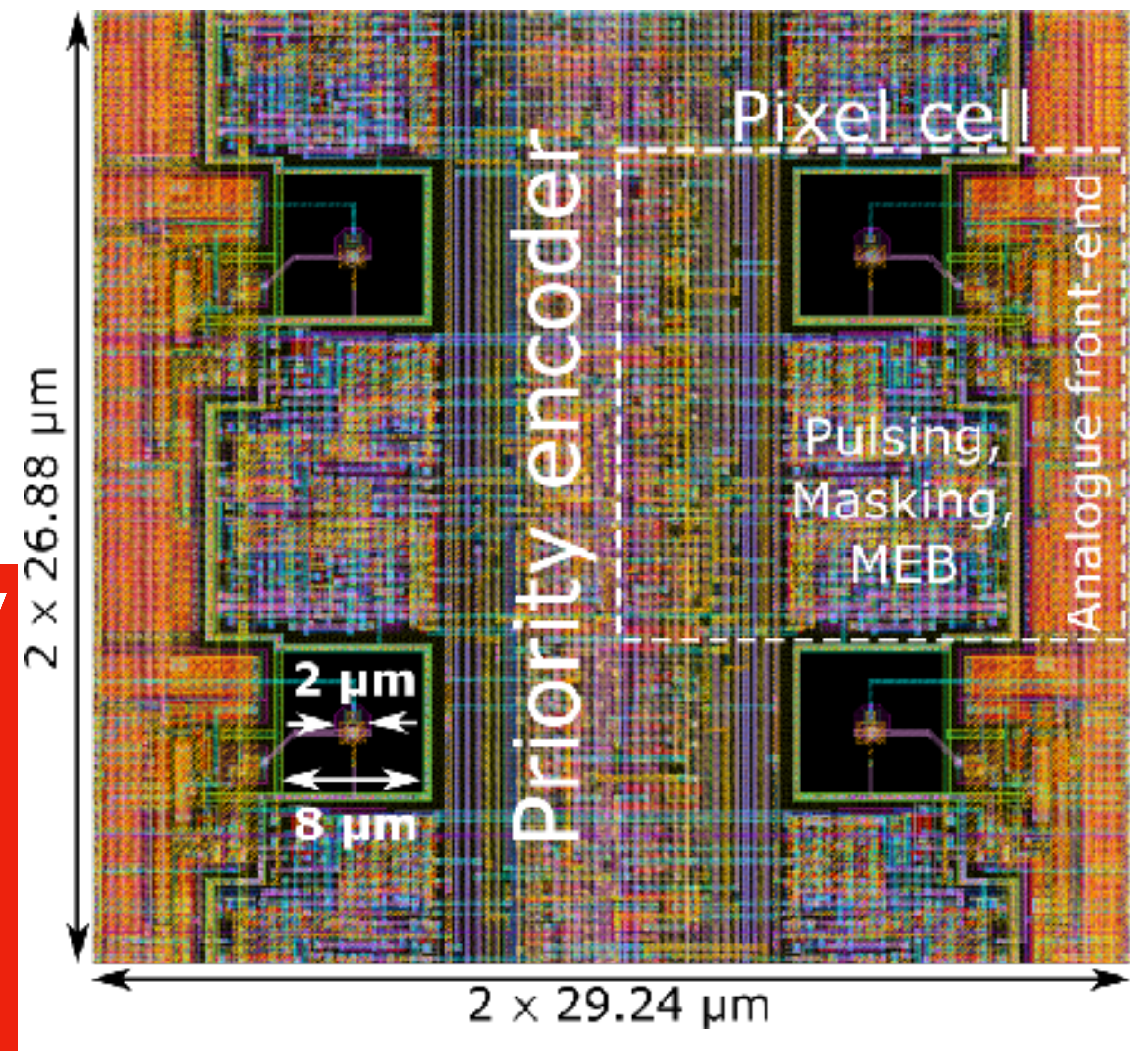


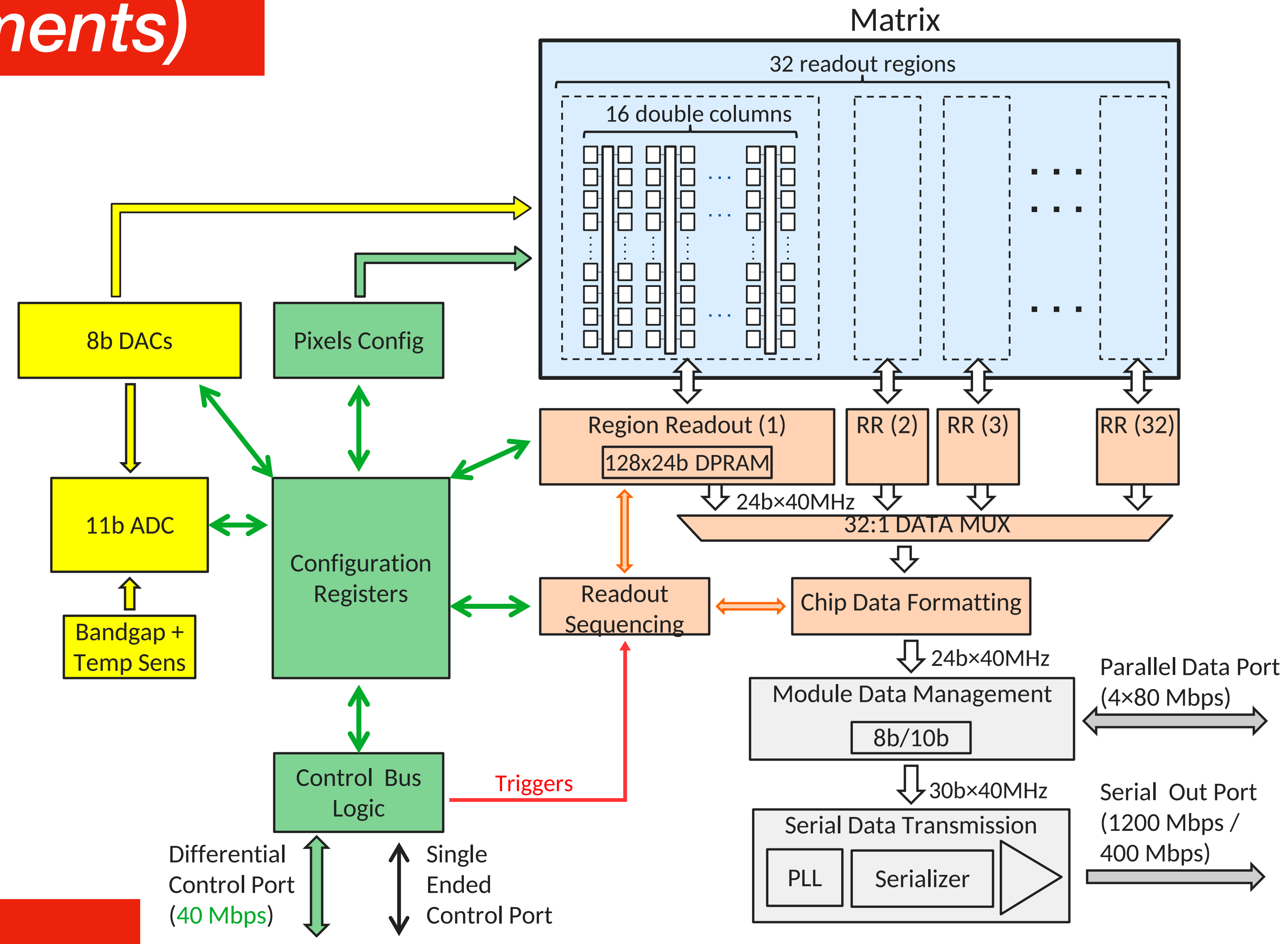
# ALPIDE
## functionality

- **In-pixel circuitry**
  - continuously active, low-power (40 nW) front-end
  - 3-level multiple-event memory
  - masking and analog+digital testing circuitry (each pixel)
- **Column readout**
  - priority encoder, asynchronous, hit-driven
- **Periphery**
  - event handling (global shutter)
  - data transmission, directly drives 8 m-long cables

O(200) transistors/ pixel

*(wrt. traditional 3T/4T arrangements)*




**This marks a new level of integration density for MAPS**

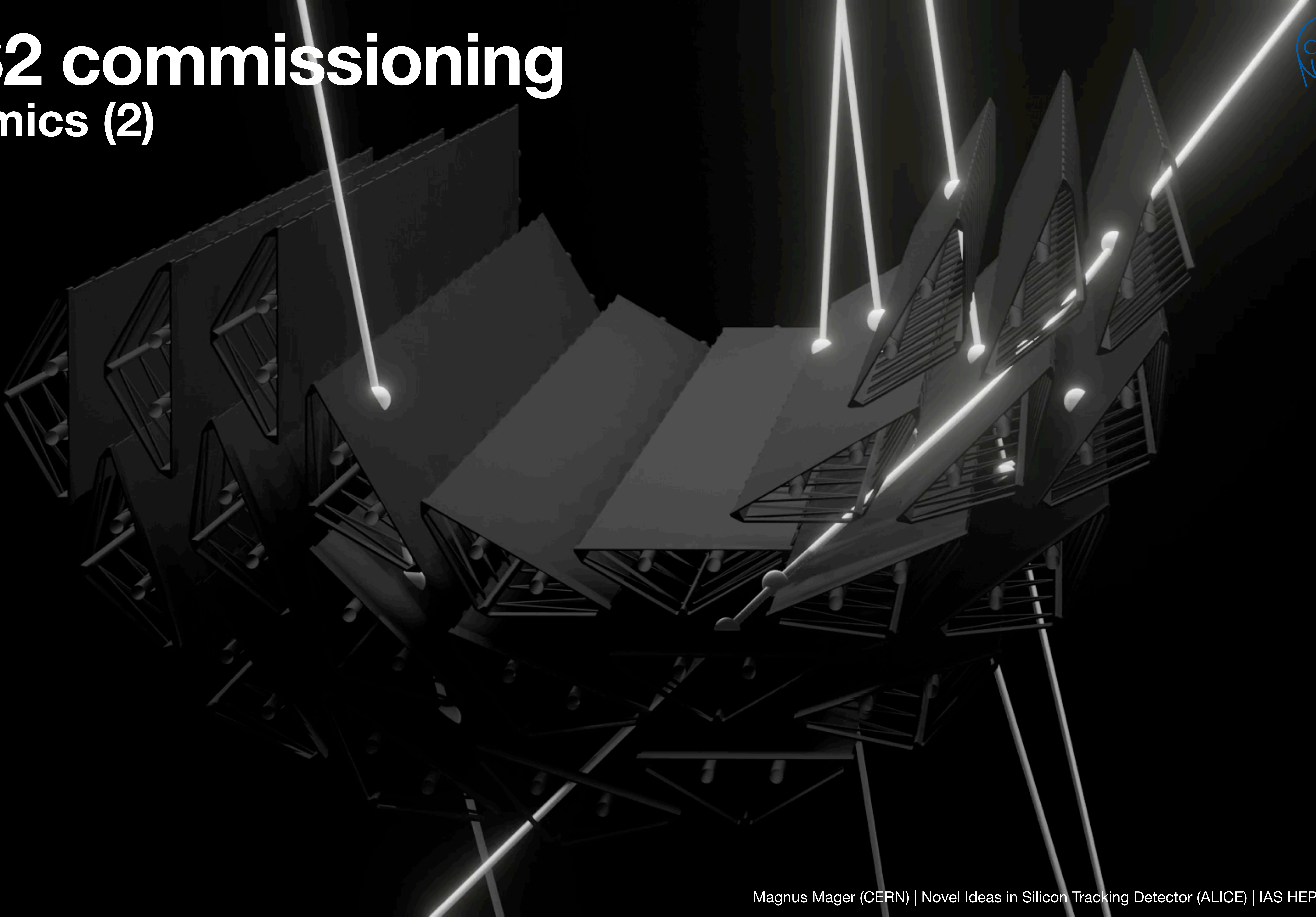
# ITS2 commissioning

# ITS2 commissioning

## Cosmics

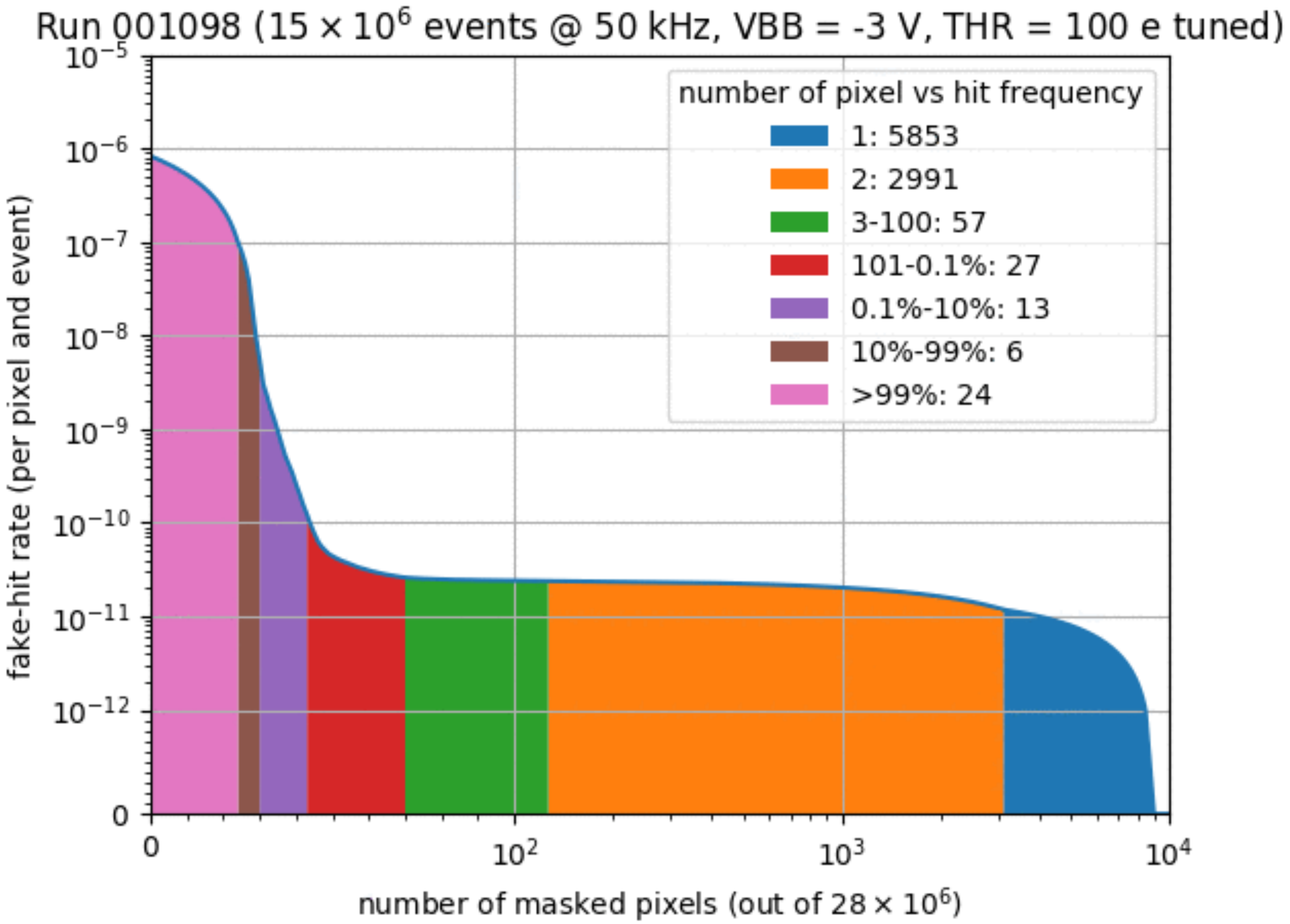

**One layer:**
**one week of data taking**

# ITS2 commissioning
## Cosmics (2)



# ITS2 commissioning
## (No) noise / fake-hit rate

- This is the real rate measured on-detector, including final services
- Essentially, apart from a hand-full pixels per chip, the detector is **noise-free**
- Biggest contributor are cosmic rays (which were *not* excluded here)

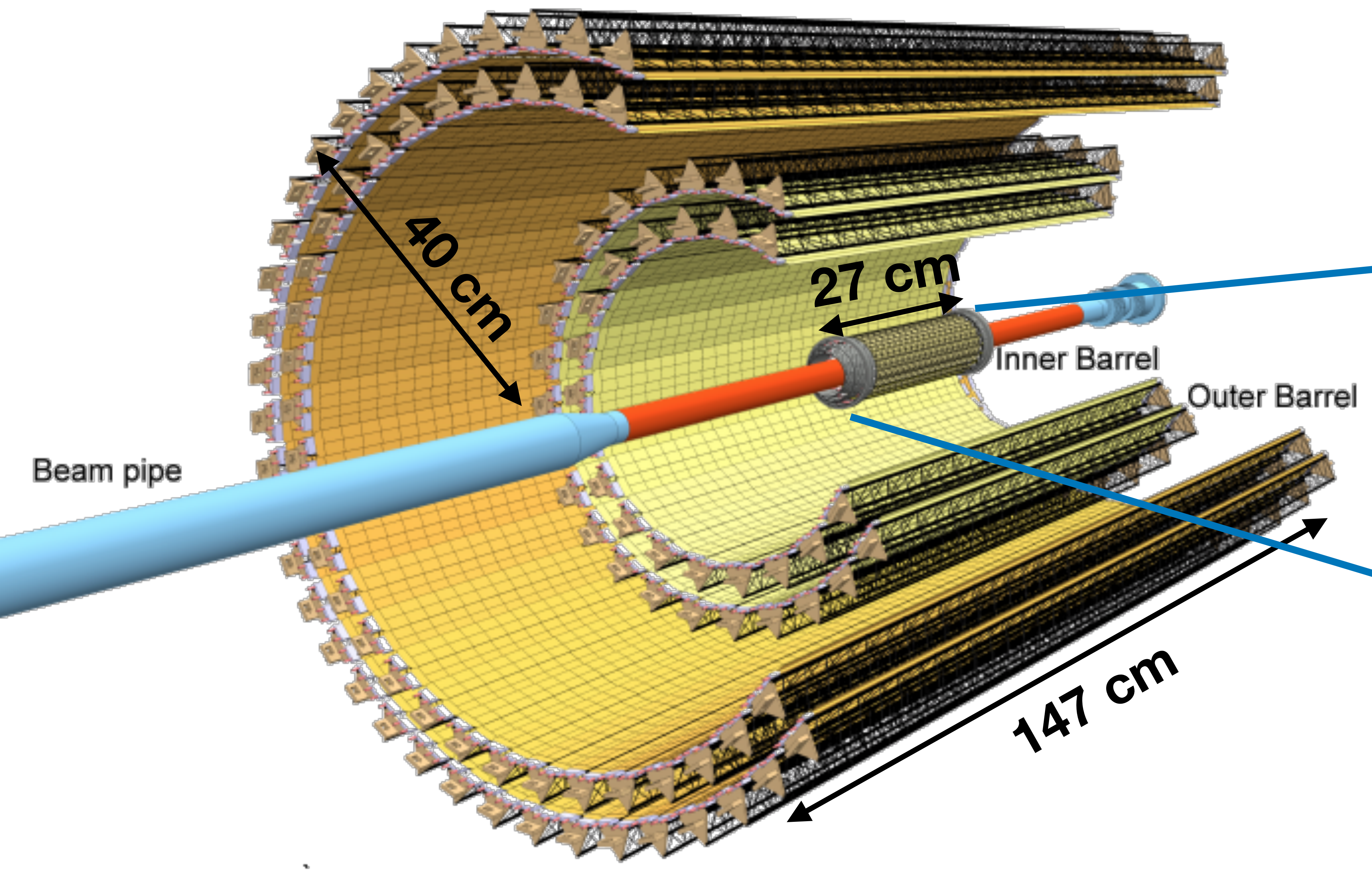



**Excellent on-detector performance! Looking forward to recording collisions!**

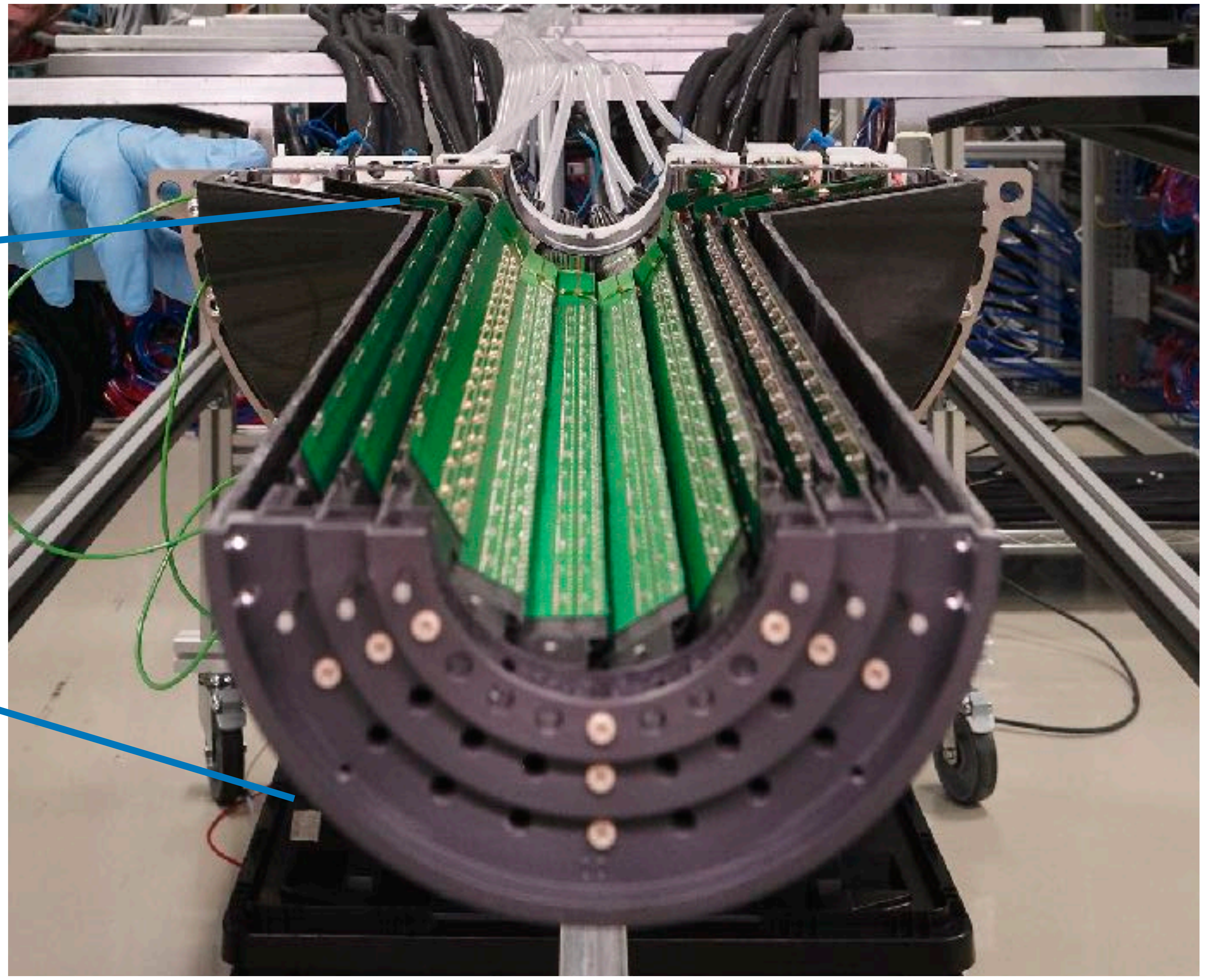
# ITS3 — the golden detector

# ITS2 inner barrel

ITS2: global layout

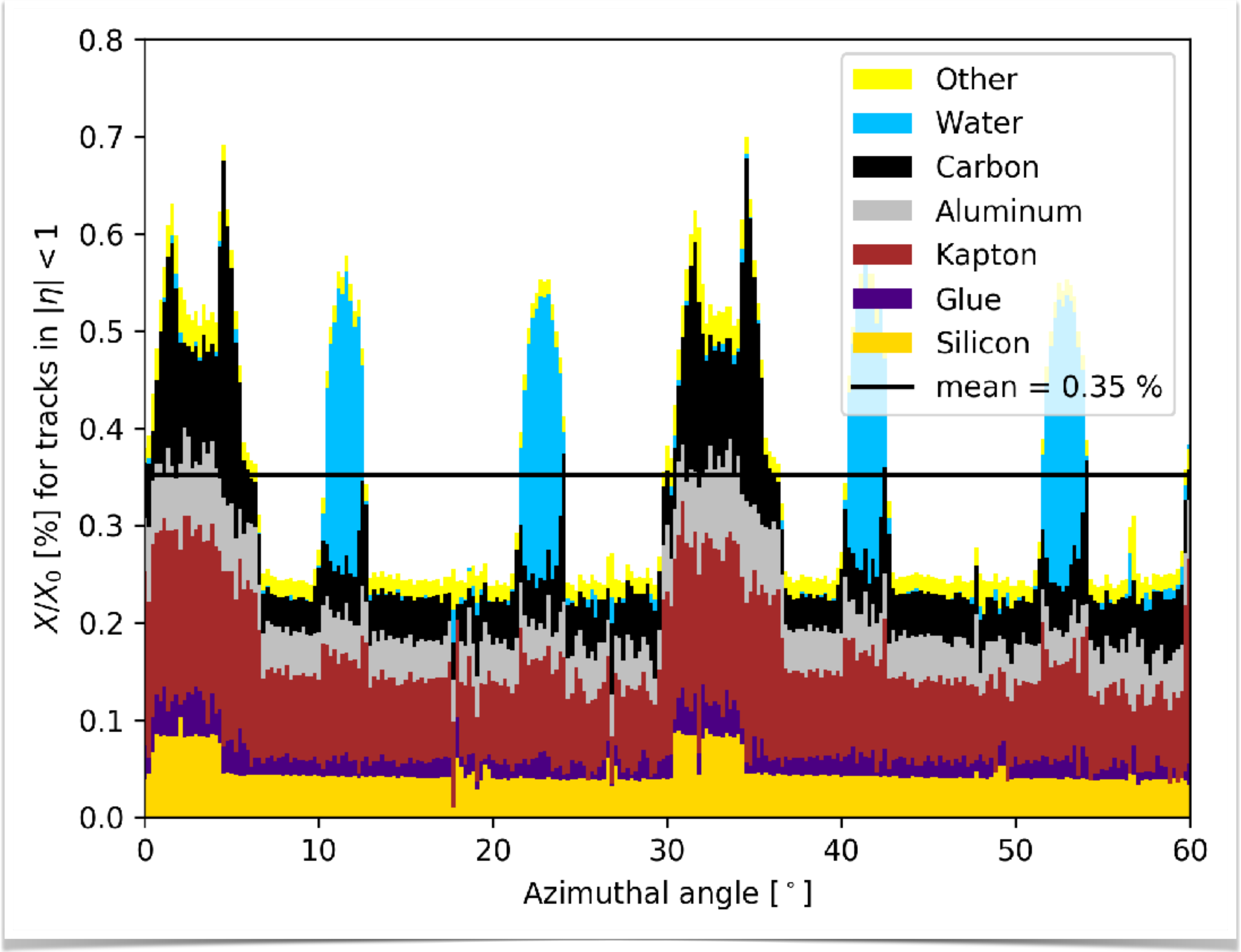



ITS2: assembled three inner-most half-layers



- ITS2 will already have unprecedented performance
- The Inner Barrel is ultra-light but rather packed → further improvements seem possible
- **Key questions: Can we get closer to the IP? Can we reduce the material further?**

# Motivation for ITS3




- Observations:
  - Si makes only **1/7th** of total material
  - **irregularities** due to support/ cooling

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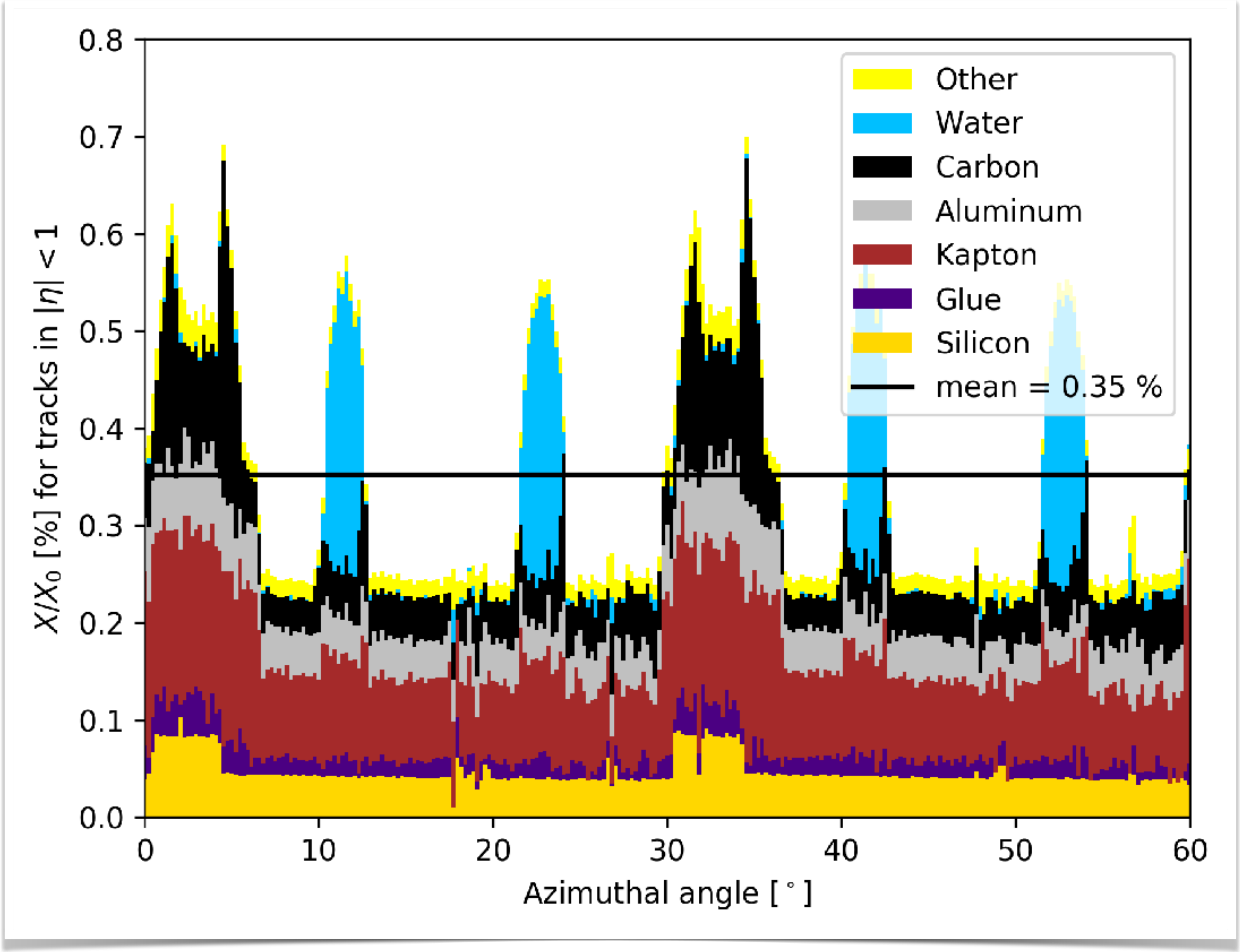


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- Removal of water cooling
  - **possible** if power consumption stays below 20 mW/cm$^2$

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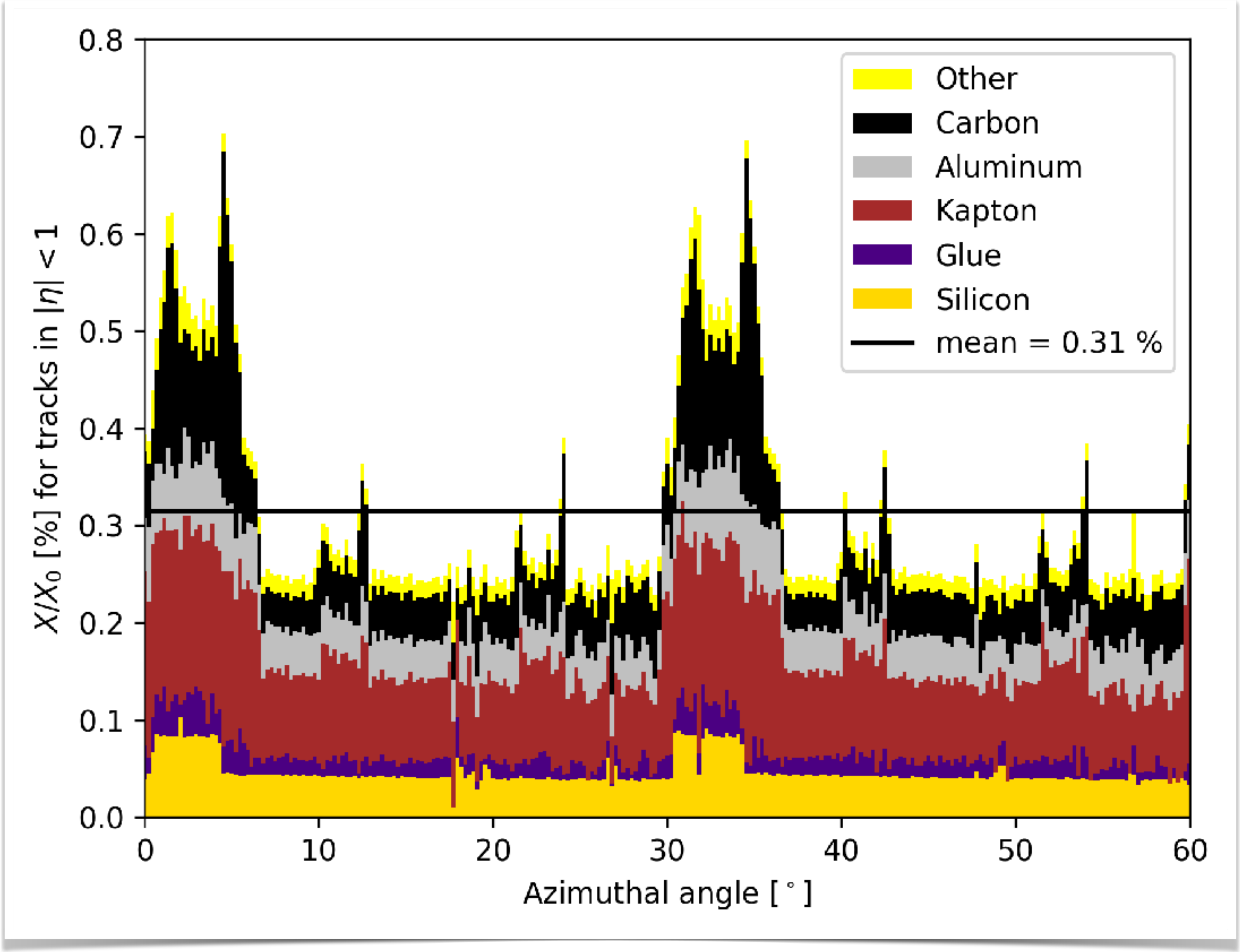


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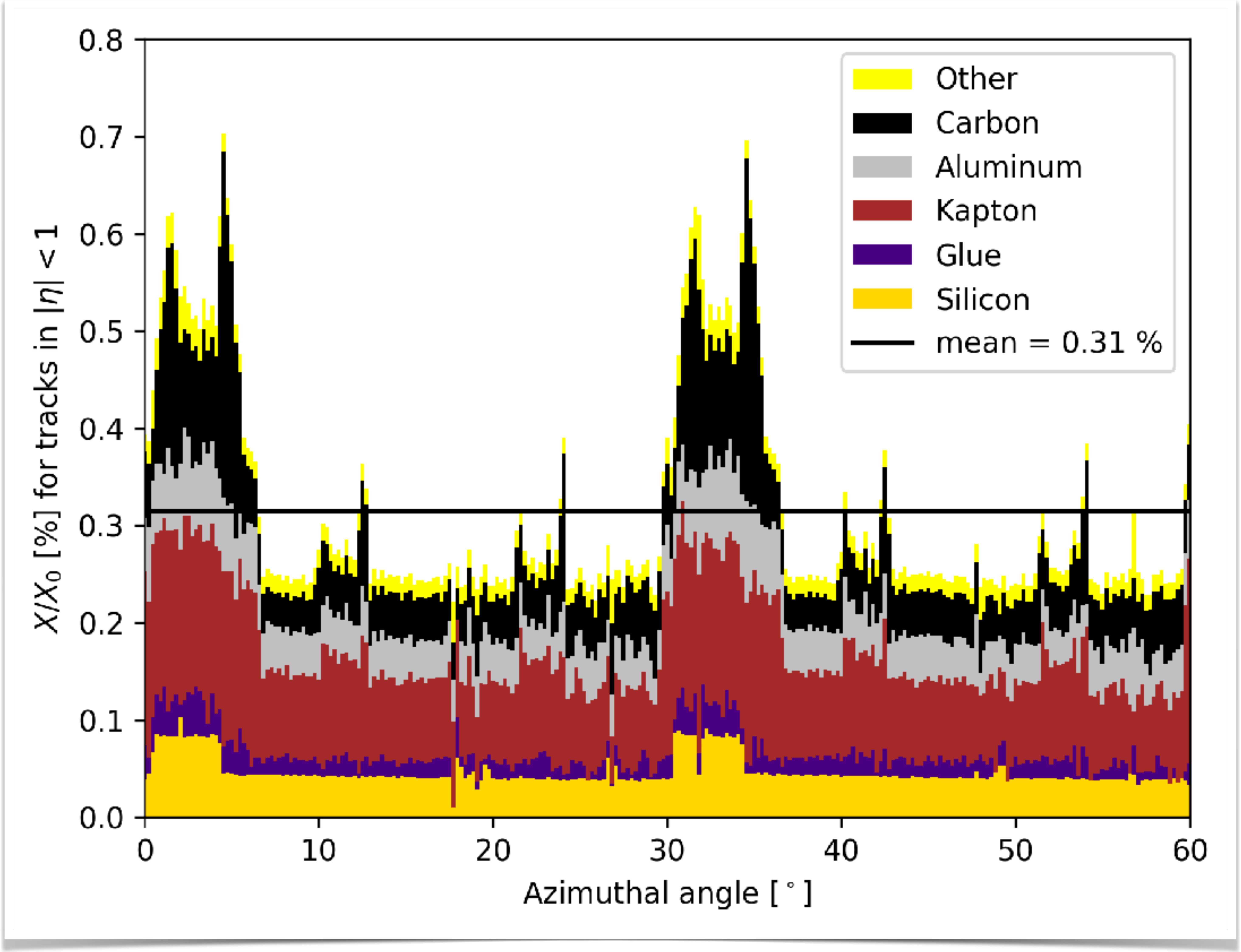


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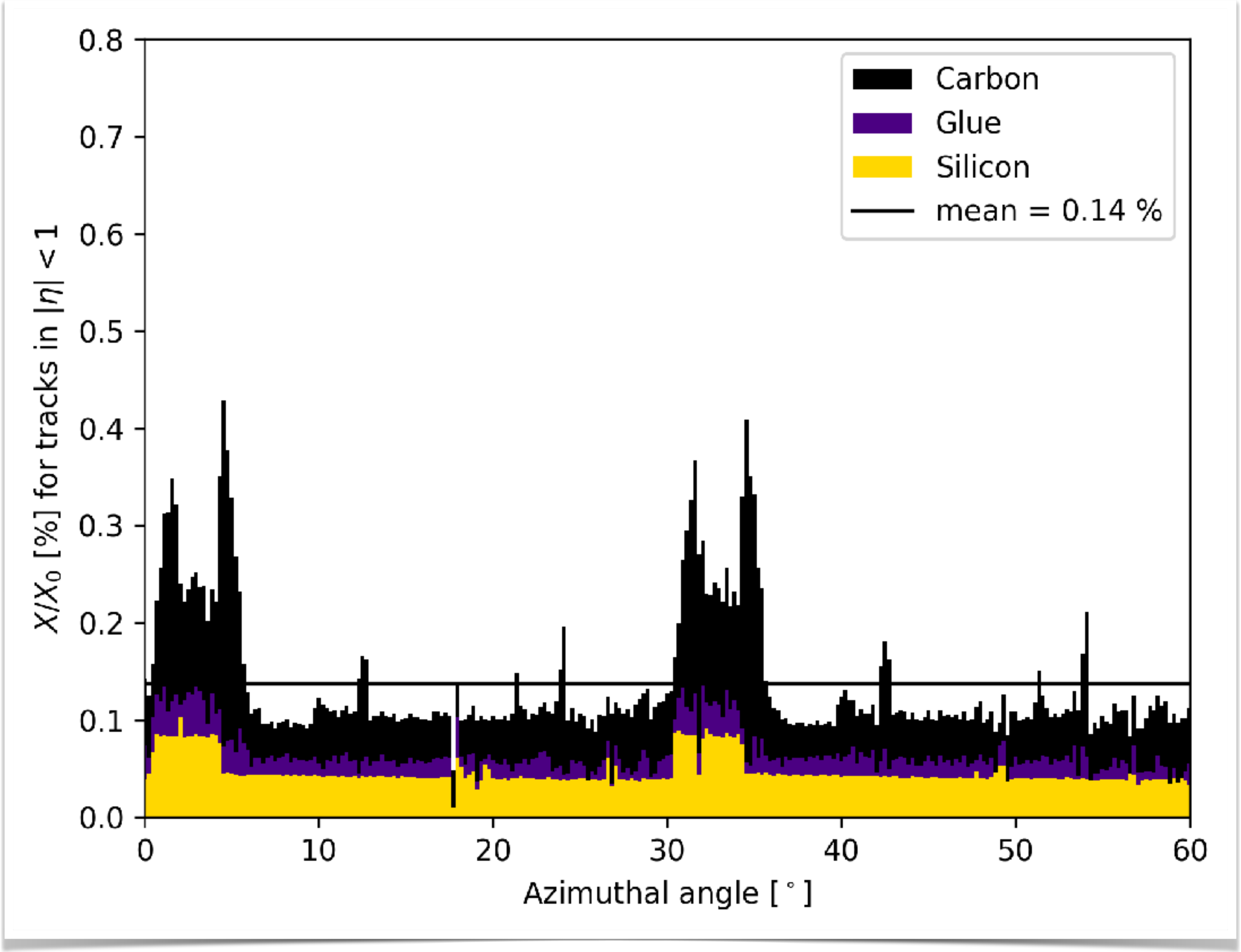


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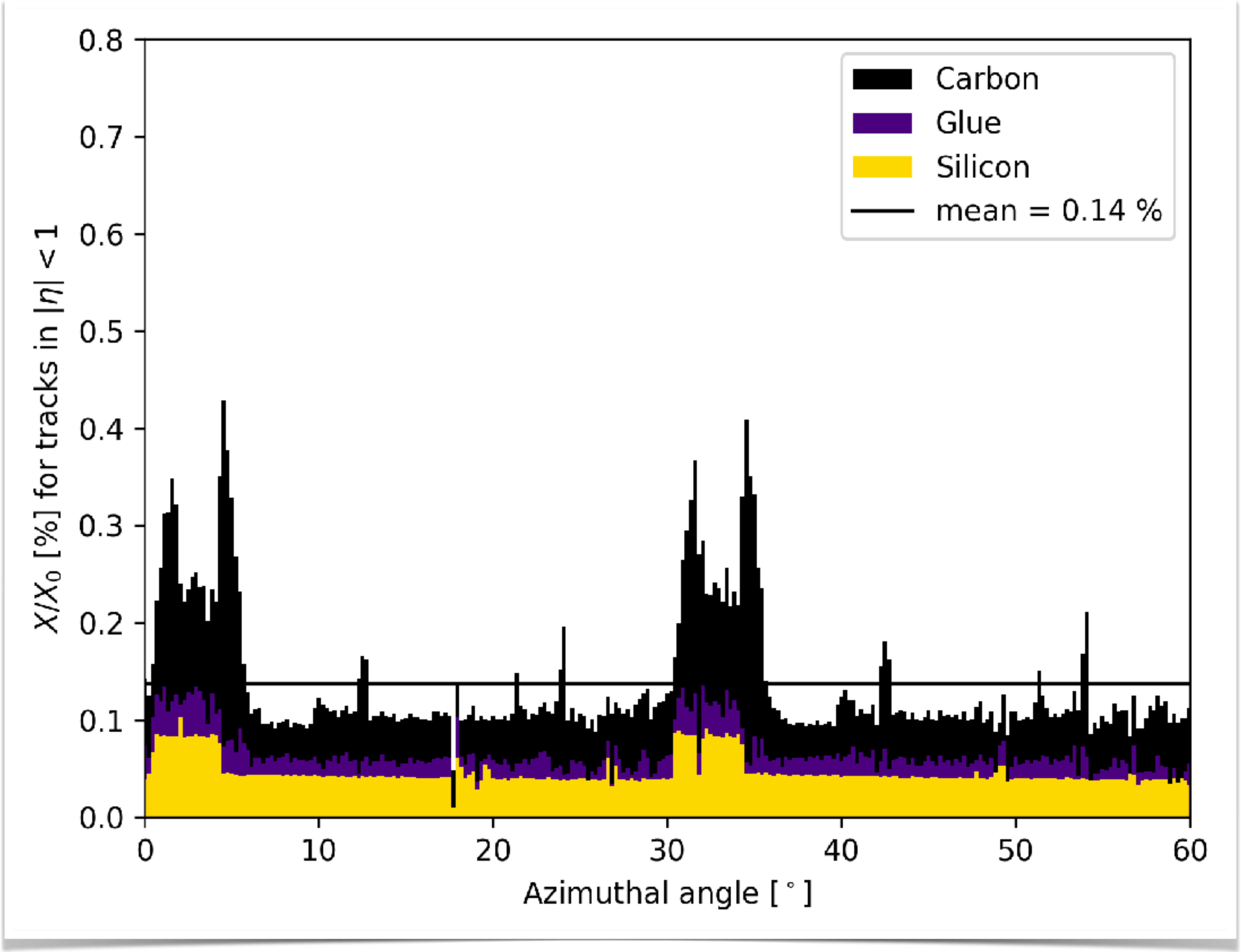


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- Removal of mechanical support
  - **benefit** from increased stiffness by rolling Si wafers

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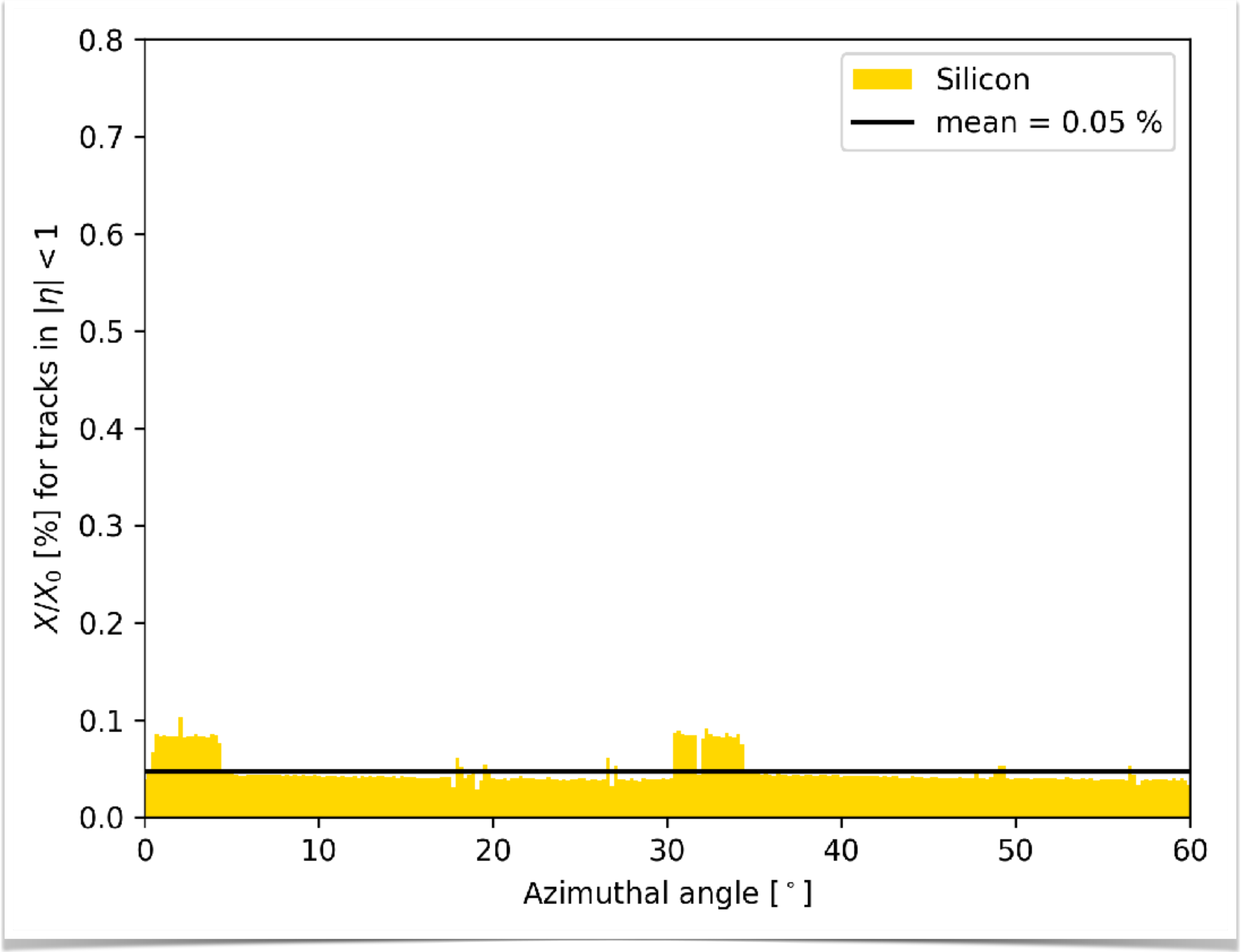


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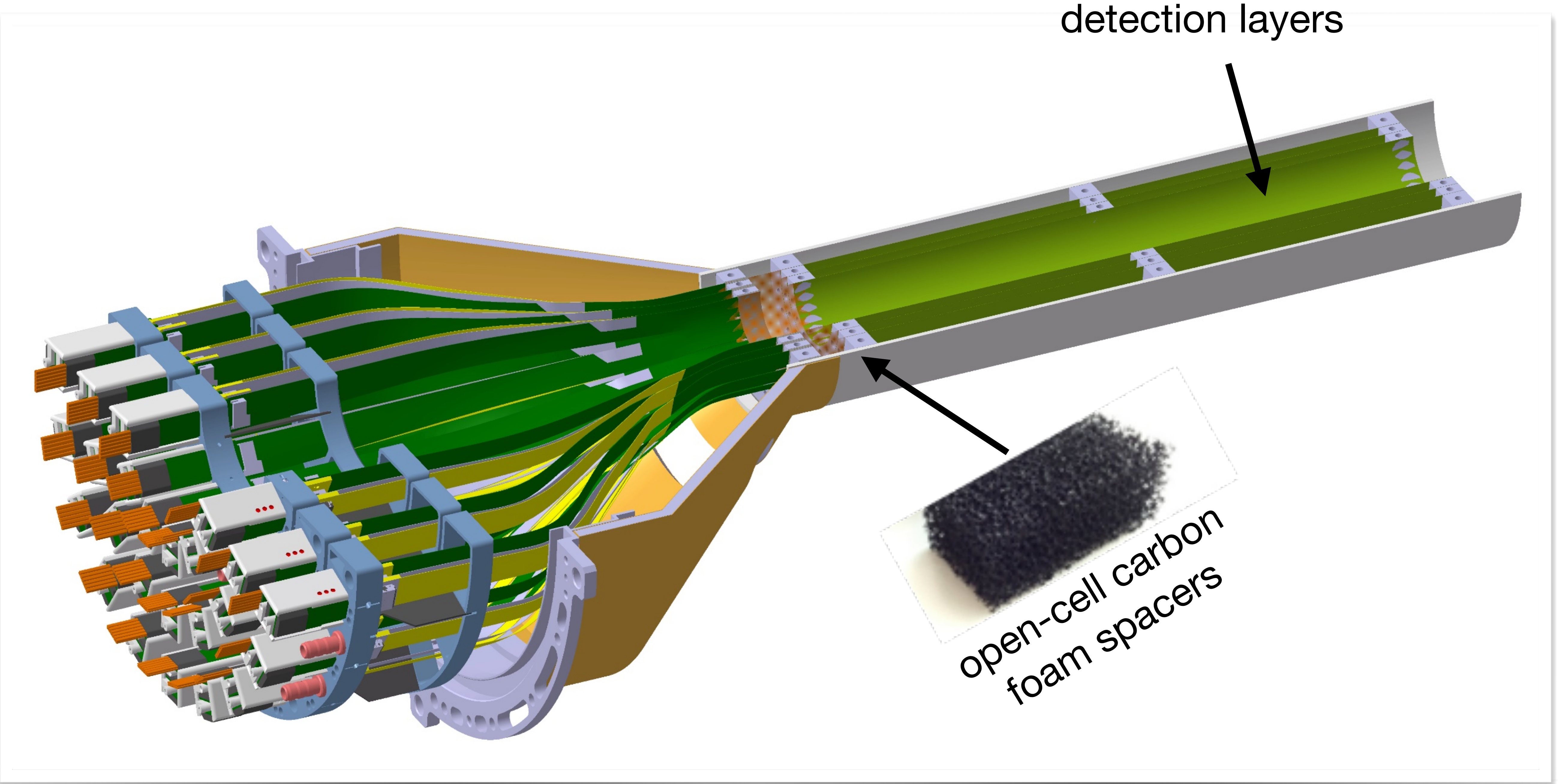
# ITS3
## detector concept



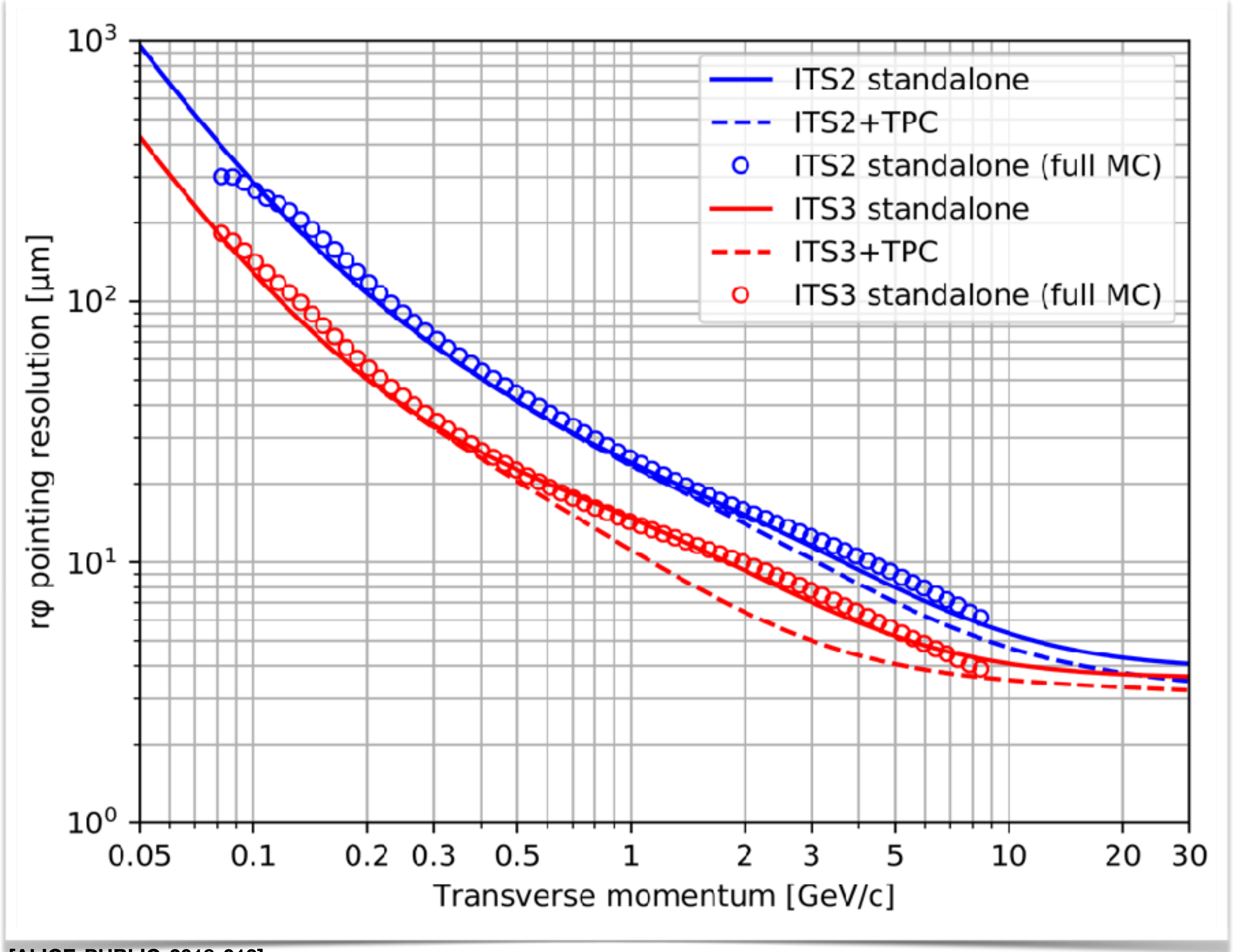

| Beam pipe Inner/Outer Radius (mm) | 16.0/16.5 | | |
|---|---|---|---|
| IB Layer Parameters | Layer 0 | Layer 1 | Layer 2 |
| Radial position (mm) | 18.0 | 24.0 | 30.0 |
| Length (sensitive area) (mm) | 300 | | |
| Pseudo-rapidity coverage | ±2.5 | ±2.3 | ±2.0 |
| Active area ($cm^2$) | 610 | 816 | 1016 |
| Pixel sensor dimensions ($mm^2$) | 280 x 56.5 | 280 x 75.5 | 280 x 94 |
| Number of sensors per layer | 2 | | |
| Pixel size ($\mu m^2$) | O (10 x 10) | | |

- Key ingredients:
  - 300 mm wafer-scale chips, fabricated using stitching
  - thinned down to 20-40 µm (0.02-0.04% X0), making them flexible
  - bent to the target radii
  - mechanically hold in place by carbon foam ribs
- Key benefits:
  - extremely low material budget: 0.02-0.04% X0 (beampipe: 500 µm Be: 0.14% X0)
  - homogeneous material distribution: essentially zero systematic error from material distribution

**The whole detector will comprise six (!) chips – and barely anything else**

# Performance figures

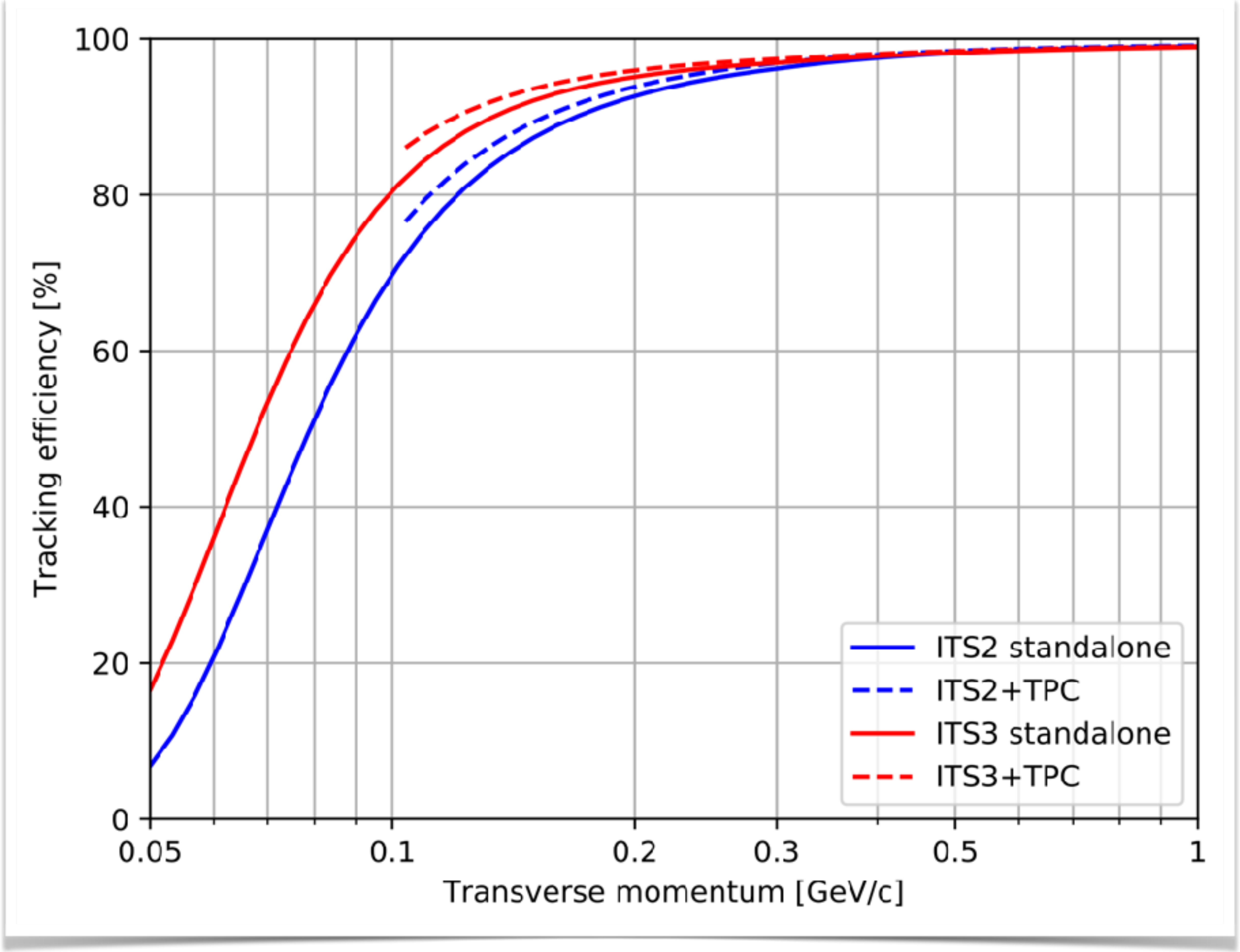
**pointing resolution**




[ALICE-PUBLIC-2018-013]

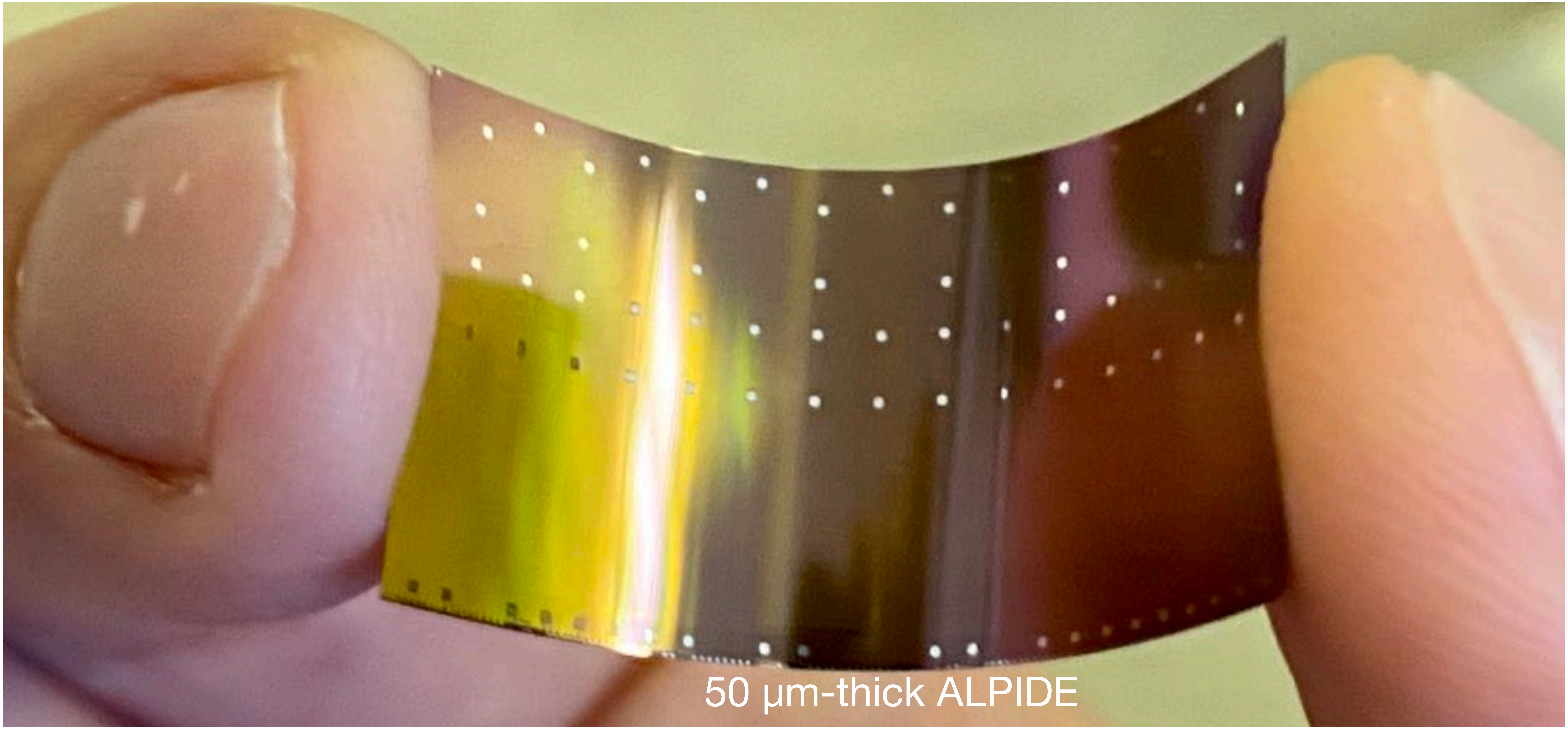
**improvement of factor 2 over all momenta**

**tracking efficiency**

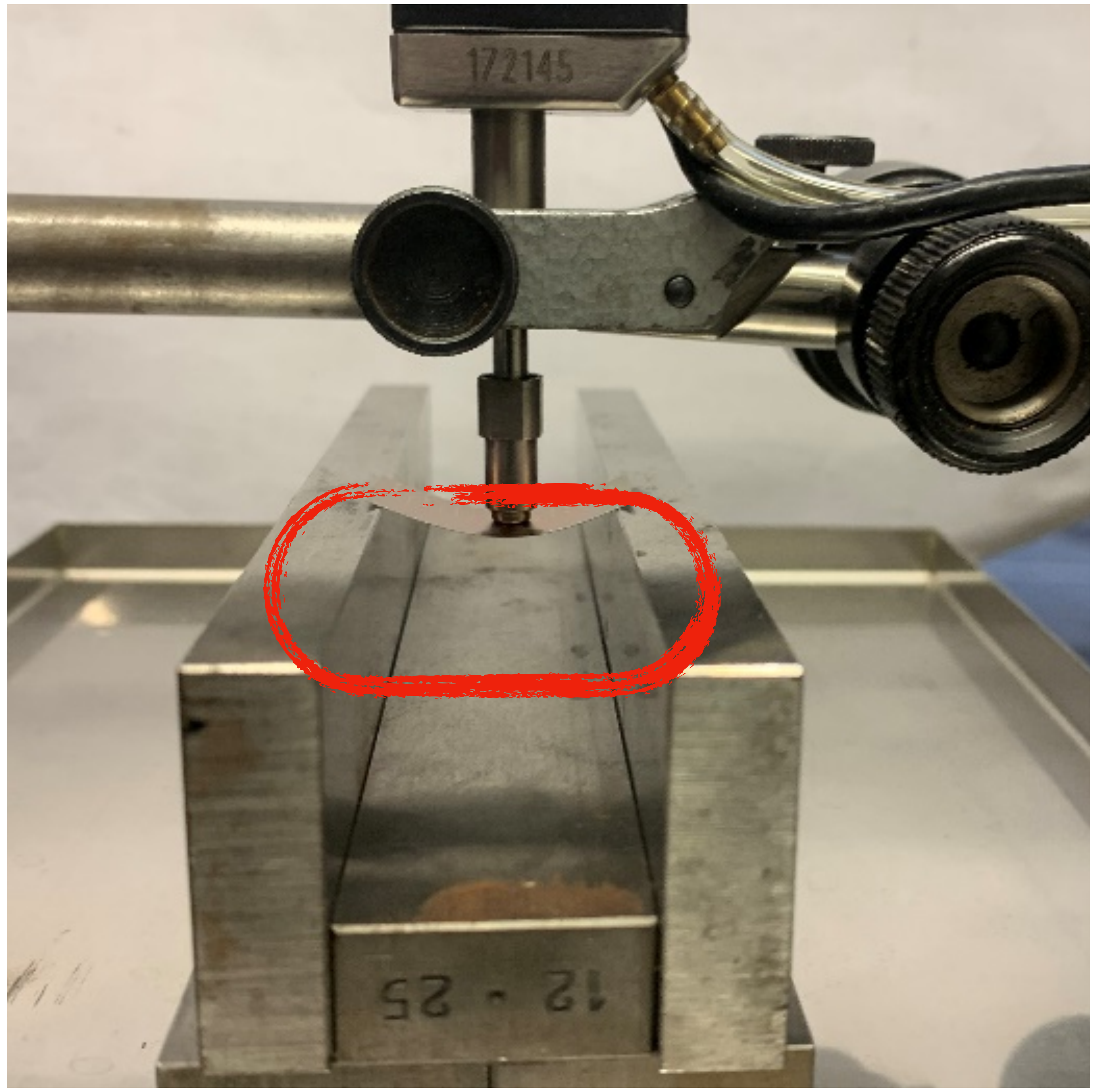


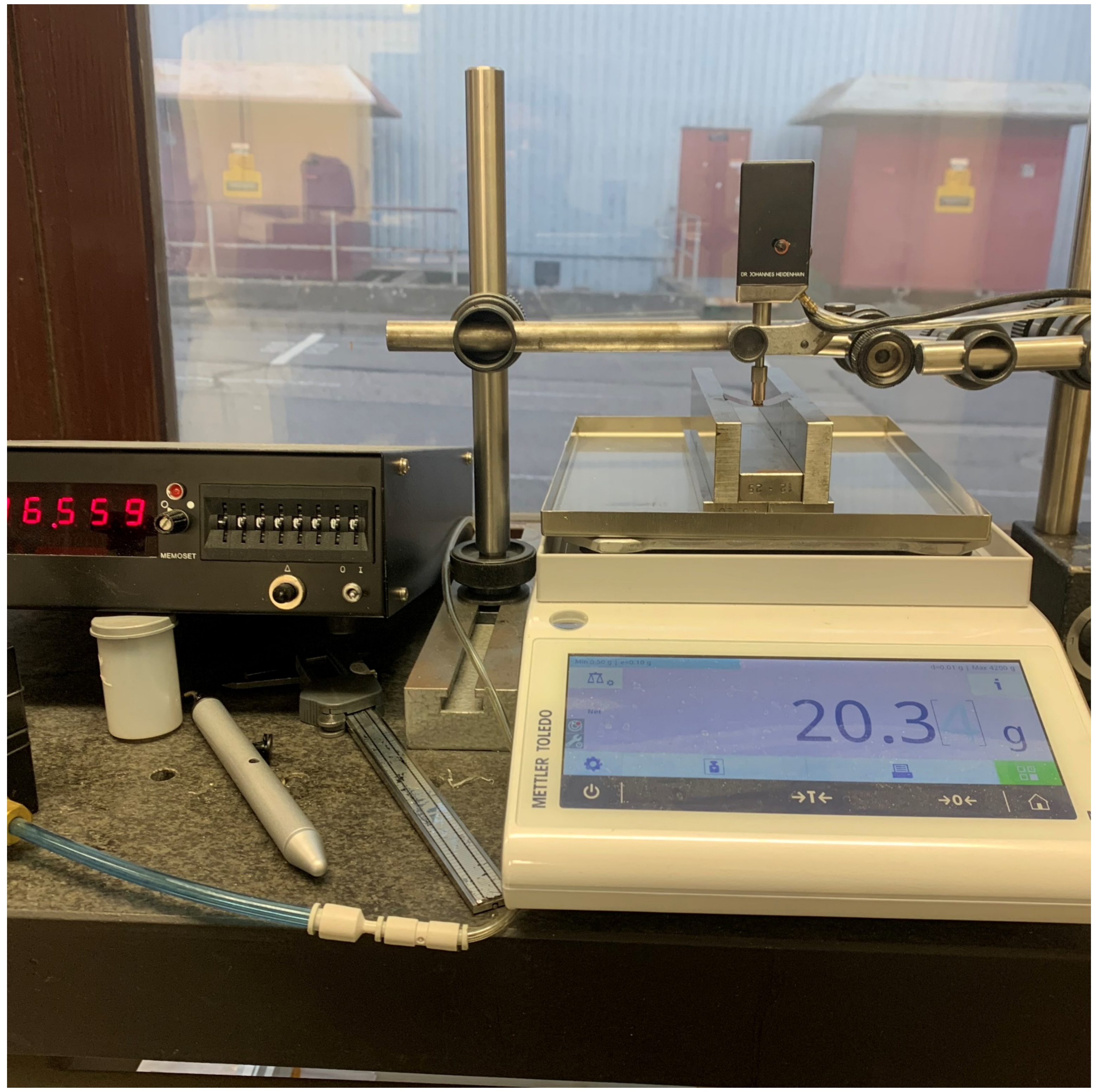

**large improvement for low transverse momenta**

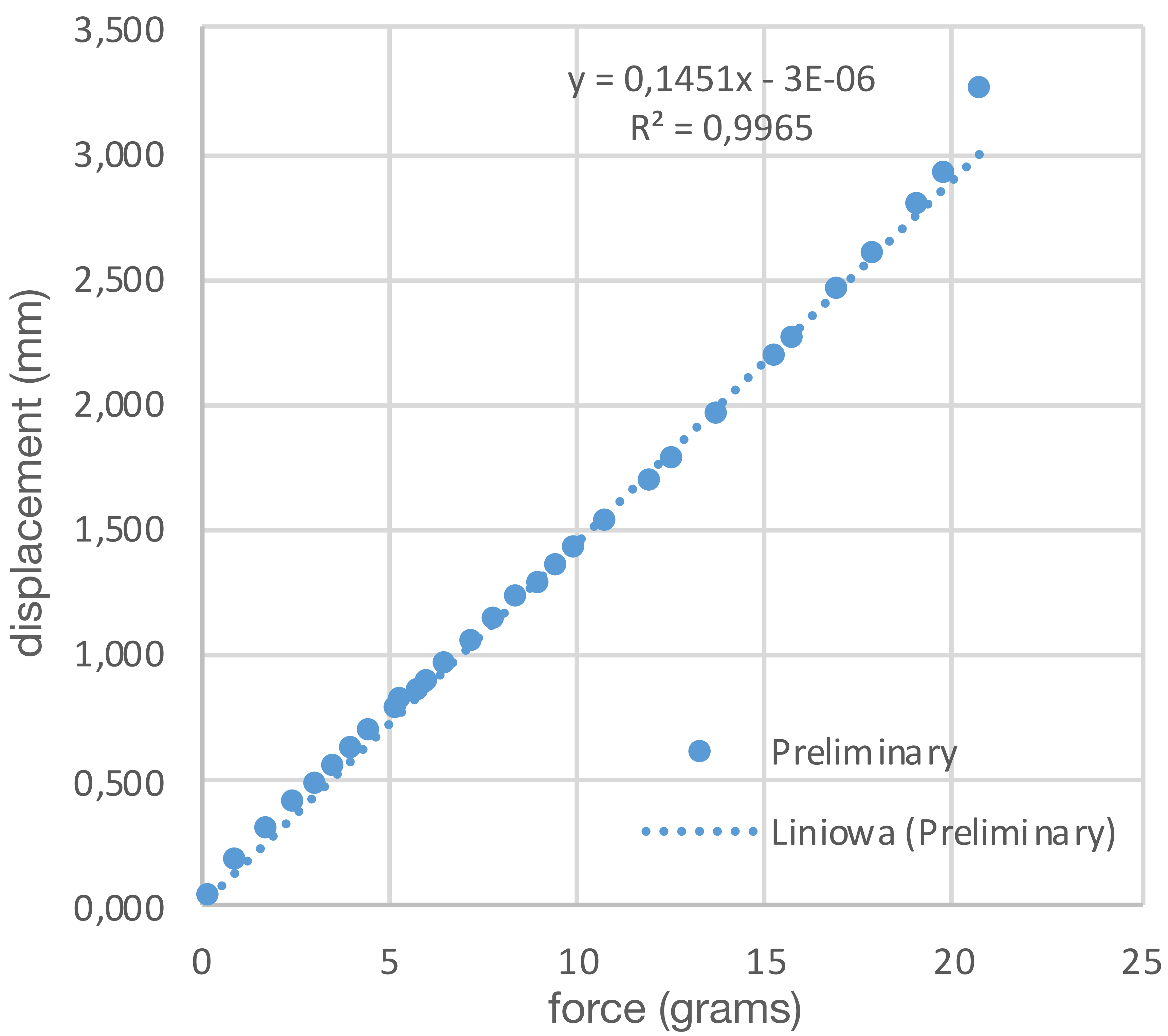
# R&D on bent MAPS



# Bending ALPIDE
*in a scientifically controlled way*



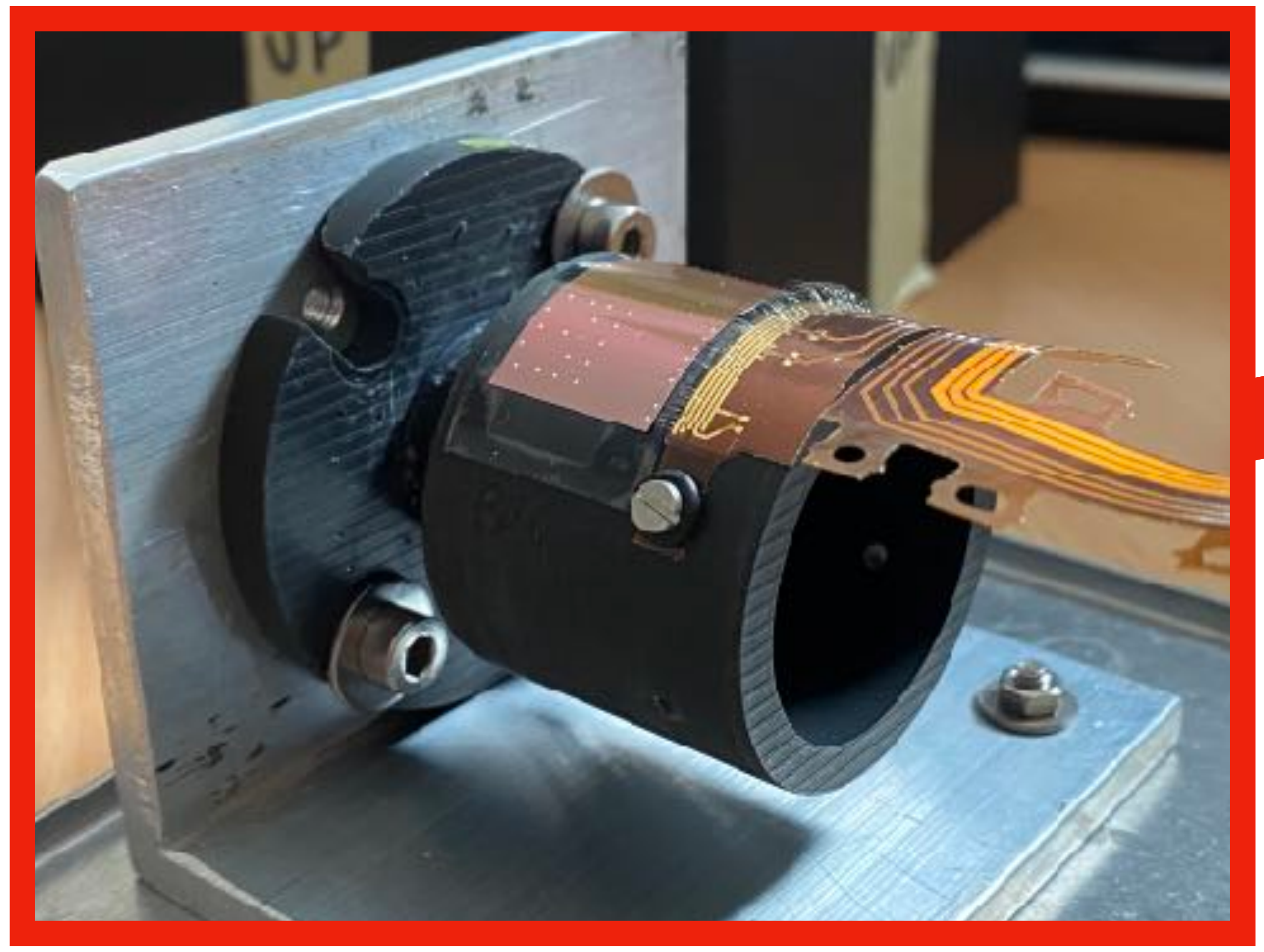

- ALPIDE bends pretty much according to text book values for Si
  - CMOS metal stack (~11 µm) seems not to influence this
- Bending force goes inversely with the third power of thickness

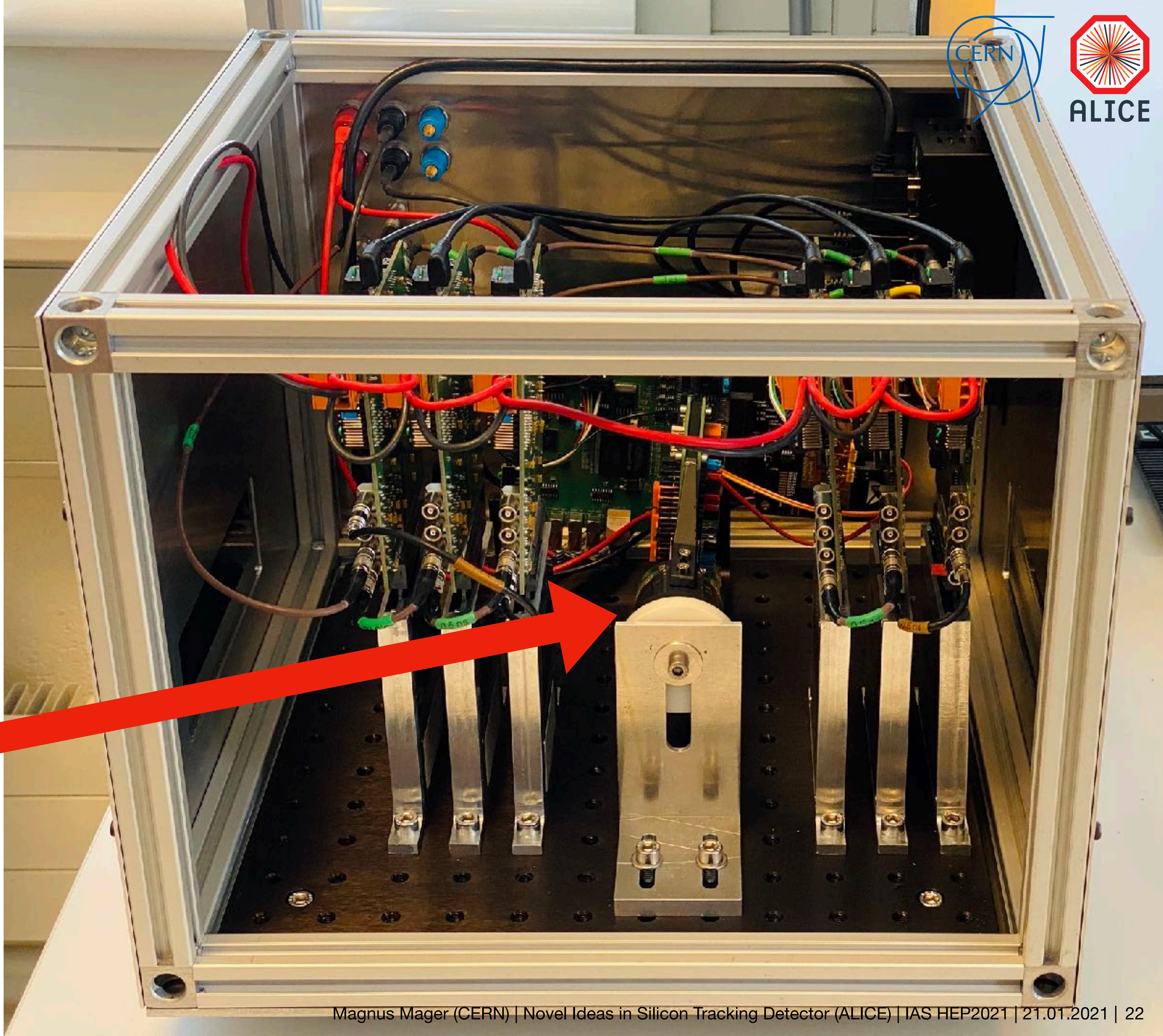
# Bending ALPIDE
example

# Bending of wafer-scale chips
## example

# Testbeam
## setup

- Second beam in August 2020
- This time bent in the perpendicular direction, i.e. bond on the curved part

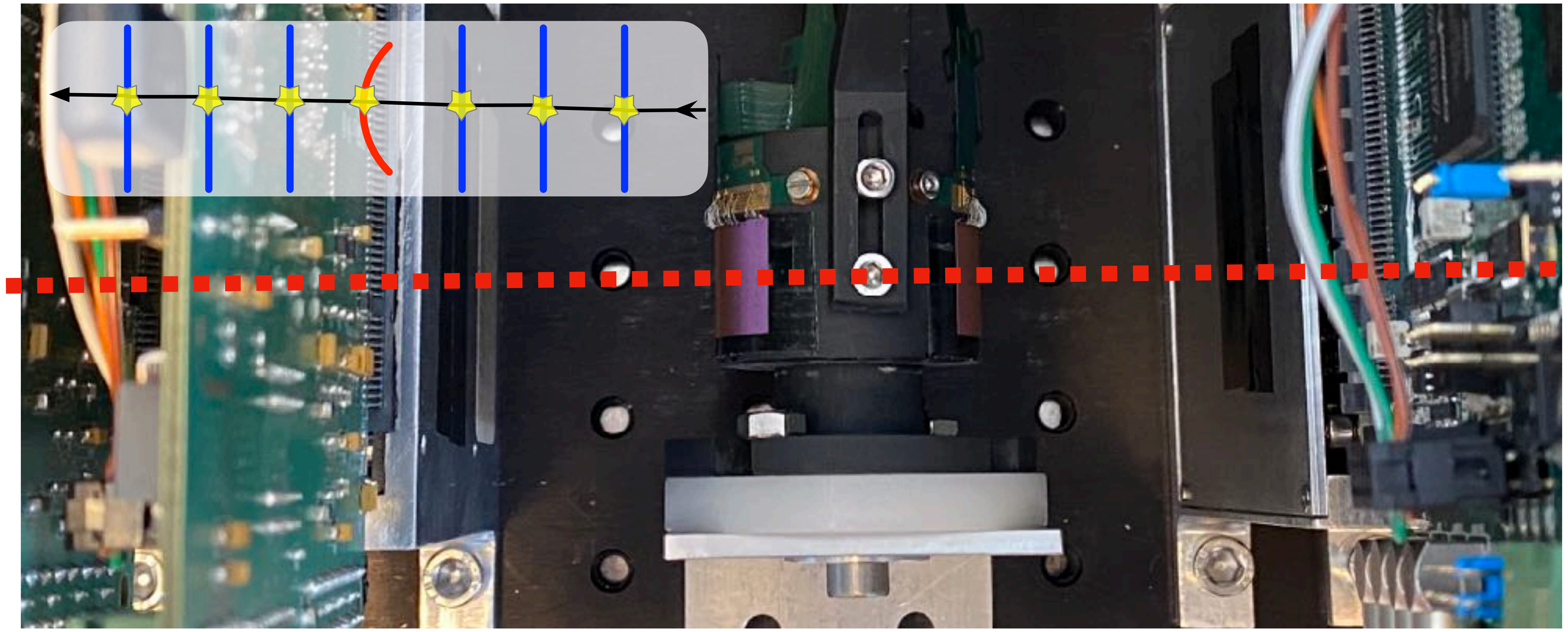




# Testbeam
## setup II

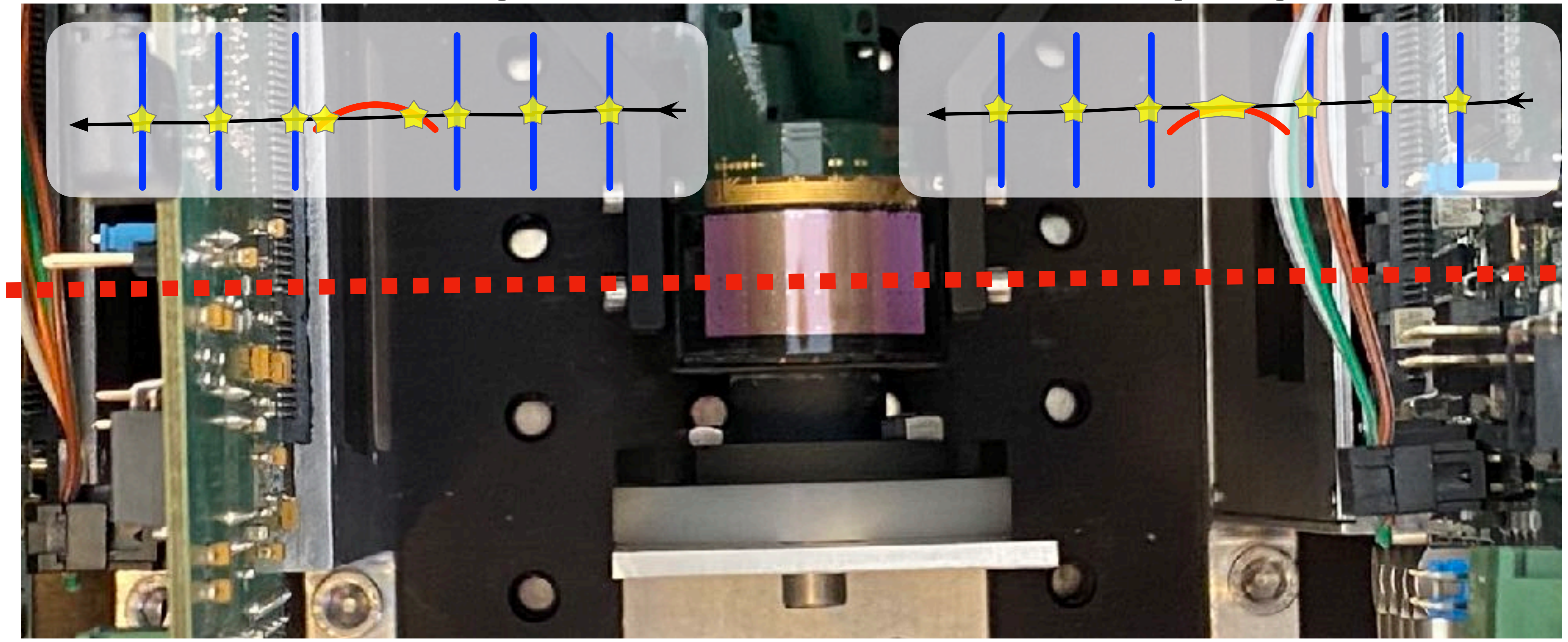
- They work!
- Very interesting geometries are becoming possible
- Data look beautiful
- Analysis ongoing

“ordinary”

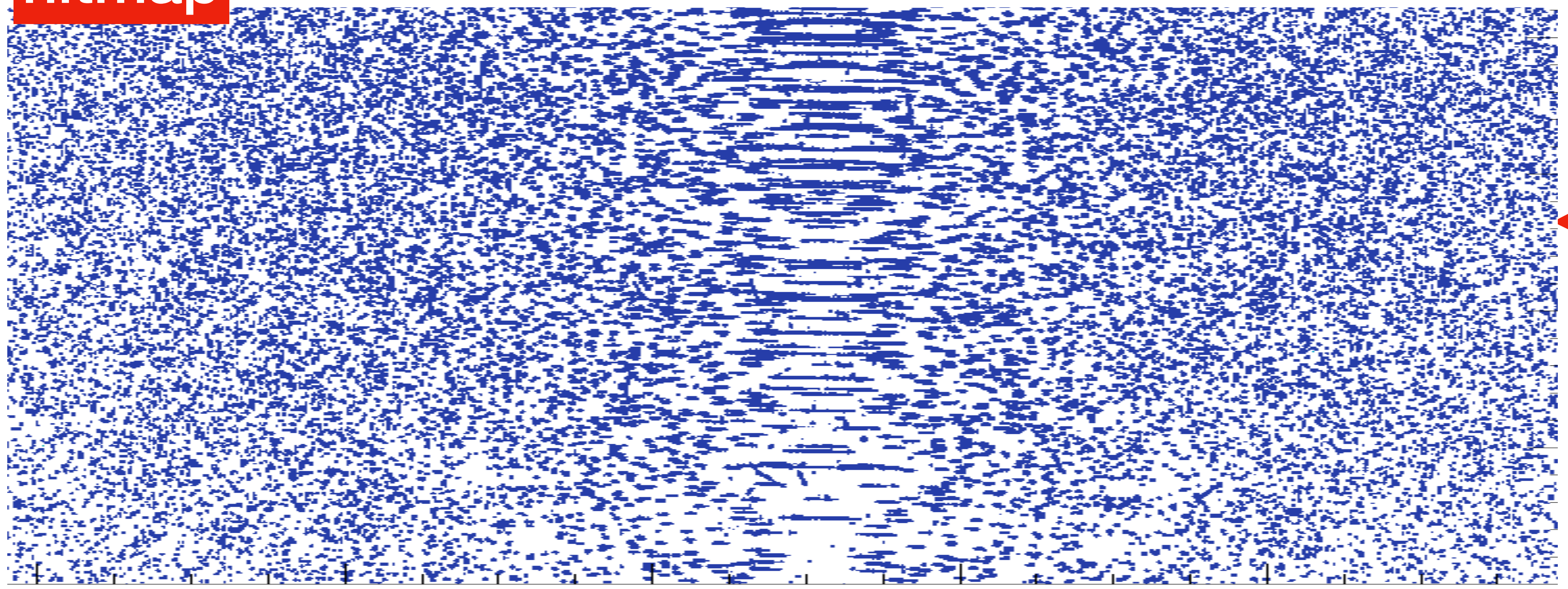


double-crossing

grazing



hitmap



# Testbeam
## results

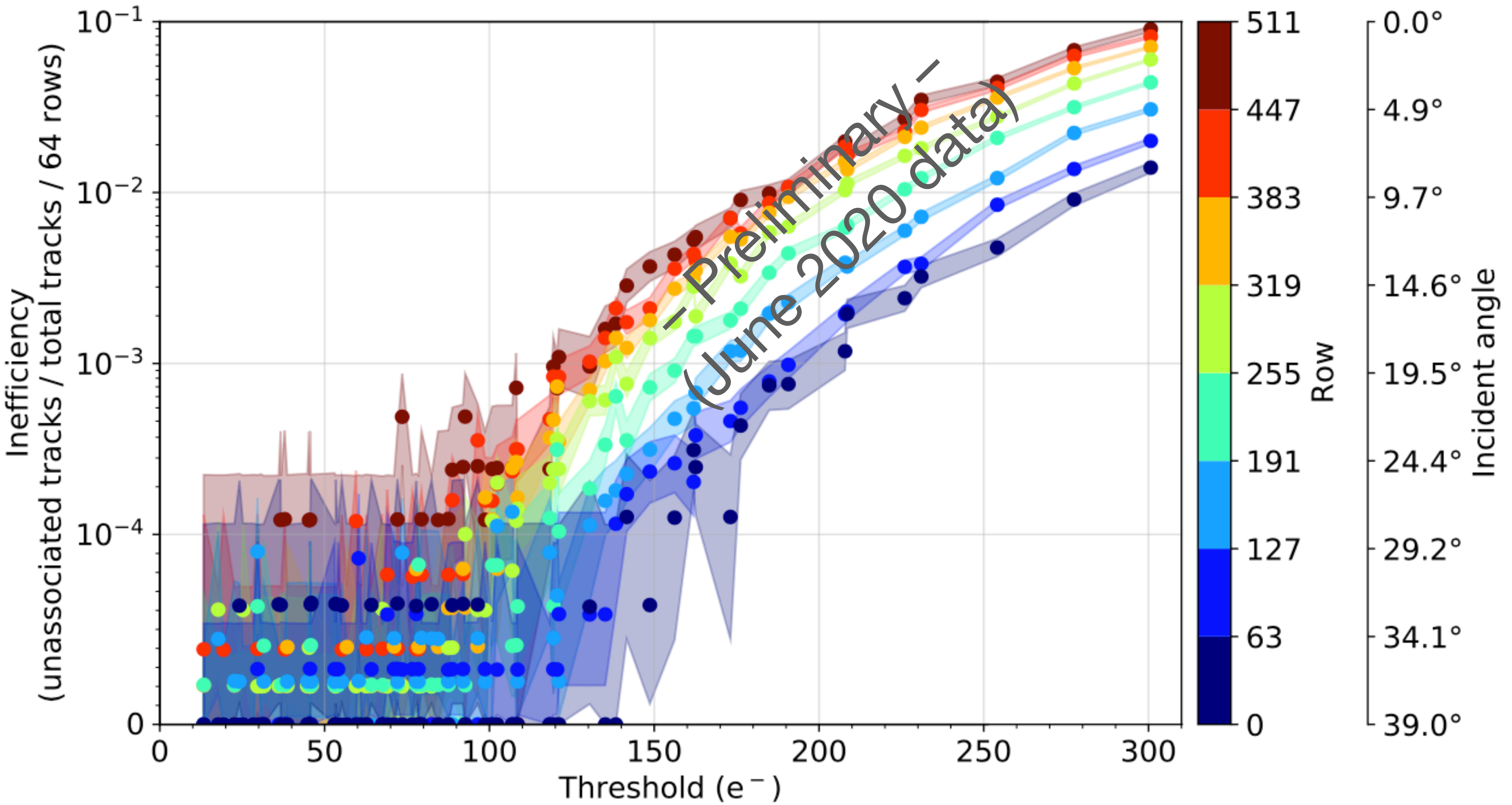
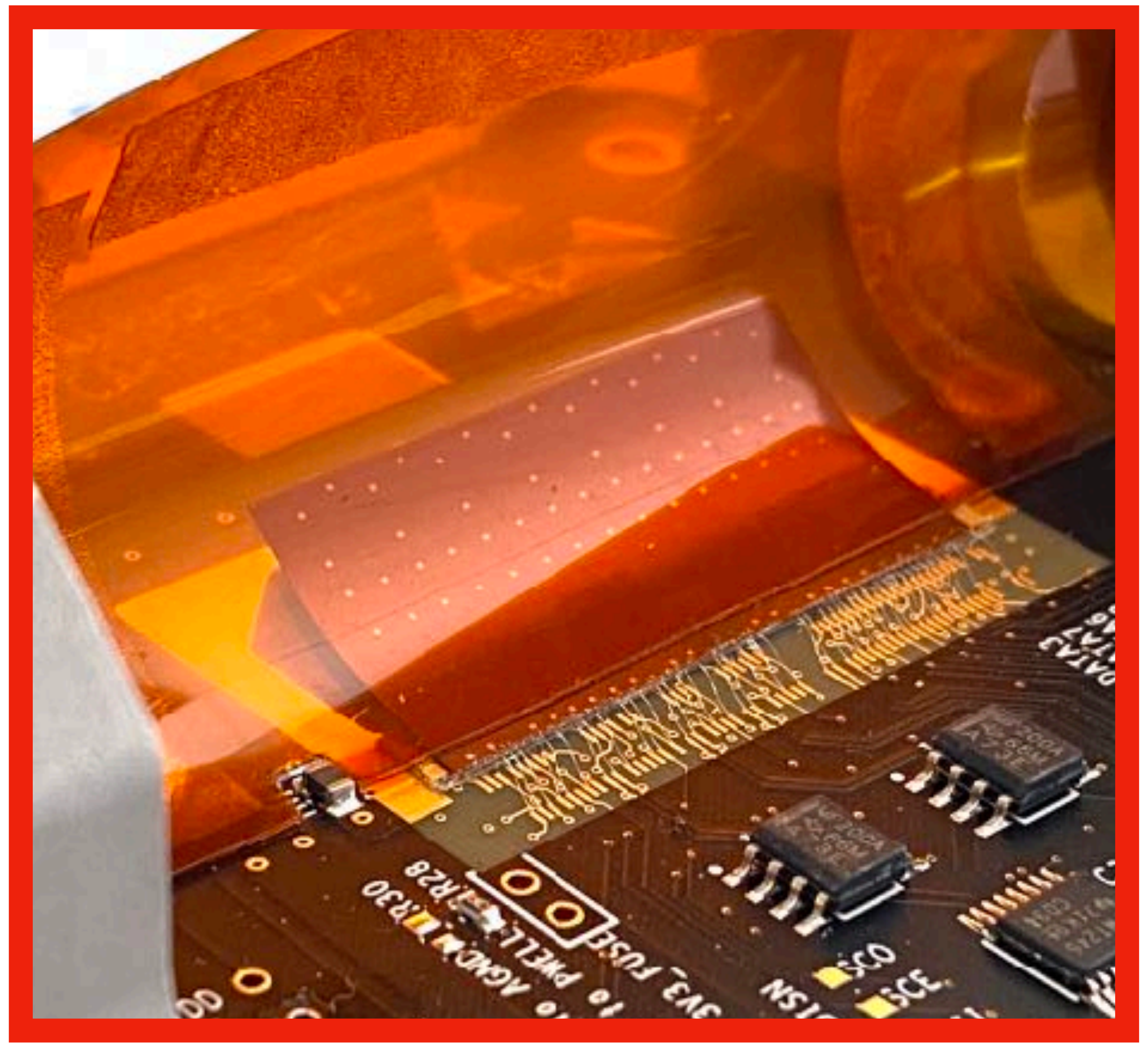
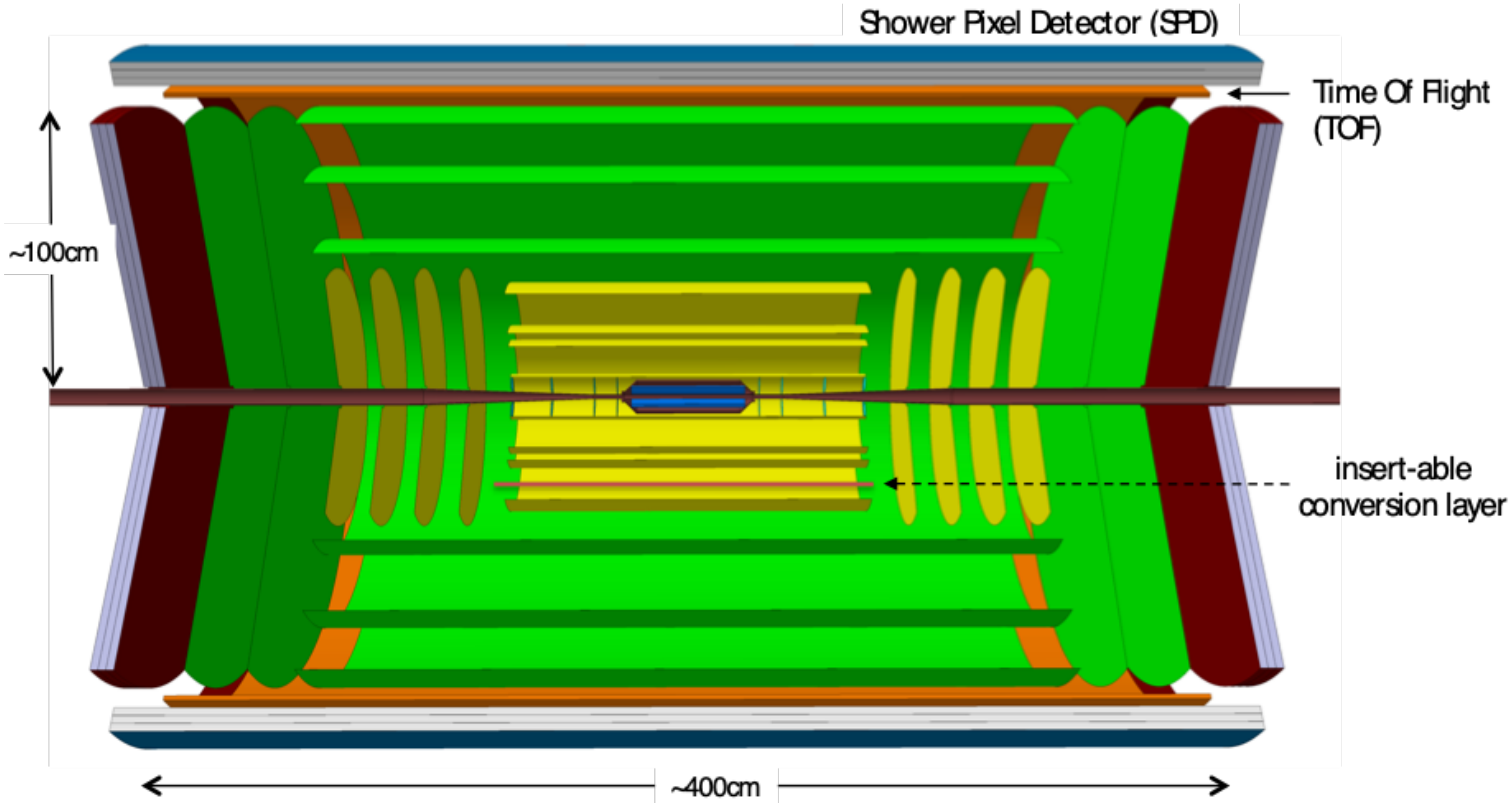



Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale ($10^{-1}$ to $10^{-5}$) to show fully efficient rows. Each data point corresponds to at least 8k tracks.



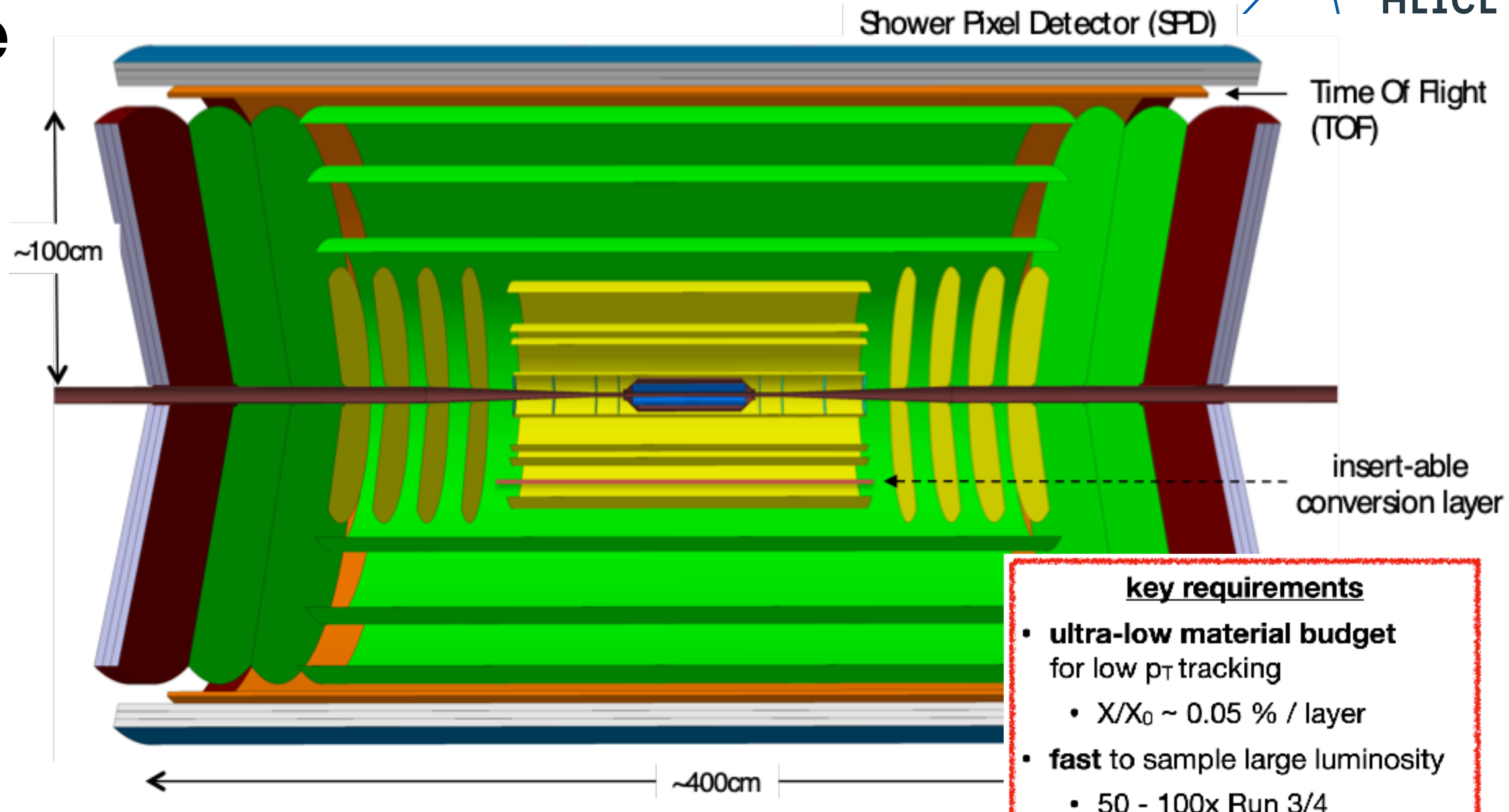
The chips just continue to work!

# ALICE 3


Shower Pixel Detector (SPD)
Time Of Flight
(TOF)
~100cm
insert-able
conversion layer
~400cm

# ALICE 3

## glimpse into the further future




- ALICE plans the next-generation heavy-ion experiment
  - targeting LHC Run 5 and beyond
- Based on an entirely new, compact detector fully based on silicon technology(-ies)
- Tracking
  - ~10 layers (blue, yellow, green) based on MAPS
- Particle identification
  - Time-of-Flight layers (orange) in central barrel based on silicon timing sensors
  - Pre-Shower Detector (outermost blue) based on dense material and MAPS

**key requirements**

- **ultra-low material budget** for low $p_T$ tracking
  - $X/X_0$ ~ 0.05 % / layer
- **fast** to sample large luminosity
  - 50 - 100x Run 3/4
- **large acceptance**
  - $|\eta| < 4 \Rightarrow \Delta\eta = 8$ (total)
  - $|\eta| < \sim 1.4$ (central barrel)
- **excellent spatial resolution** for tracking and vertexing
  - innermost layers: $\sigma$ < 3 µm
  - outer layers: $\sigma$ ~ 5 µm
- **precise time measurement** for particle identification
  - $\sigma$ ~ 20 ps

# Summary

- **ALICE ITS2** is the first really **large-scale** (O(10 $m^2$)) application of **MAPS** in HEP
  - the detector is fully built and **ready for installation**
  - commissioning results verify excellent system-level performance
- The development of **ALPIDE** marks a **new generation** of MAPS in terms of functionality and performance figures
- **ALICE ITS3** will push the technology even further, approaching the massless detector
  - R&D encouraged by LHCC in Sep 2019 and progressing at full steam
  - just proved the feasibility of curved silicon detectors, marking **the start of a new chapter** of silicon-detector designs
- Silicon detectors, *and MAPS in particular,* can take full advantage of semiconductor industry, making large-scale (not only "inner") tracking applications possible
  - **ALICE 3** is based on full-silicon tracker

# Thank you!