LHC Injectors Upgrade

SPS RF interlocks post-LS2

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Outline

- Introduction – SPS RF upgrade
- RF power interlocks
- Beam interlocks
- Interlock procedures and OP interface
- Conclusion

LIU SPS RF upgrade

- **200MHz travelling wave cavities**
  - TWC200 cavities removed from SPS, dismantled and reassembled
  - 4 cavities (4 and 5 sections) + spare sections → 6 cavities (3 and 4 sections)
- **New Solid State power Amplifiers (Thales)**
  - Powering the 2 new cavities (cavity 3 and cavity 6)
  - 16 towers per cavity (total 32)
  - 80 amplifier modules per tower
  - Controls: 1 PLC per tower + 1 PLC per cavity
- **Existing Siemens and Philips power plants**
  - Tetrode tube amplifiers + solid state pre-drivers
  - 2 cavities each
- **Renovation of Low-Level RF system**
  - LLRF Cavity Control and Beam Control (analog + VME) removed from Faraday cage
  - Replaced with fully digital microTCA-based feedback systems and new electronics for pickup and cavity controller front-ends

RF power interlocks overview

- **Protections limit maximum power to avoid damage to hardware**
  - In particular for Thales SSPA but also for existing Philips and Siemens amplifiers
  - Several layers of interlocks with different timescales

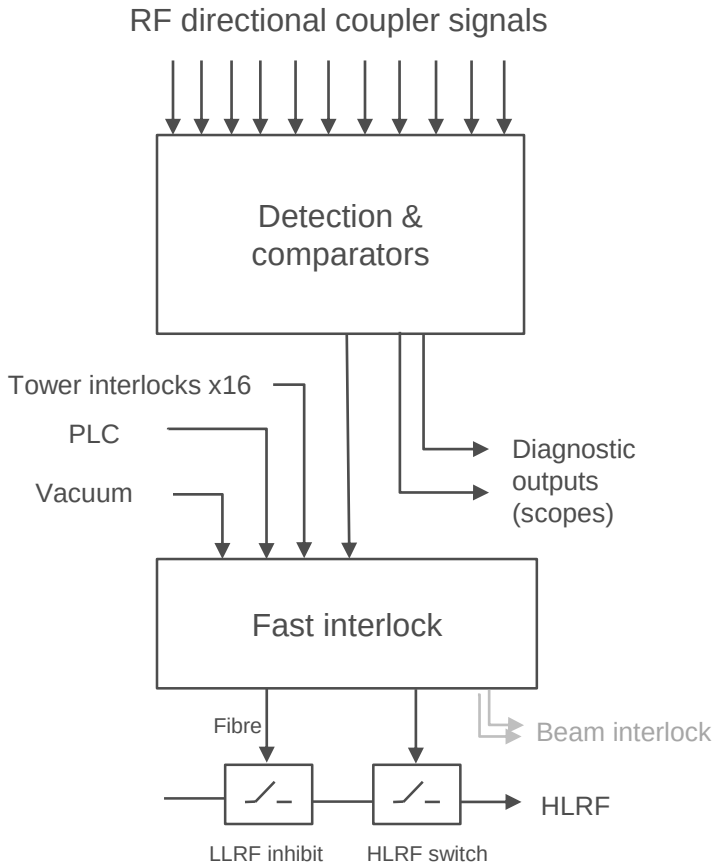
Functionality	Check	System	Averaging	Action
Digital clamping of RF drive	**Peak** power	LLRF	**~10 ns**	**Alarm**
RF switch piloted by power (protect amplifiers)	**Peak** power	Fast interlock, ~50 µs delay	**11.5 µs (~2 turns)**	**RF OFF** (+ Dump)
RF switch piloted by PLC (protect coax lines etc.)	**Average** power	Power/PLC	**Limits <10 s and >10 s**	**RF OFF** (+ Dump)
Amplifier interlocks (*I*, *V*, etc.)	**Average** power	Power/PLC	**~200 ms**	**RF OFF** (+ Dump)

Hierarchy

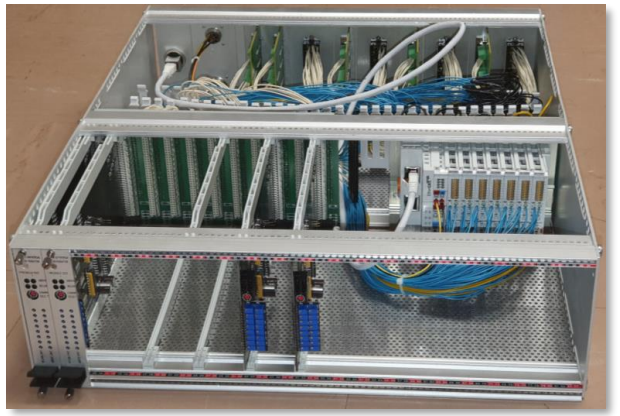
- The clamping performed by LLRF is a **functional limitation**
- All other limits are part of **hardware protection**

RF power interlocks implementation

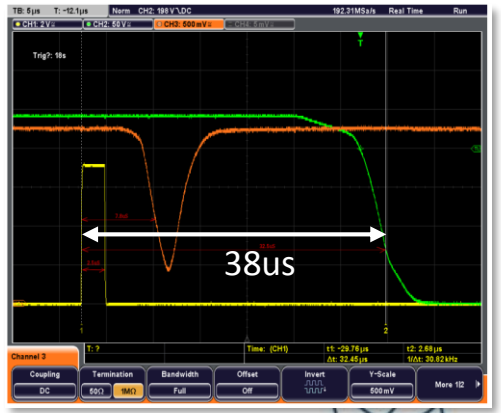
- **Fast interlock system**
  - Based on Beckhoff fast interlock modules in PLC
    - Hardware logic independent of PLC CPU
  - Interlock chain performance tested and accepted
    - ~38us latency from input to output
  - Deployed in Thales, currently under test
    - Power interlocks generated via hardware comparators (47 signals)
  - Fast interlock modules installed in Siemens/Philips
    - Power signals not yet available, but will eventually be used for average power interlocks
    - Amplifier protection by internal fast interlocks



- **Signal acquisition and slow interlocks:**
  - Slow (average power) interlocks will be implemented in PLC
    - Analog inputs installed in Philips and Siemens PLCs (4 channels par cavity), will shortly be installed in Thales PLCs
  - Average power measurements will also be published via FESA
  - Alarms and warnings will be generated
  - Fast analogue signals available in patch panel for scope



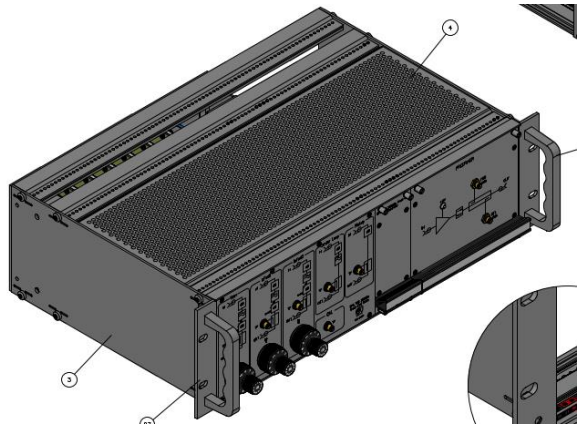
Fast interlock chassis



Latency test

RF beam interlocks overview

- **Beam interlocks are foreseen to:**
  - protect **Thales amplifiers** from reverse power
    - amplifiers are not in safe state immediately after a trip
    - potential for damage with intense beams if beam not dumped
  - protect **pickup analog front-ends** from overvoltage
    - switchable attenuators (PPM)
    - can burn electronics if wrong attenuation selected
    - HW detection and interlock in analog front-end chassis
  - pre-empt **beam loss** in case of RF trip during ramp
    - simulations show that for HL-LHC beam, demanded power peak is before end of ramp
    - close to limit → trip of 1 cavity would result in beam loss
    - dump if any 200MHz cavity trips (not foreseen for 800MHz)
  - inhibit injection if **incorrect reference clocks** selected
    - "LHC REFERENCE" must be selected if Dynamic destination = LHC1_TI1 or LHC2_TI8
    - check 5ms before 1st injection
    - before LS2: NIM module (manual switches) + VME DIO + FESA class
    - after LS2: new VME 6-channel switch module + FESA class (remote PPM control only)

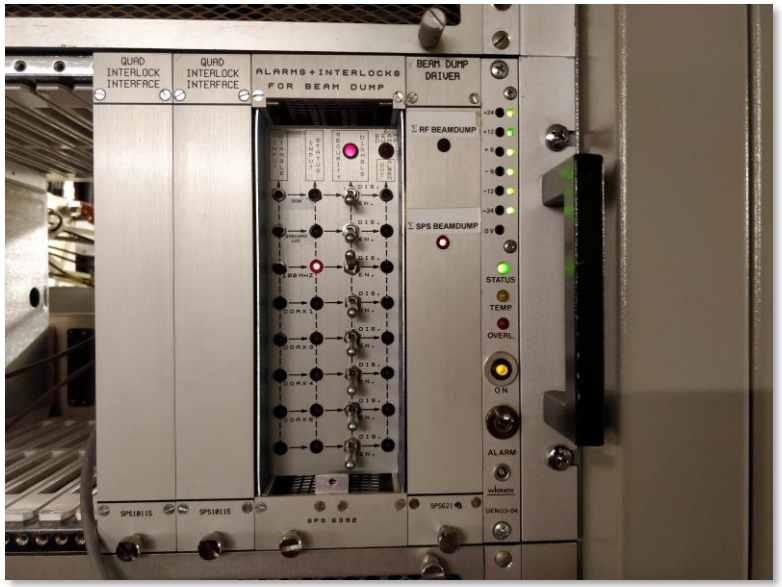


New pickup front-ends

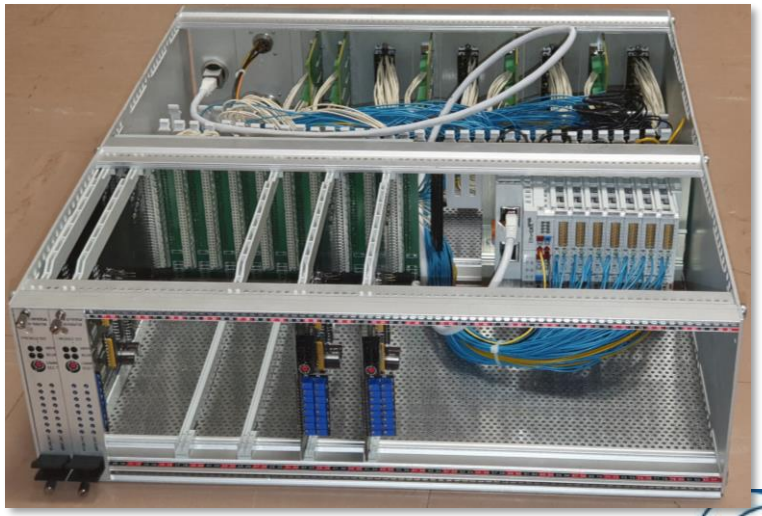
Clock switching pre-LS2

Beam interlocks implementation

- **Beam interlock concentrator + CIBU in BA3 Faraday cage**
  - 1 input from each cavity interlock
    - 1 fibre per cavity already foreseen for RF OFF signal to LLRF
    - 1 additional fibre will be used for beam interlock
  - Inputs from other equipment in Faraday cage
    - PU front-ends, clock selection, crab cavity phase, …
- **Installation of new fast interlock crate in Faraday cage**
  - Replaces old beam dump interface crate and alarms PLC
  - Same HW used for cavity interlocks
  - Greater flexibility, monitoring and remote control
  - Possibility to mask interlocks in case of cavity downtime
    - Allow degraded mode operation with lower intensity beams
    - Management of masking, critical settings?



Faraday cage beam dump interface pre-LS2



Proposed replacement post-LS2

Interlock behaviour (Thales)

- **16 solid-state amplifier towers per cavity**
  - 80 SSPA modules per tower
  - After RF trip, possible SSPA module damage from beam-induced reverse power
- **If a module trips or RF power limit exceeded: RF OFF and beam dump**
  - Interlocks latched - operator has to make a reset
  - PLC automatically switches faulty modules off line (output short circuited)
- **As long as we still have more than N modules, the operator can then switch on again, beam permit restored**
  - N is a programmable parameter, defined by RF experts
- **If the number of active modules on one tower is lower than N: RF off and beam dump**
  - until an RF expert repairs or lowers N
- **If we decide to switch off the cavity (all modules off line), RF switch will remain off, beam permit automatically restored**
  - Self-masking - no need for explicit masking of beam interlocks
  - Injecting beam with poor RF power, BLMs will dump the beam
    - Rely on operational procedure to avoid this
    - SIS could be surveying the lines and interlock if there is not enough power

Similar logic for Philips/Siemens

- Switching back on will clear beam interlock
- If restart not possible, masking?
- Automatic beam permit restore?

Controls and OP interface

- **RF power interlocks will be integrated into existing RF PLC FESA class**
  - PLC acquisition will also be available in this FESA class
- **Interlock thresholds management**
  - Fast interlocks: set in hardware (potentiometers)
  - “Slow” PLC interlocks: Keep threshold settings expert but make them readable for OP
- **Warning when approaching power limits**
  - Warning limits could be put into FESA class or application
- **Alarms**
  - Archived alarms in dedicated application (or tab in RF power application)
  - Alarm status and timestamp taken directly from FESA class Alarm property
  - Try to get history data also from logging
- **Beam interlock concentrator + Faraday cage alarms**
  - HW integration and PLC development starting (Dec 2020)
  - New FESA class to be written

Conclusions

- **LIU-SPS renovation of RF system requires reorganisation and implementation of new interlocks**
- **Fast interlock system integrated into controls of Thales solid-state amplifiers**
  - Most important for hardware protection
- **Evolution of interlocks for existing Philips and Siemens systems**
  - Less critical than Thales
  - Amplifier protection assured by existing internal interlocks
  - Protection of lines will benefit from average power interlocks (to be implemented)
- **Beam interlocks required for protection of Thales as well as other RF equipment**
  - New beam interlock crate being developed, will be ready in early 2021
- **Operational interface being defined in collaboration with OP**

LHC Injectors Upgrade

THANK YOU FOR YOUR ATTENTION!

Power observation and diagnostics

→ **Observation** and **logging** of RF power **per amplifier/cavity** averaged over relevant timescales

→ **Generate alarms**, but no further automatic action

Averaging duration	Purpose	Limit [MW] (3/4 sections)	Observation system
11.5 μs (~T_{rev}/2)	Peak power	**1/1.6**	**LLRF (fast acq.)**
10 ms	Fast manipulations, bunch rotation	**0.6/0.8**	**LLRF and PLC**
2 s	Acceleration part (fixed target beams)		**Measurement with PLC system**
10 s	Acceleration part of cycle (LHC-type beams)		
20 s	Limit towards CW for amplifiers	**0.4/0.5**	
Cycle length			
Super-cycle length			
10 min	Long term evolution		

→ Use capabilities of LLRF and PLC systems to determine power to cavities

→ Derive also average per cycle from LLRF for cross-calibration of PLC and LLRF systems