Introduction to Field Programmable Gate Arrays

Hannes Sakulin
CERN / EP-CMD

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What is a **F**ield **P**rogrammable **G**ate **A**rray ?
.. a quick answer for the impatient

- An FPGA is an integrated circuit
  - Mostly digital electronics
- An FPGA is programmable in the in the field (=outside the factory), hence the name “field programmable”
  - Design is specified by schematics or with a hardware description language
  - Tools compute a programming file for the FPGA
  - The FPGA is configured with the design (gateware / firmware)
  - Your electronic circuit is ready to use

With an FPGA you can build electronic circuits …
… without using a bread board or soldering iron
… without plugging together NIM modules
… without having a chip produced at a factory

Outline

- Quick look at digital electronics
- Short history of programmable logic devices
- FPGAs and their features
- Programming techniques
- Design flow
- Example Applications in the Trigger and DAQ domain

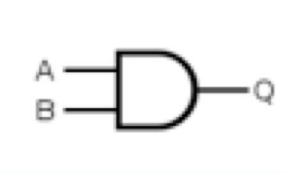
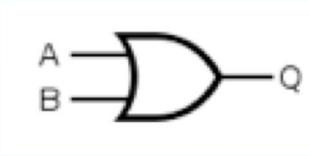
Acknowledgement

- Parts of this lecture are based on material by Clive Maxfield, author of several books on FPGAs. Many thanks for his kind permission to use his material!

Re-use

Digital electronics

The building blocks: logic gates

		Truth table	C equivalent
AND gate			q = a && b;
OR gate			q = a || b;
Exclusive OR gate XOR gate			q = a != b;

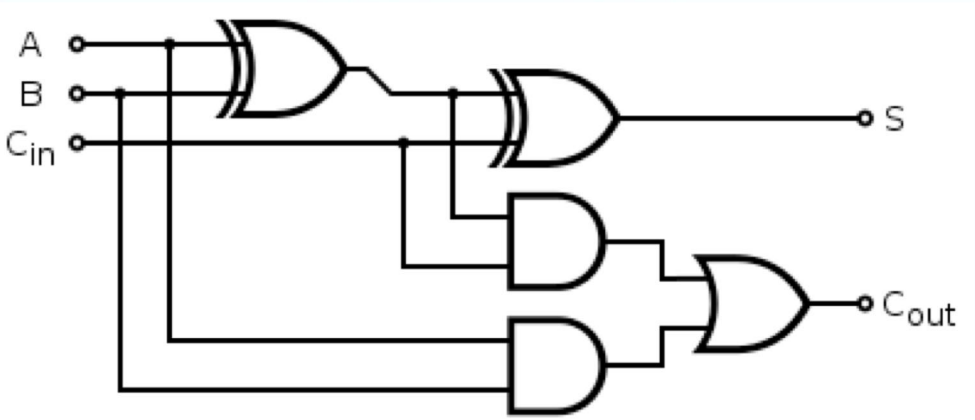
INPUT		OUTPUT
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

INPUT		OUTPUT
A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

⋮

Combinatorial logic (asynchronous)



Example: Full adder with carry-in, carry-out

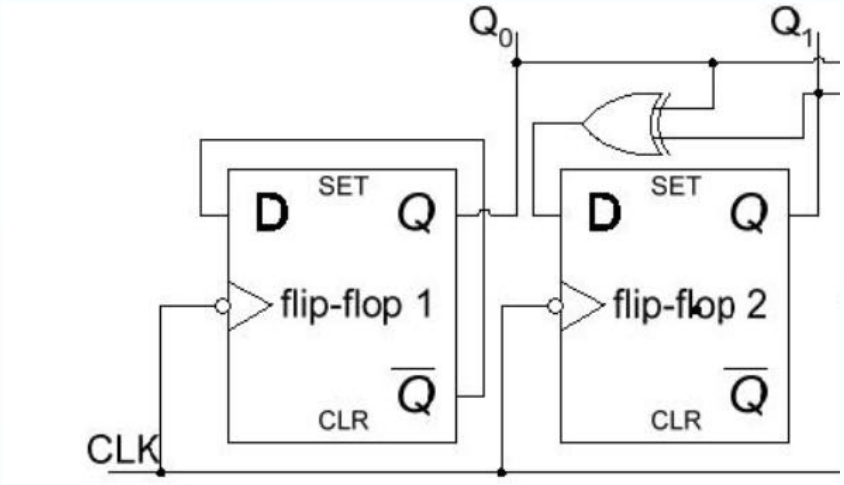
Outputs are determined by Inputs, only

A	B	C_{in}	S	C_{out}
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Combinatorial logic may be implemented using Look-Up Tables (LUTs)

LUT = small memory

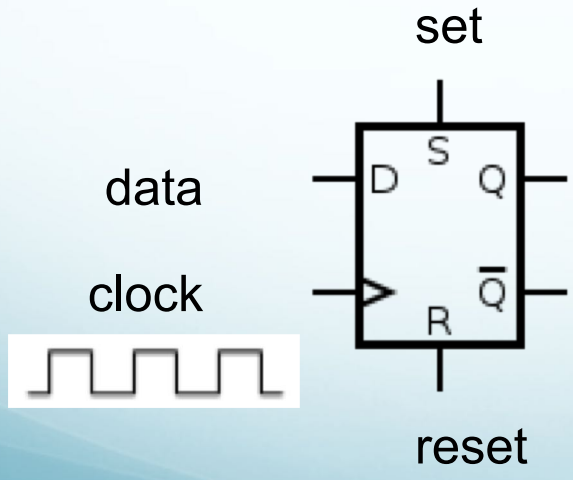
(Synchronous) sequential logic



Outputs are determined
by Inputs and their History
(Sequence)
The logic has an internal state

2-bit binary counter

https://www.zeepedia.com/read.php?b=9&c=32&d_flip-flop_based_implementation_digital_logic_design



Output

Inverted output

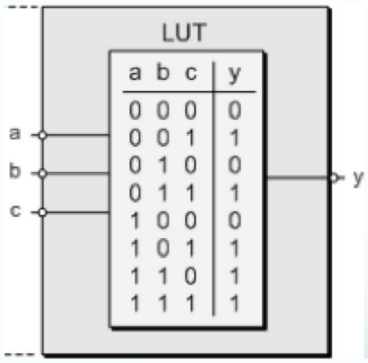
D Flip-flop:

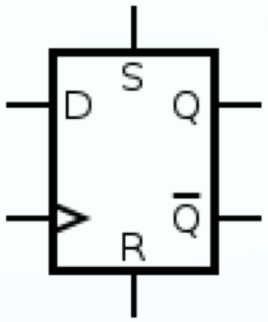
samples the data at the rising (or falling) edge of the clock

The output will be equal to the last sampled input until the next rising (or falling) clock edge

D Flip-flop (D=data, delay)

Synchronous sequential logic



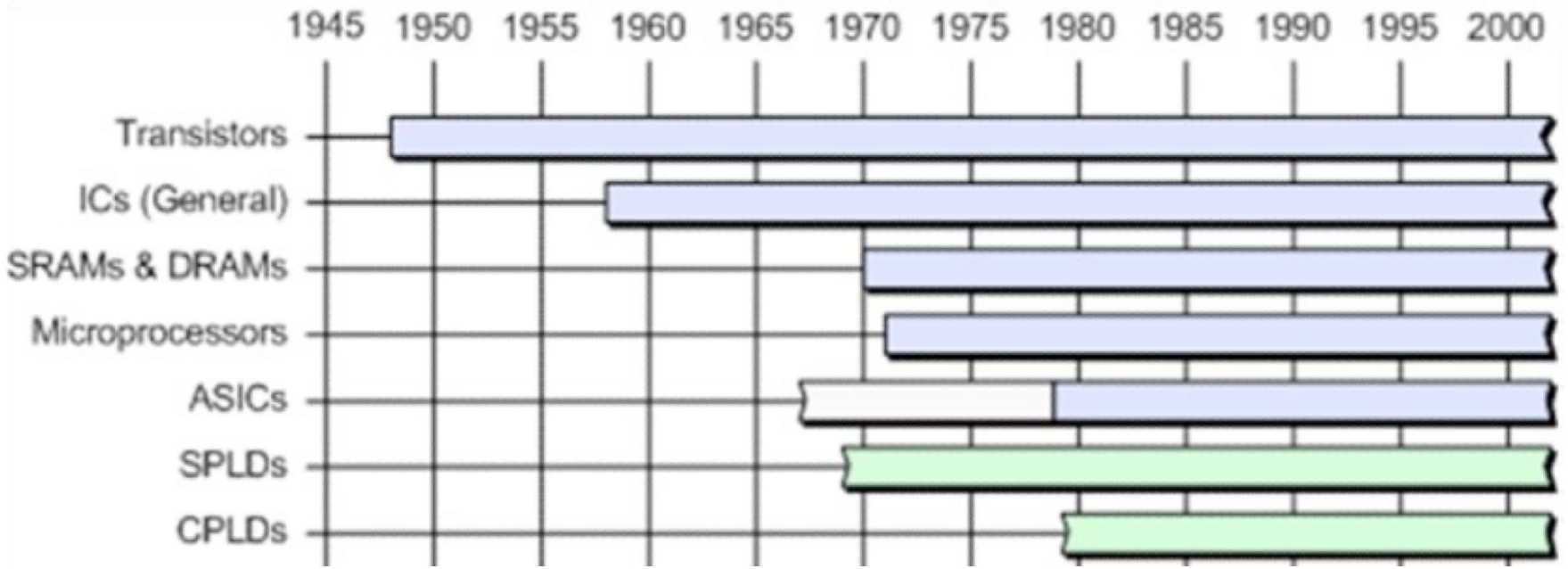


Using Look-Up-Tables and Flip-Flops
any kind of digital electronics may be implemented

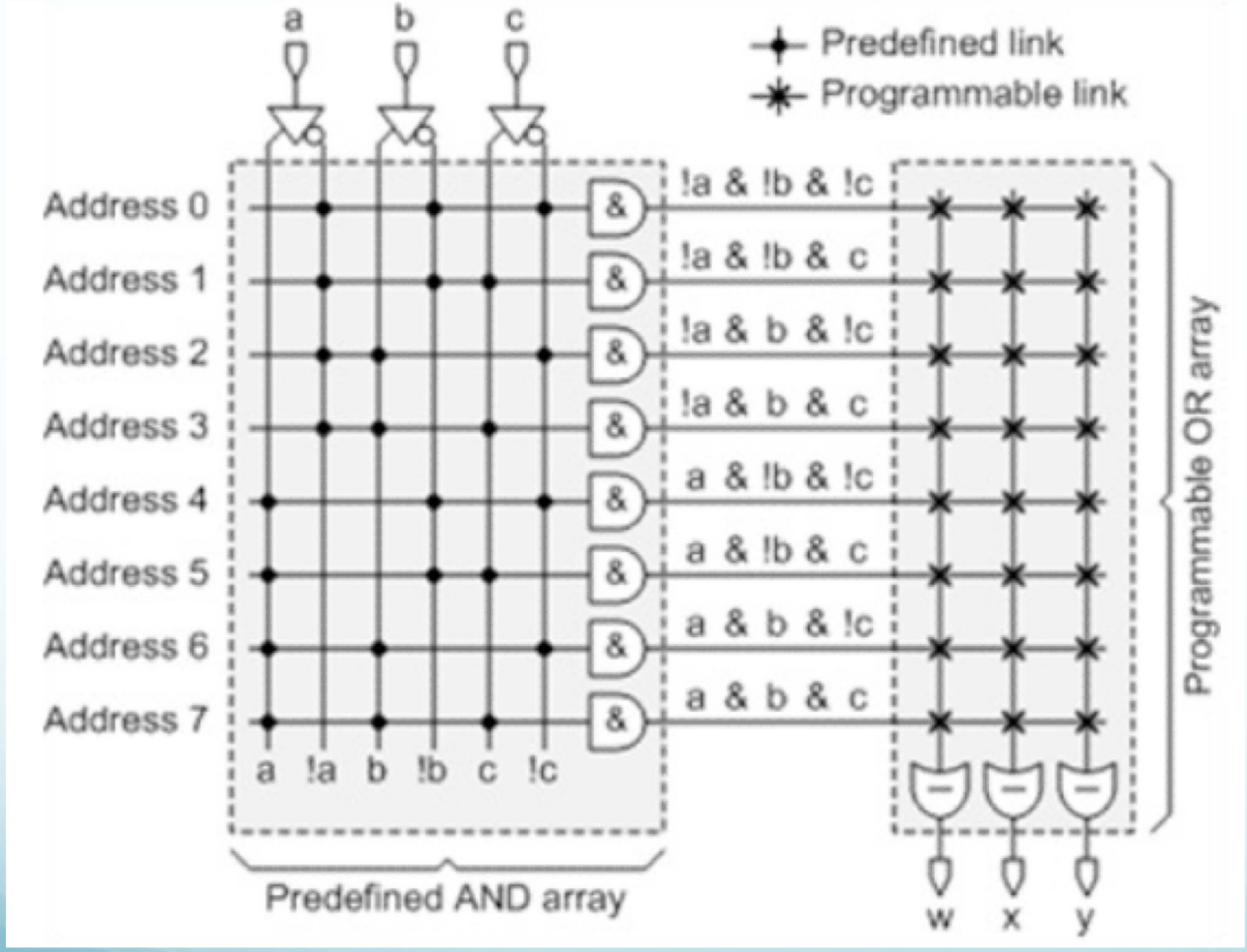
Of course there are some details
to be learnt about electronics design …

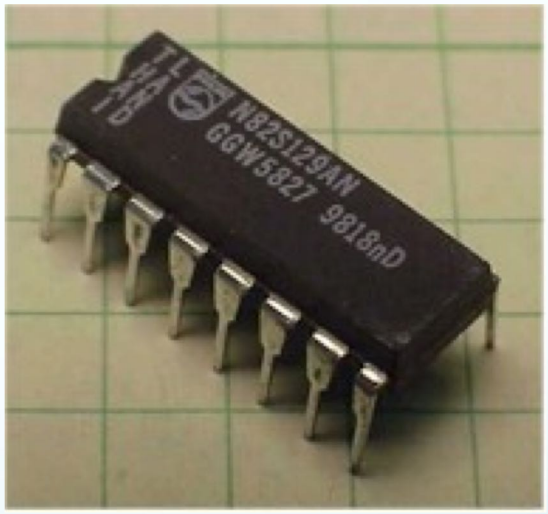
Programmable digital electronics

Long long time ago ...



Simple Programmable Logic Devices (sPLDs)
a) Programmable Read Only Memory (PROMs)

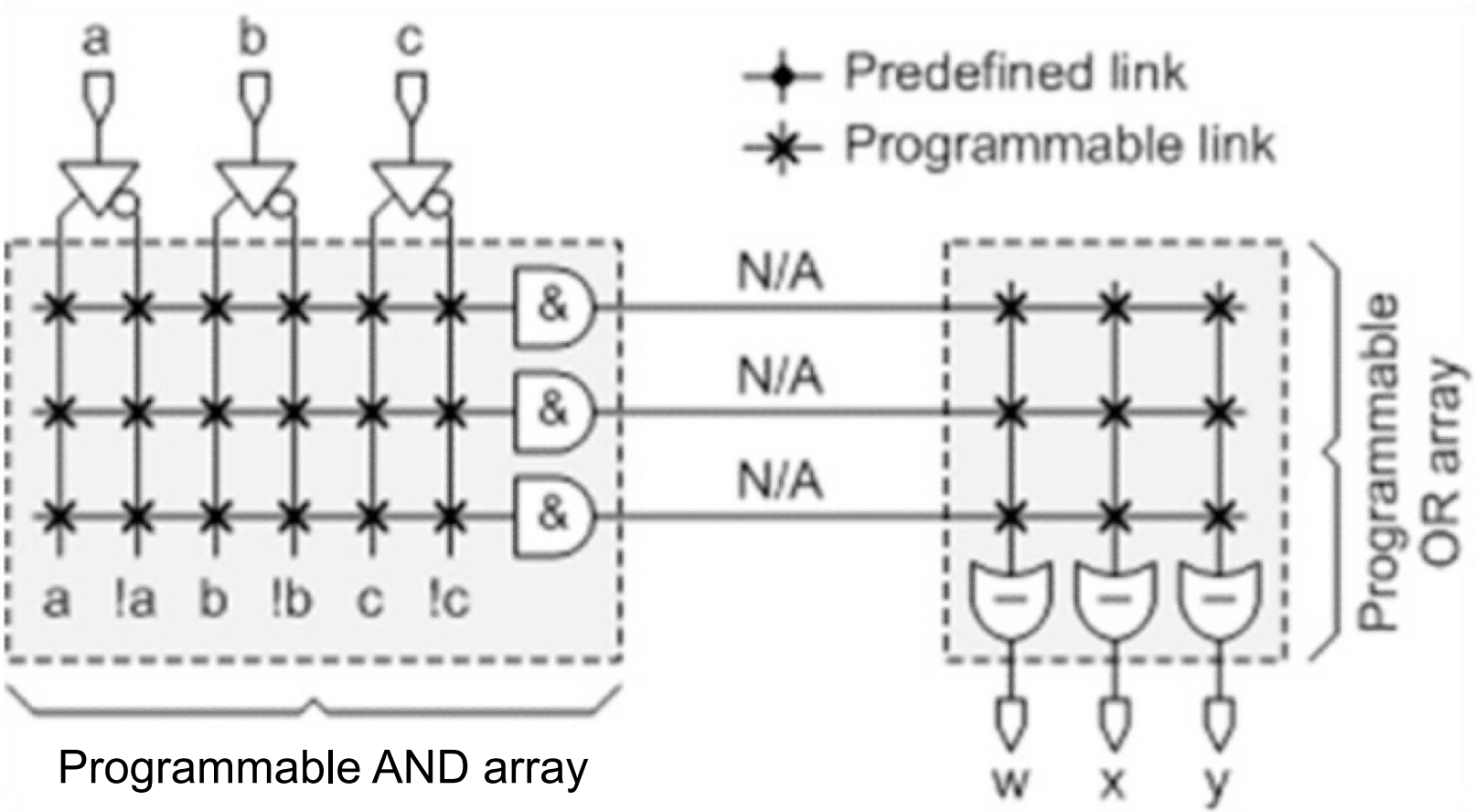




Late 60's

Unprogrammed PROM (Fixed AND Array, Programmable OR Array)

Simple Programmable Logic Devices (sPLDs)
b) Programmable Logic Arrays (PLAs)

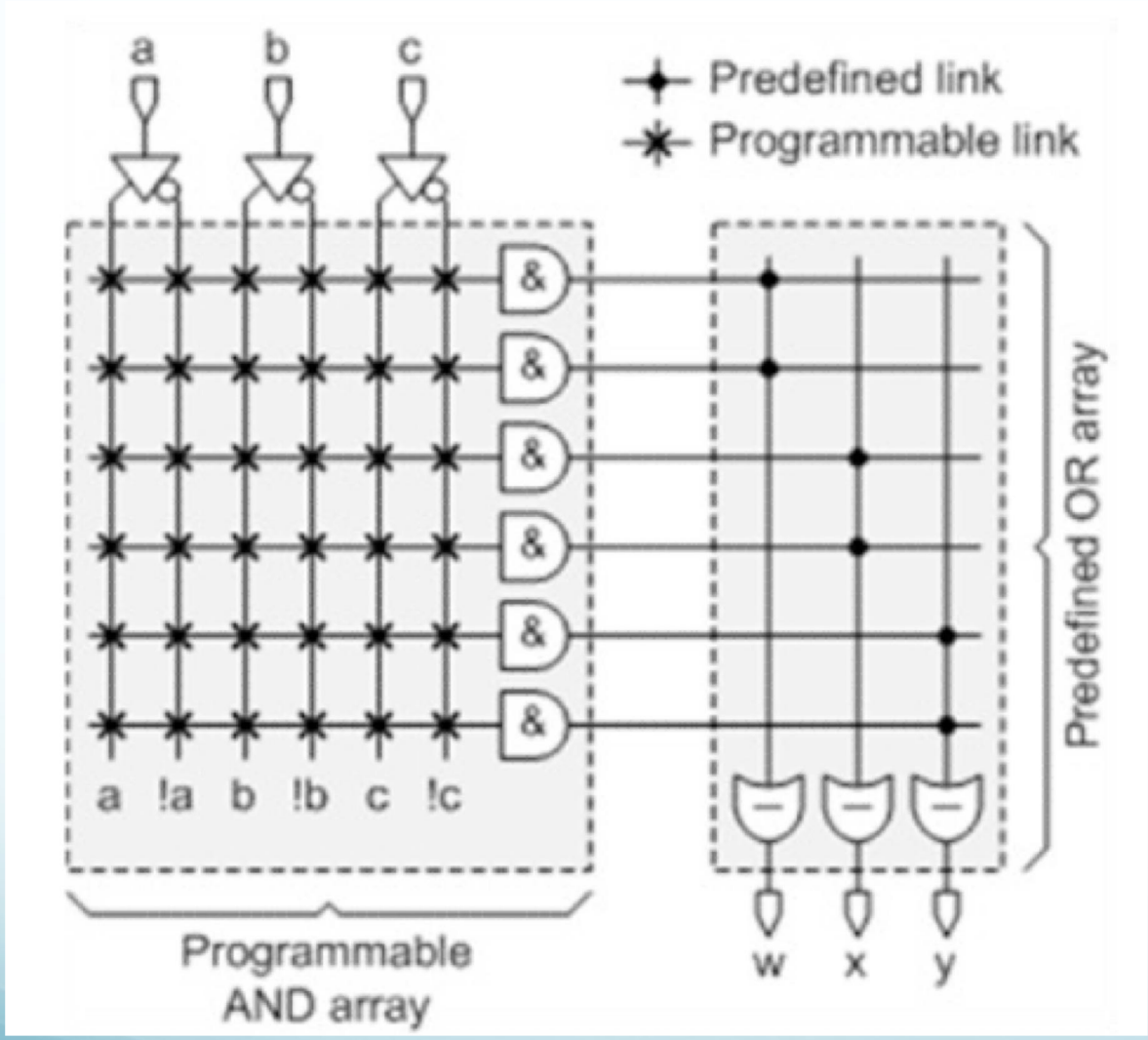


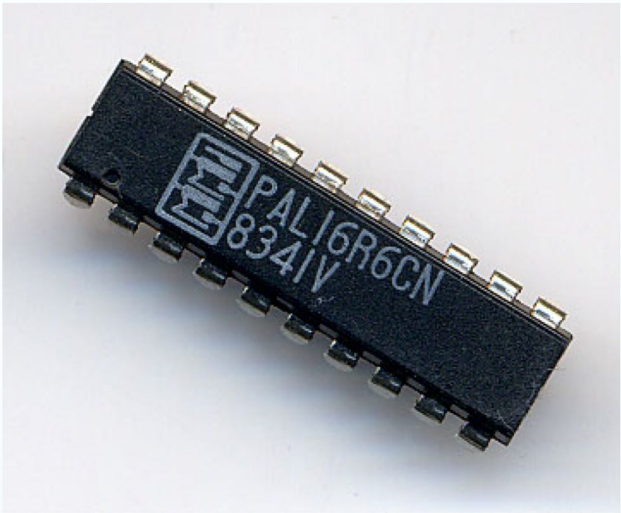
Unprogrammed PLA (Programmable AND and OR Arrays)

Most flexible
but slower

1975

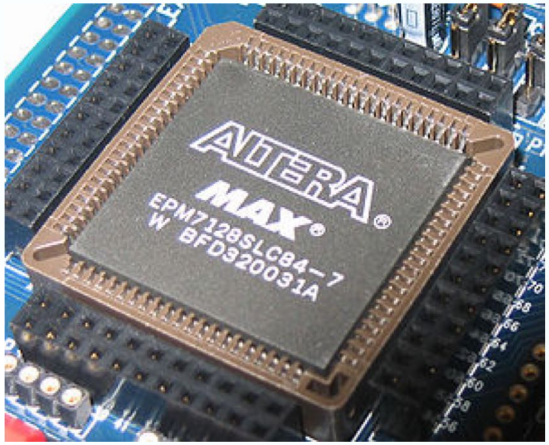
Simple Programmable Logic Devices (sPLDs)
c) Programmable Array Logic (PAL)

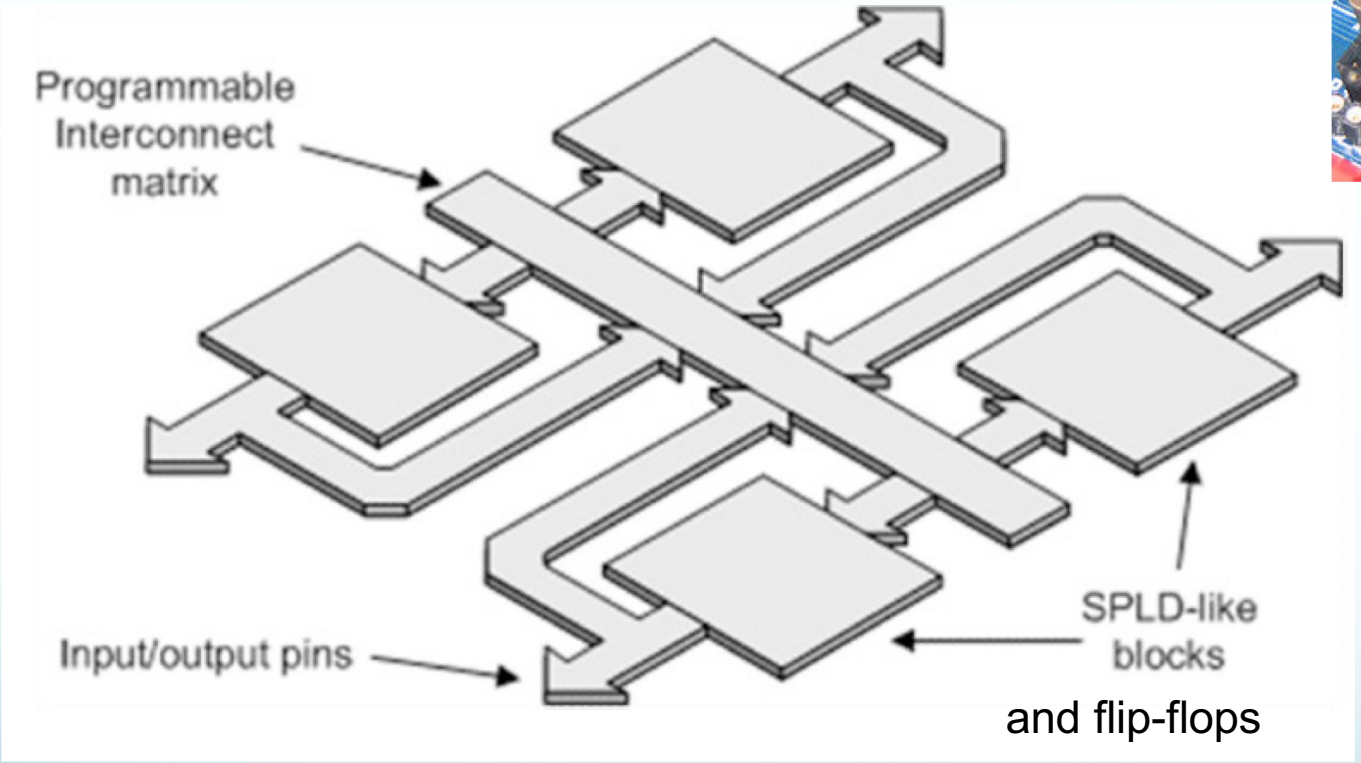




Unprogrammed PAL (Programmable AND Array, Fixed OR Array)

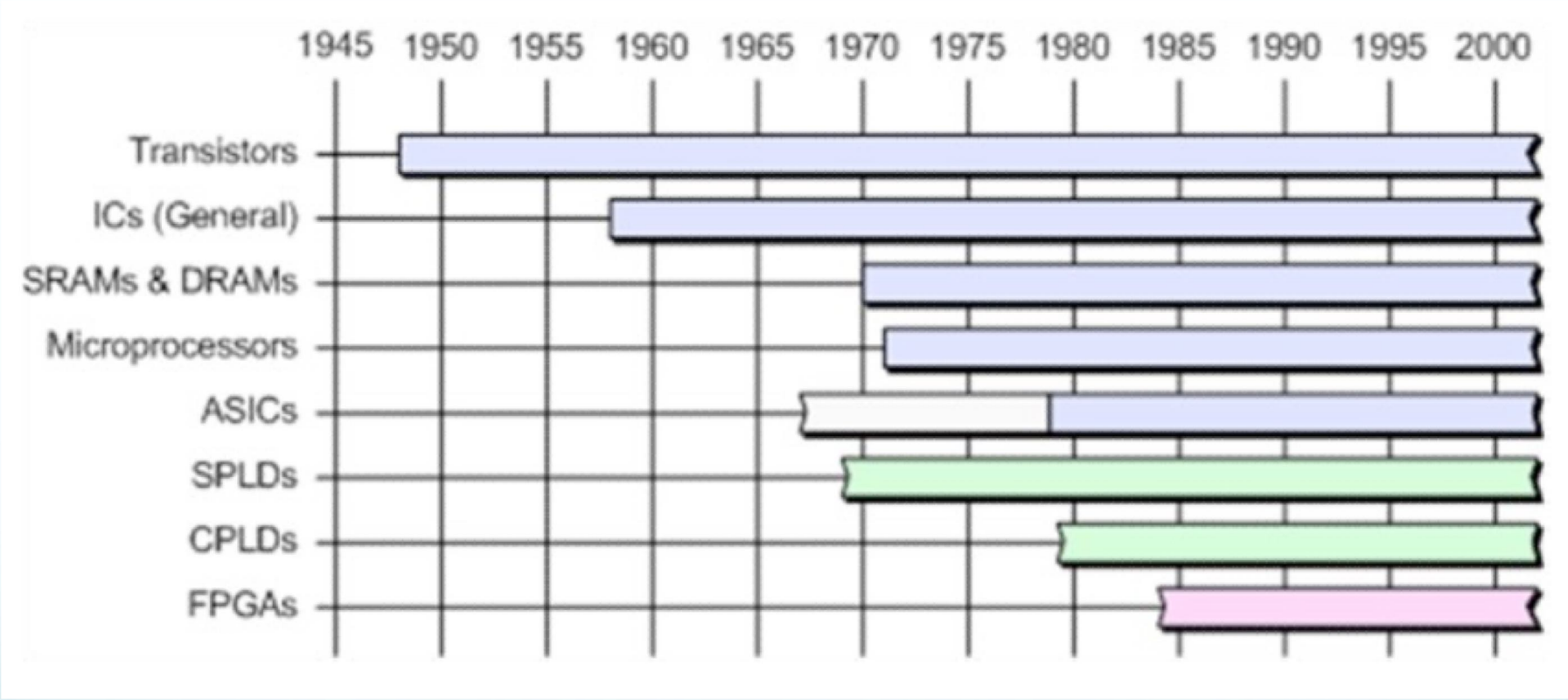
Complex PLDs (CPLDs)



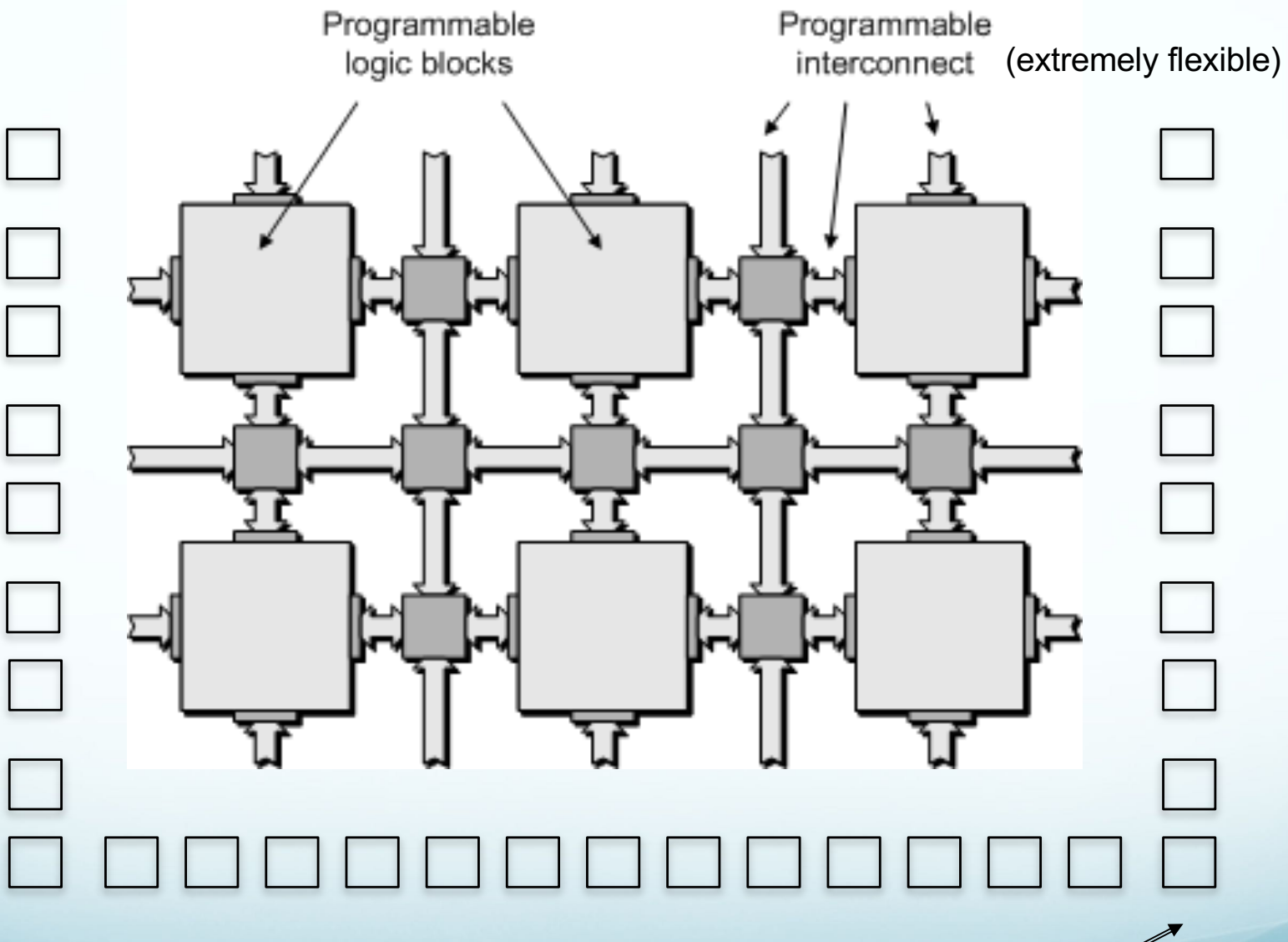


Coarse grained
100's of blocks, restrictive structure
(EE)PROM based

FPGAs ...

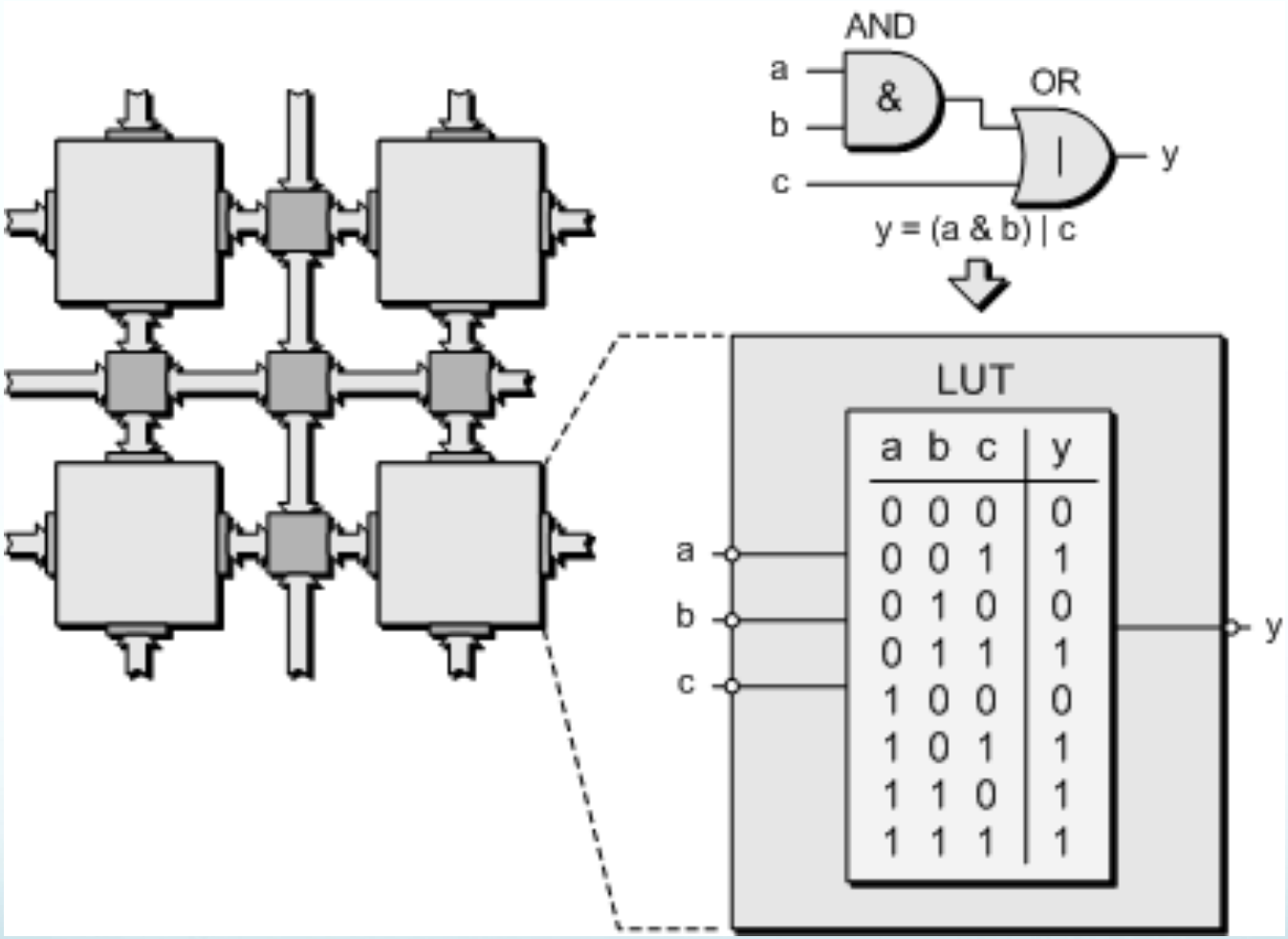

1945
1950
1955
1960
1965
1970
1975
1980
1985
1990
1995
2000
Transistors
ICs (General)
SRAMs & DRAMs
Microprocessors
ASICs
SPLDs
CPLDs
FPGAs

FPGAs

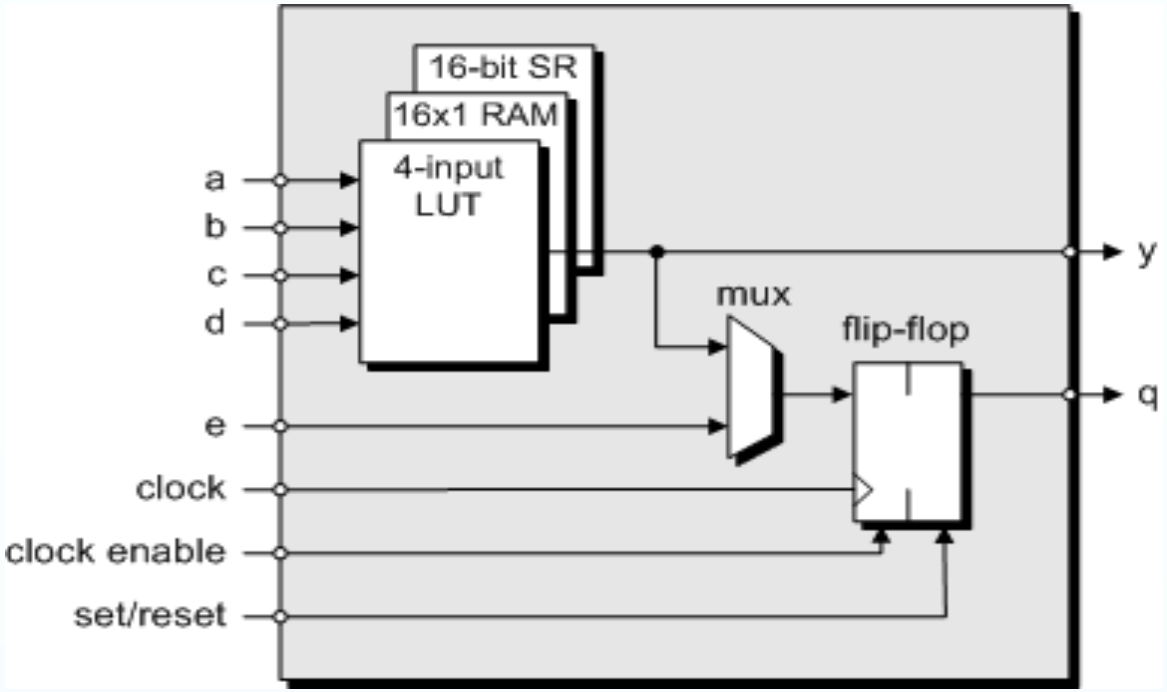


Fine-grained: 100.000's of blocks
today: up to 5 million logic blocks

LUT-based Fabrics



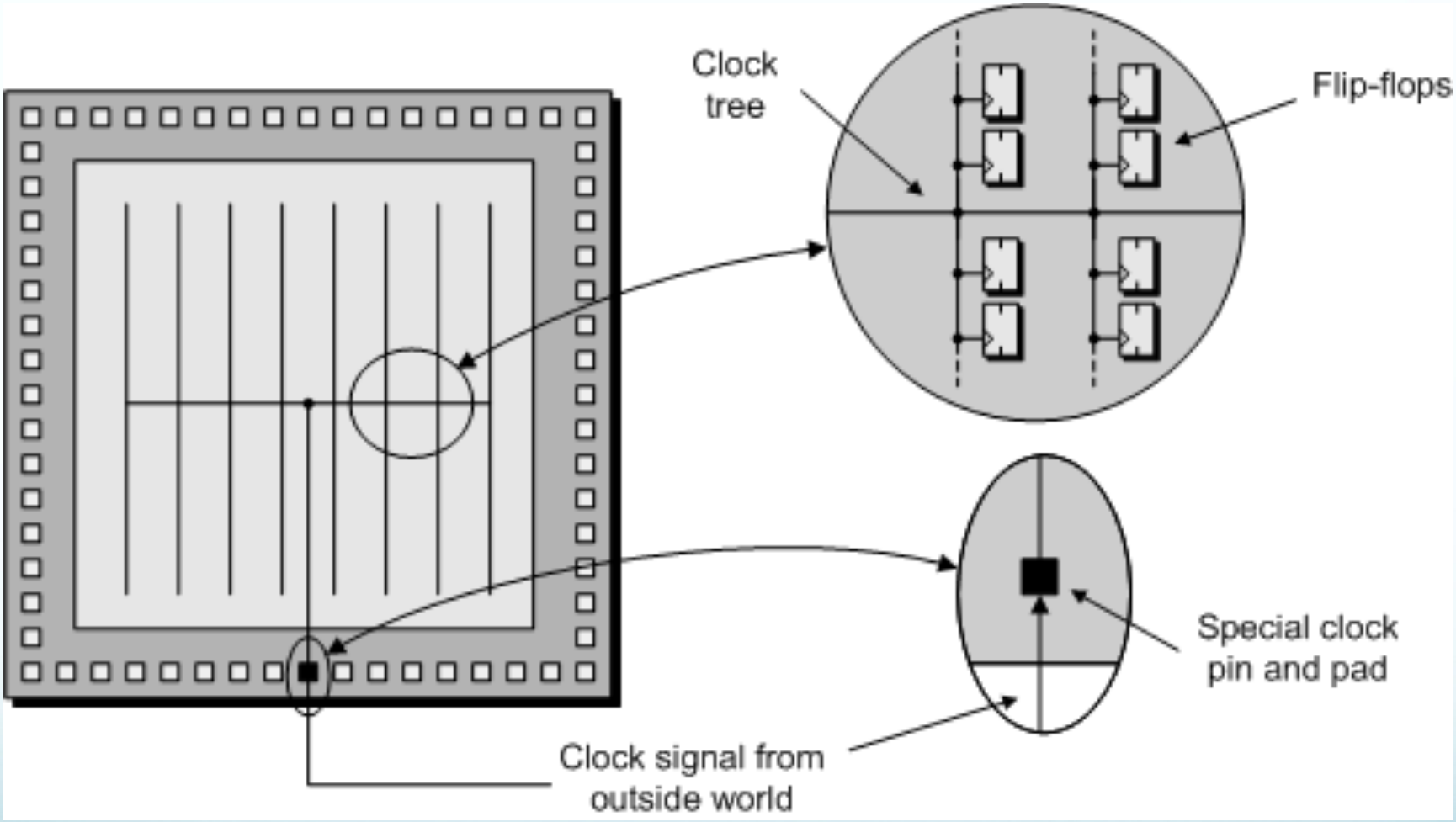
Typical LUT-based Logic Cell



Xilinx: logic cell,
Altera: logic element

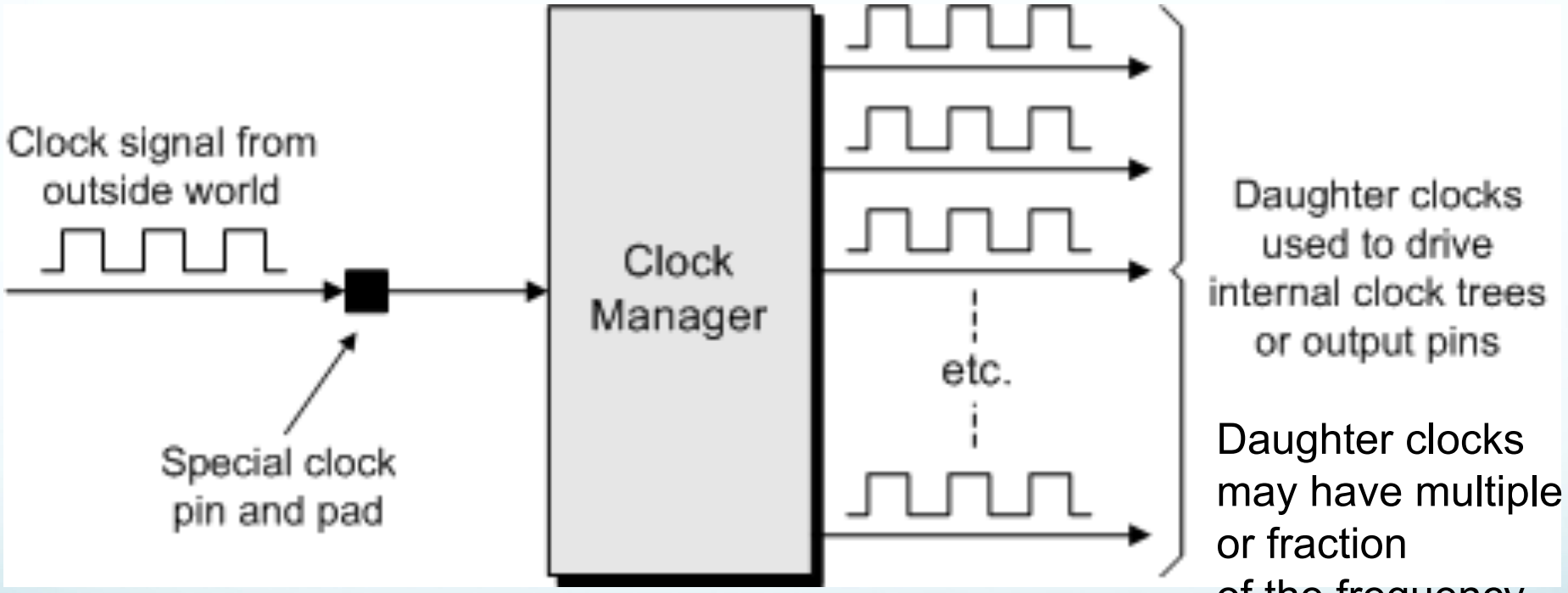
- LUT may implement any function of the inputs
- Flip-Flop registers the LUT output
- May use only the LUT or only the Flip-flop
- LUT may alternatively be configured a shift register
- Additional elements (not shown): fast carry logic

Clock Trees



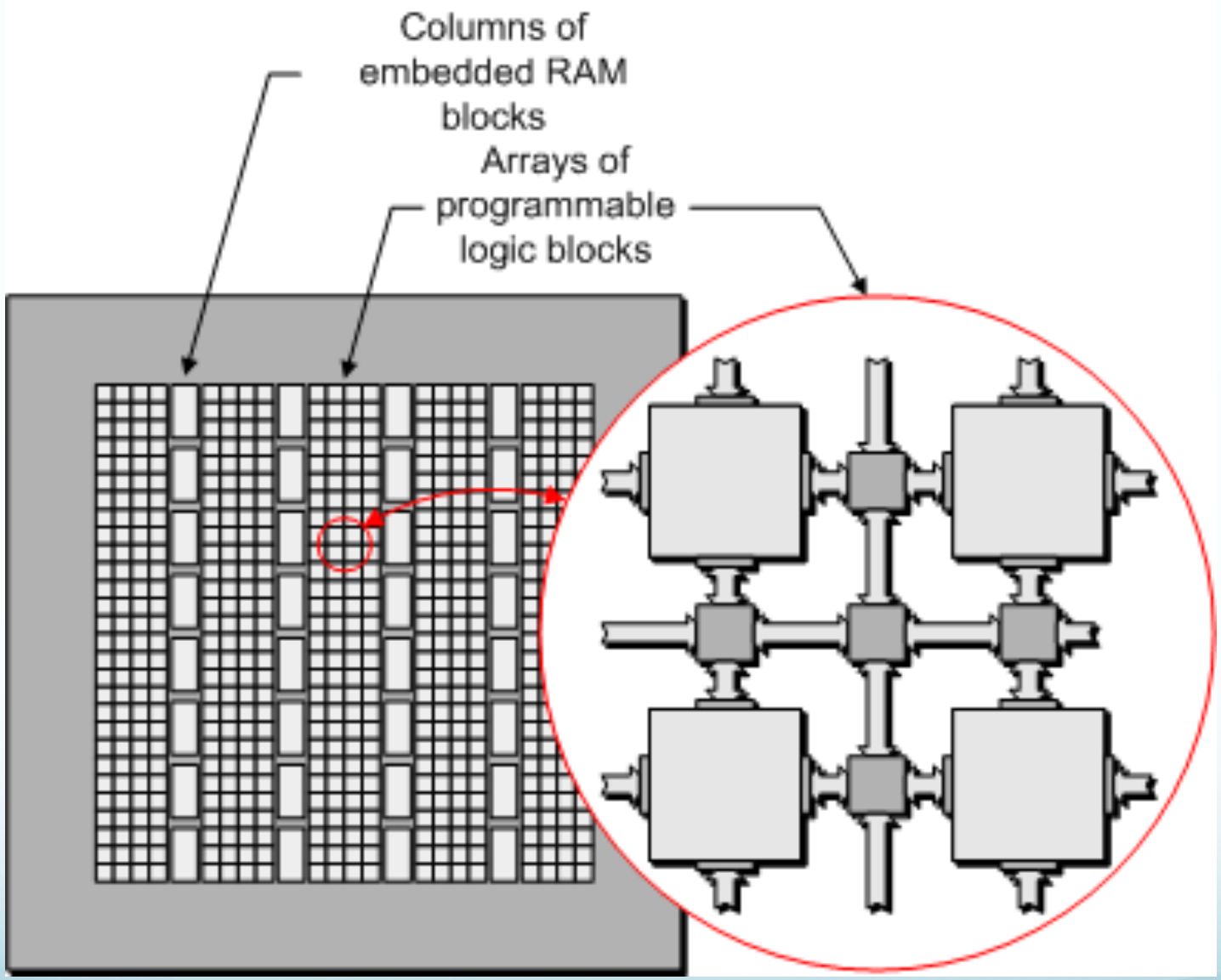
Clock trees guarantee that the clock arrives at the same time at all flip-flops

Clock Managers



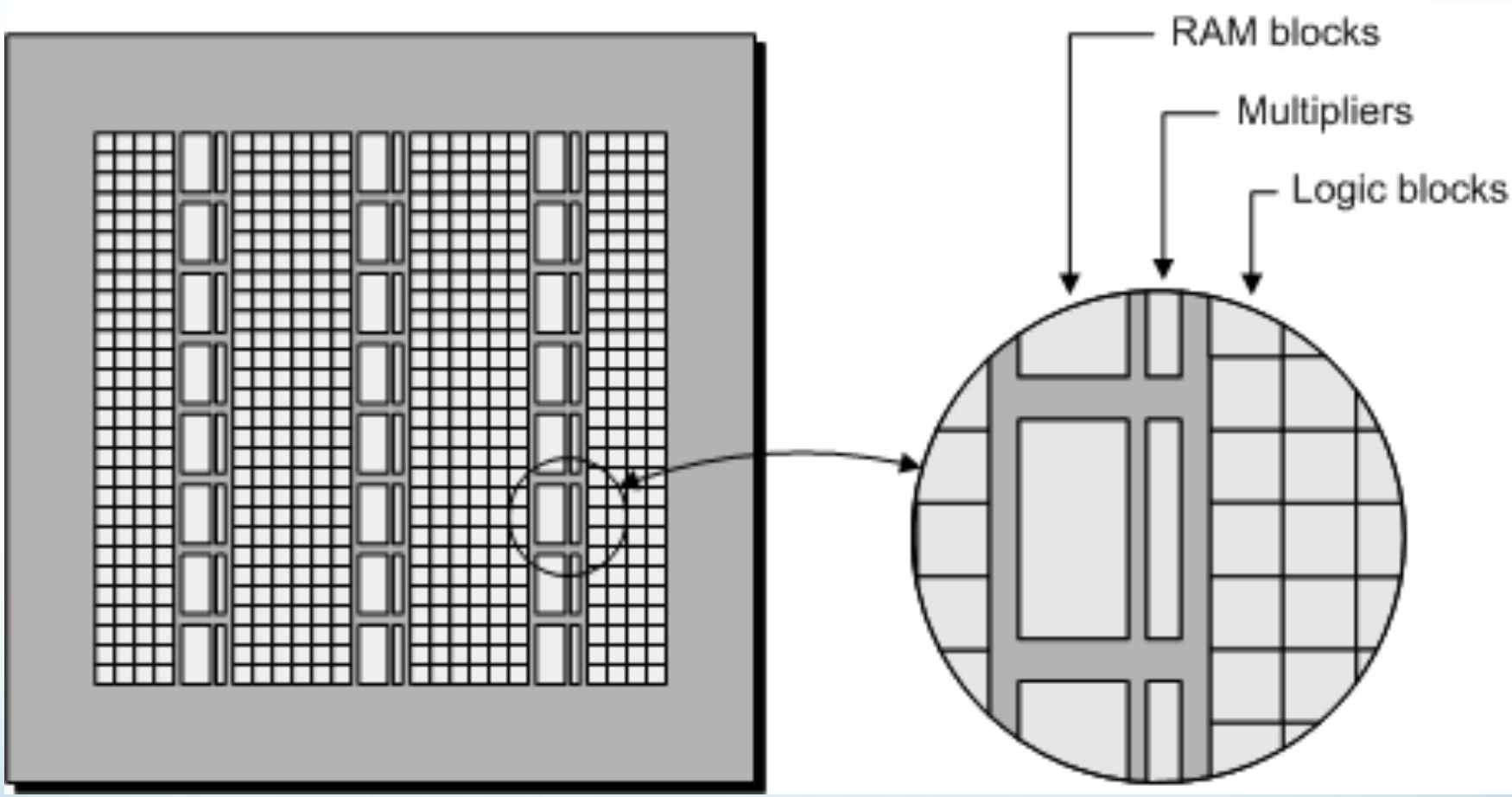
Daughter clocks may have multiple or fraction of the frequency

Embedded RAM blocks

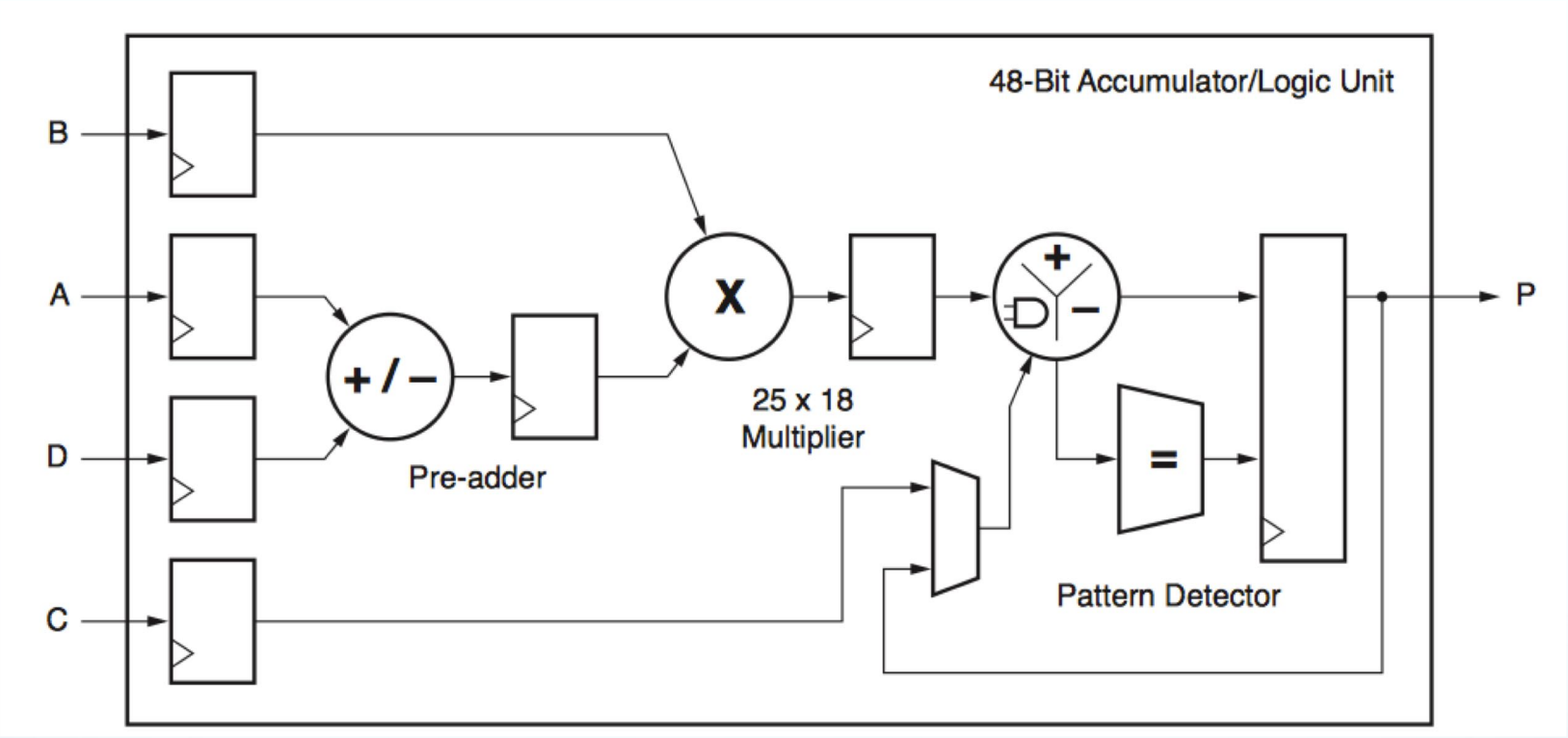


Today: Up to ~500 Mbit of RAM

Embedded Multipliers & DSPs



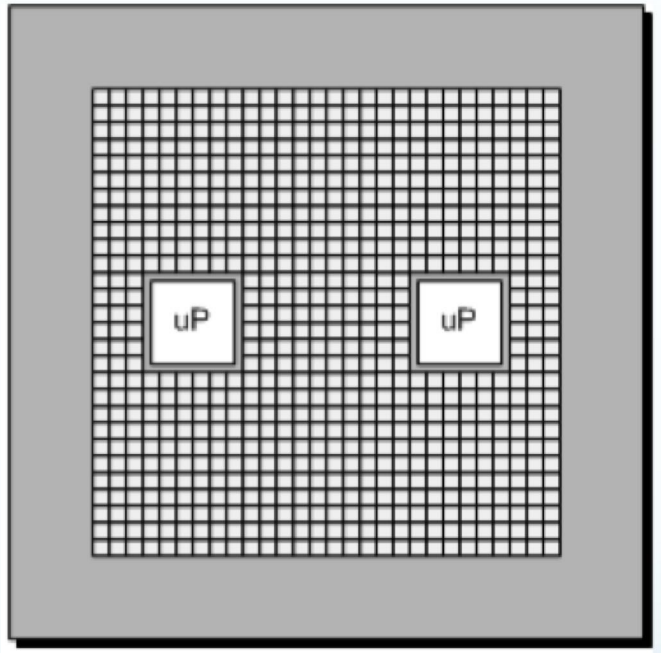
Digital Signal Processor (DSP)



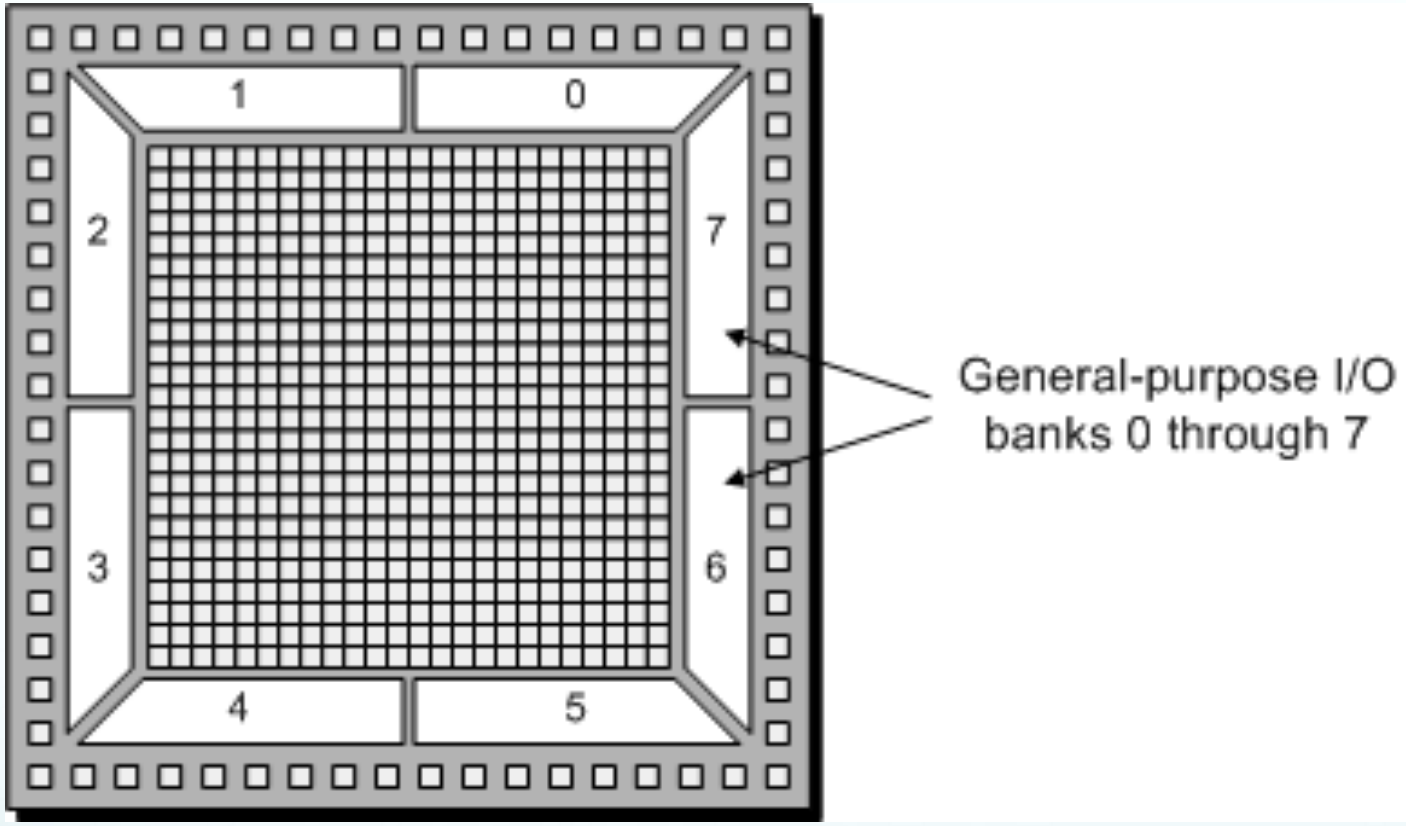
DSP block (Xilinx 7-series)
Up to several 1000 per chip

Soft and Hard Processor Cores

- Soft core
  - Design implemented with the programmable resources (logic cells) in the chip
- Hard core
  - Processor core that is available in addition to the programmable resources
  - E.g.: Power PC, ARM



General-Purpose Input/Output (GPIO)

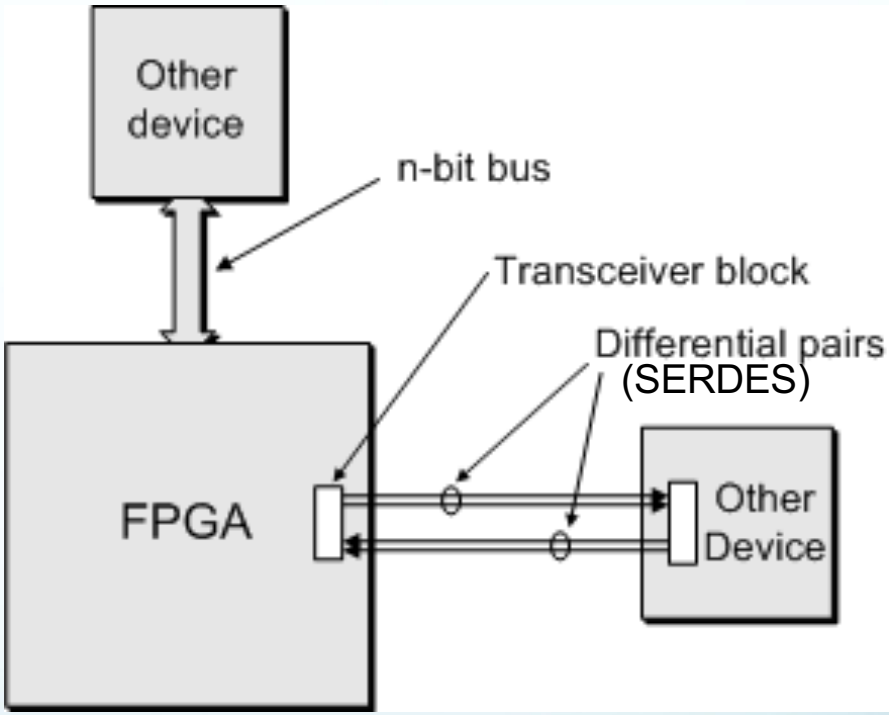


Today: Up to 1200 user I/O pins

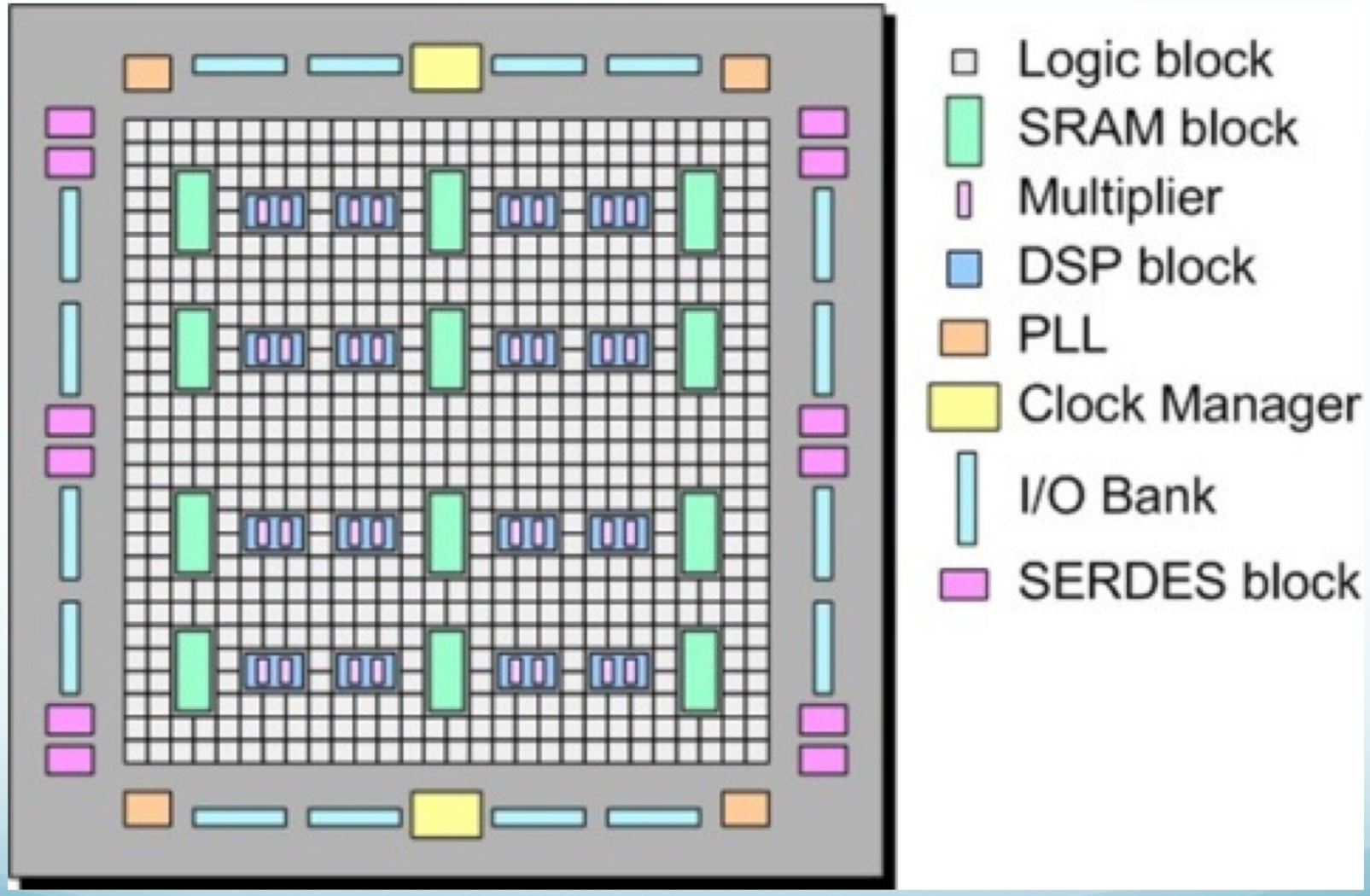
- Input and / or output
- Voltages from (1.0), 1.2 .. 3.3 V
- Many IO standards
- Single-ended: LVTTL, LVCMOS, …
- Differential pairs: LVDS, …

High-Speed Serial Interconnect

- Using differential pairs
- Standard I/O pins limited to about 1 Gbit/s
- Latest serial transceivers: typically 10 Gb/s, 13.1 Gb/s,
  - up to 32.75 Gb/s
  - up to 56 Gb/s with Pulse Amplitude Modulation (PAM)
- FPGAs with multi-Tbit/s IO bandwidth

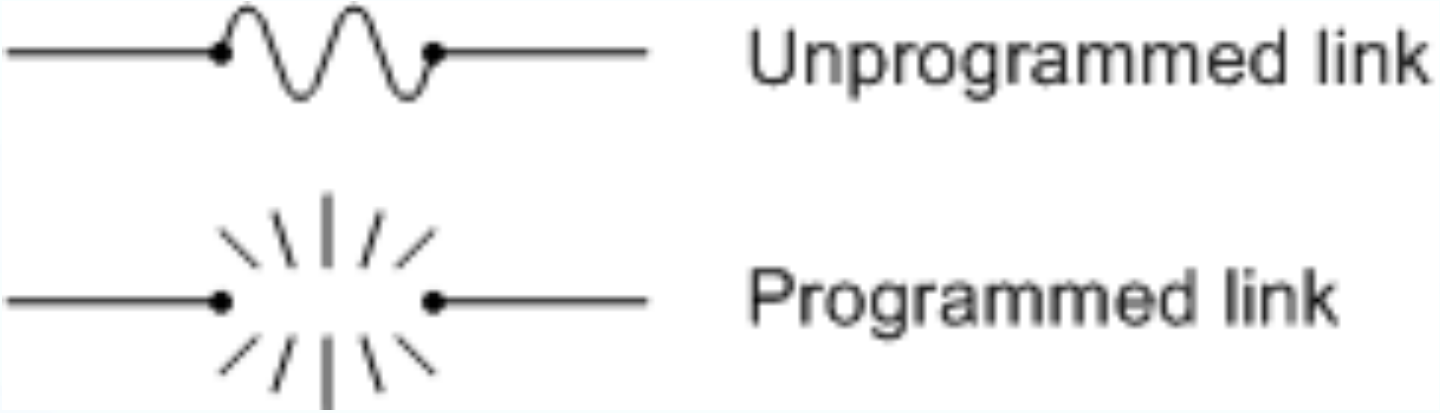


Components in a modern FPGA

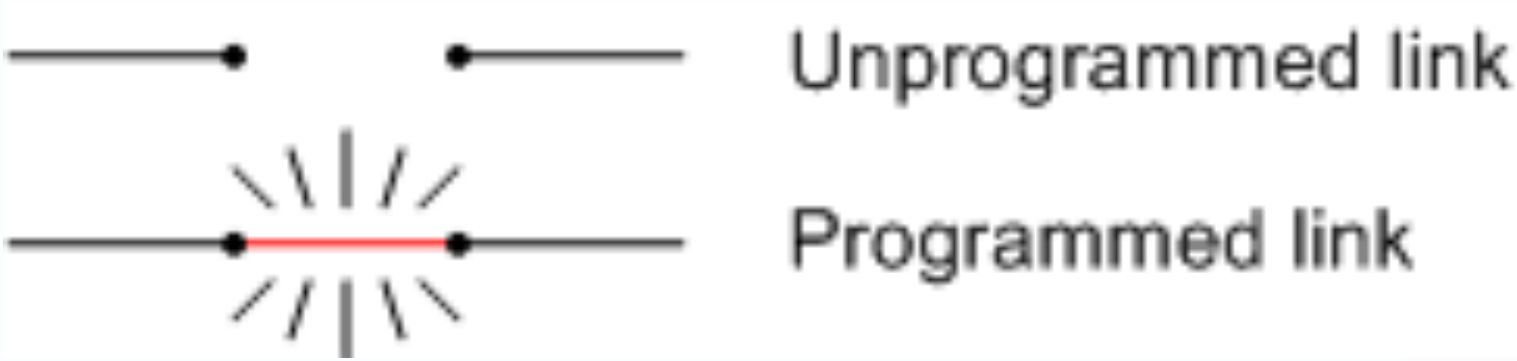


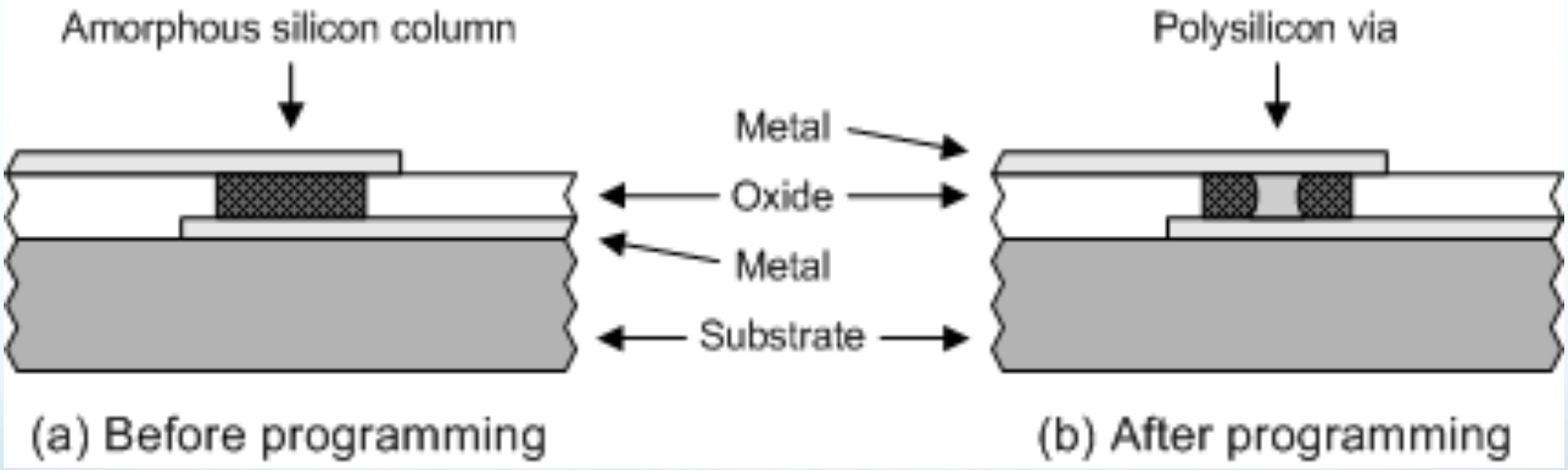
Programming techniques

Fusible Links (not used in FPGAs)



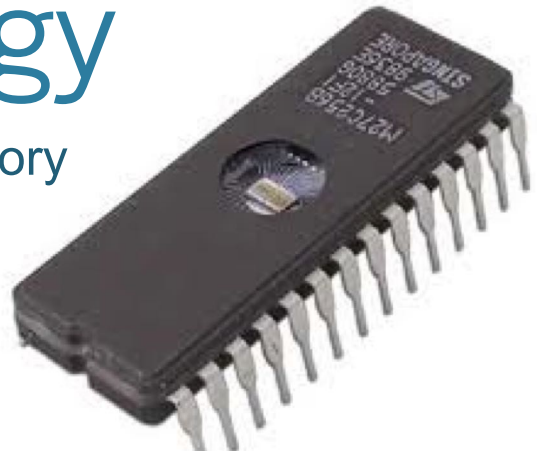
Antifuse Technology

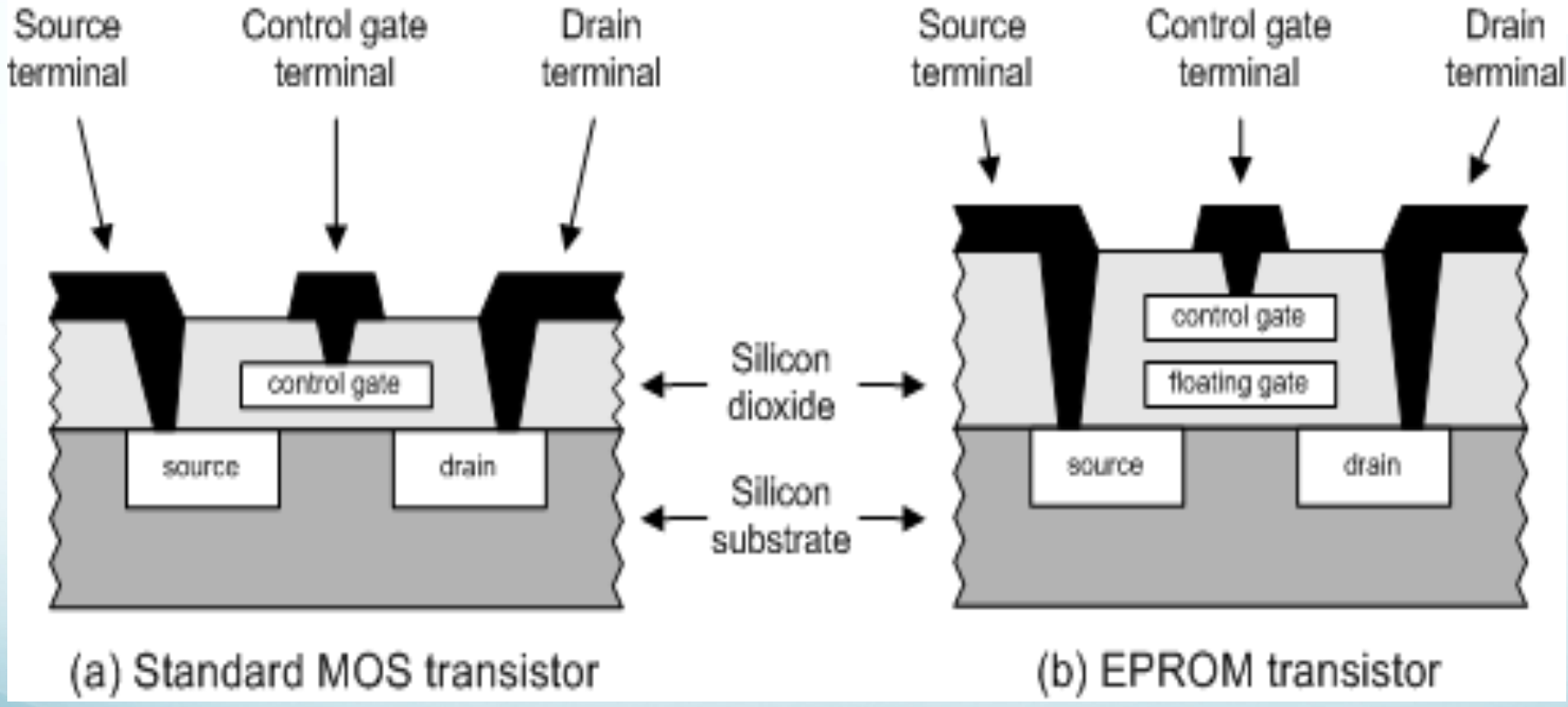




EPROM Technology

Erasable Programmable Read Only Memory

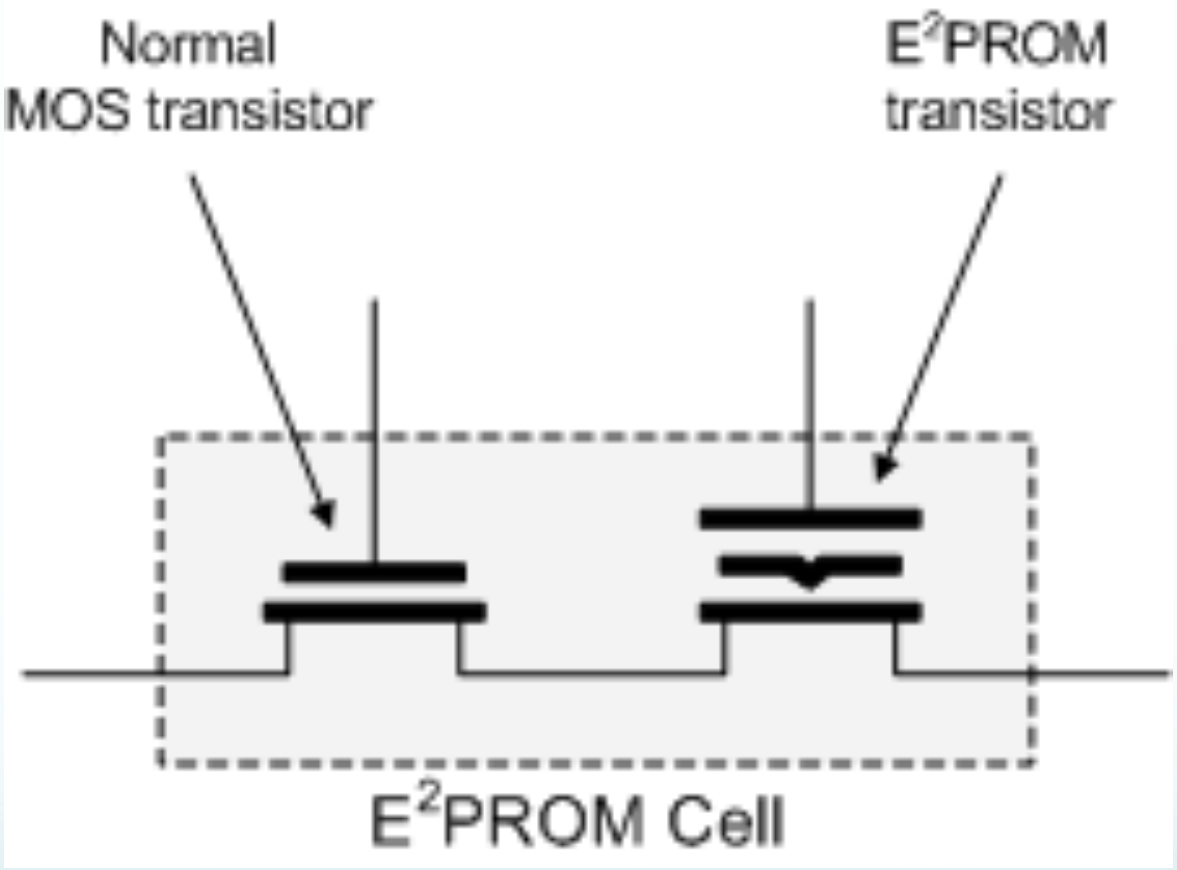




Intel, 1971

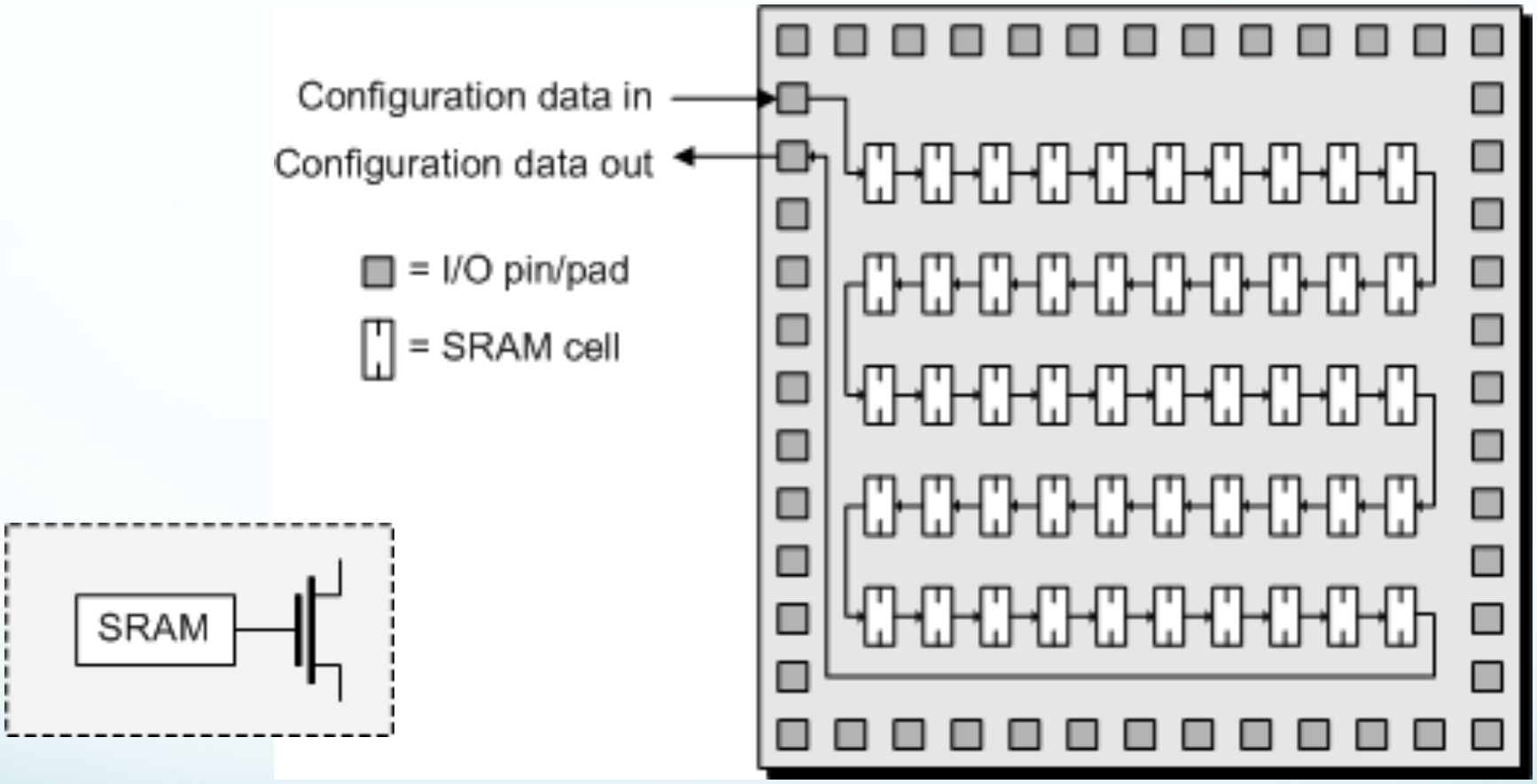
EEPROM and FLASH Technology

Electrically Erasable Programmable Read Only Memory



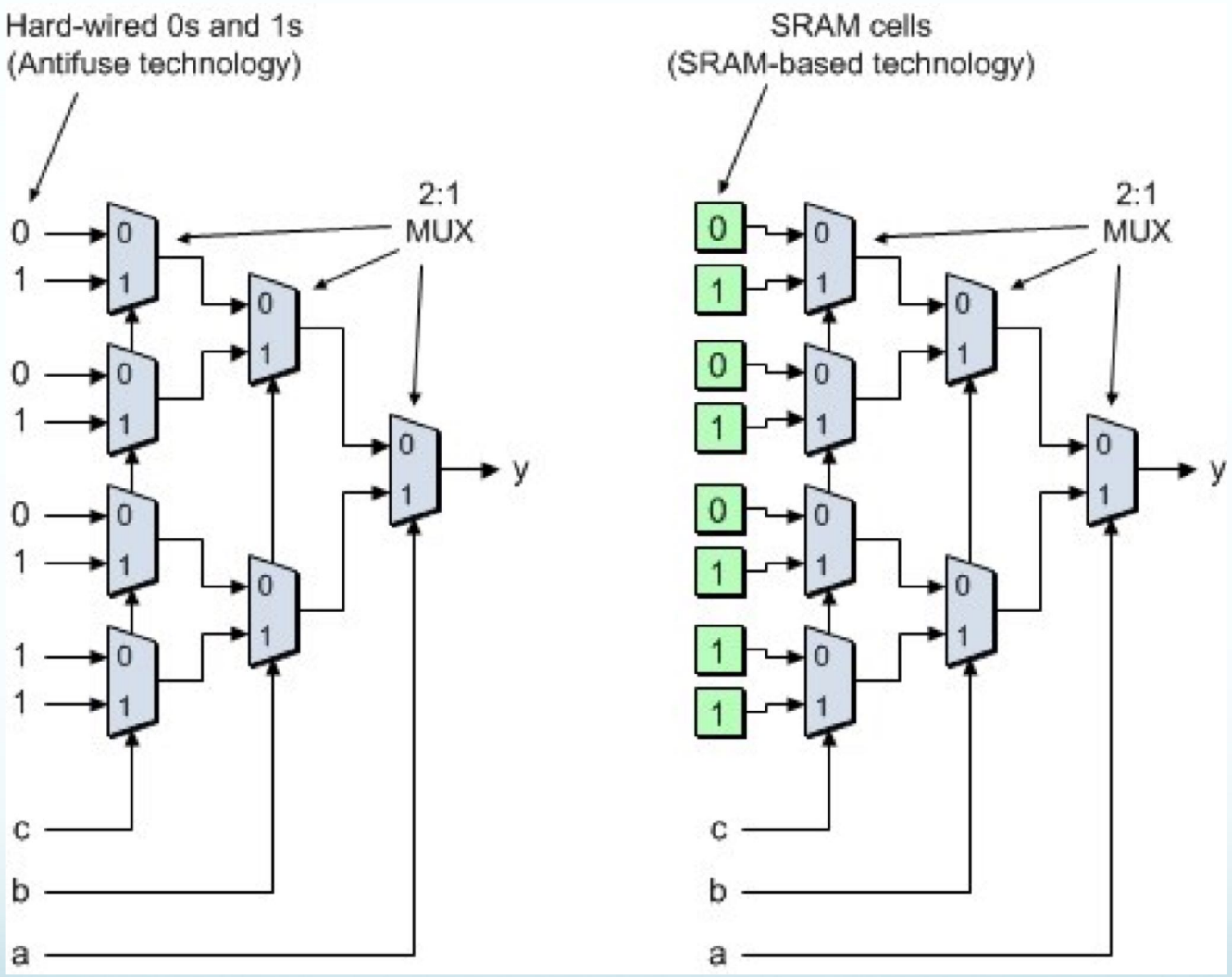
EEPROM: erasable word by word
FLASH: erasable by block or by device

SRAM-Based Devices

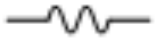
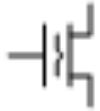


Multi-transistor SRAM cell

Programming a 3-bit wide LUT



Summary of Technologies

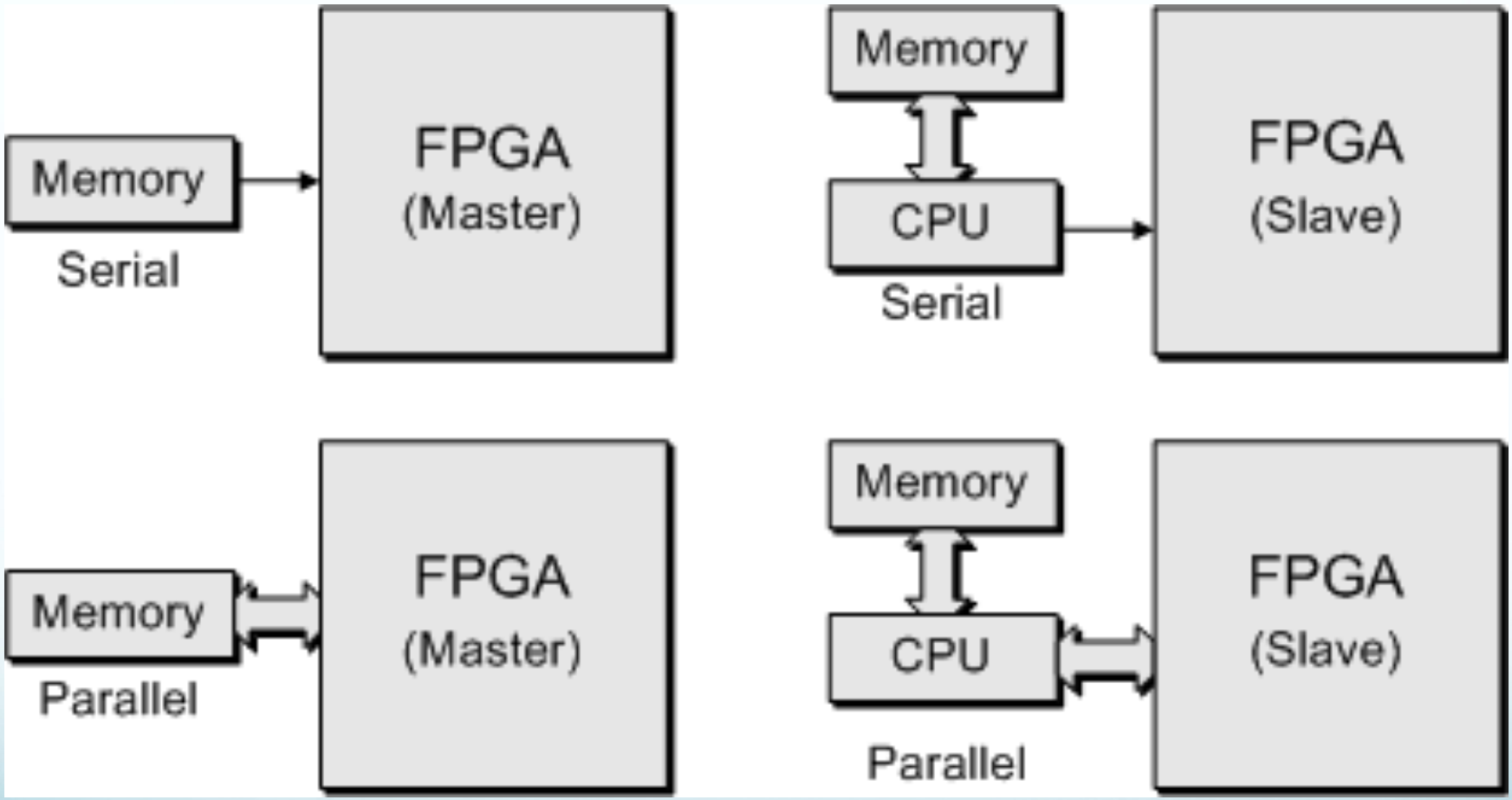
Technology	Symbol	Predominantly associated with ...
Fusible-link		SPLDs
Antifuse		FPGAs
EPROM		SPLDs and CPLDs
E^2PROM/ FLASH		SPLDs, CPLDs, and FPGAs
SRAM		FPGAs (some CPLDs)

Rad-tolerant secure

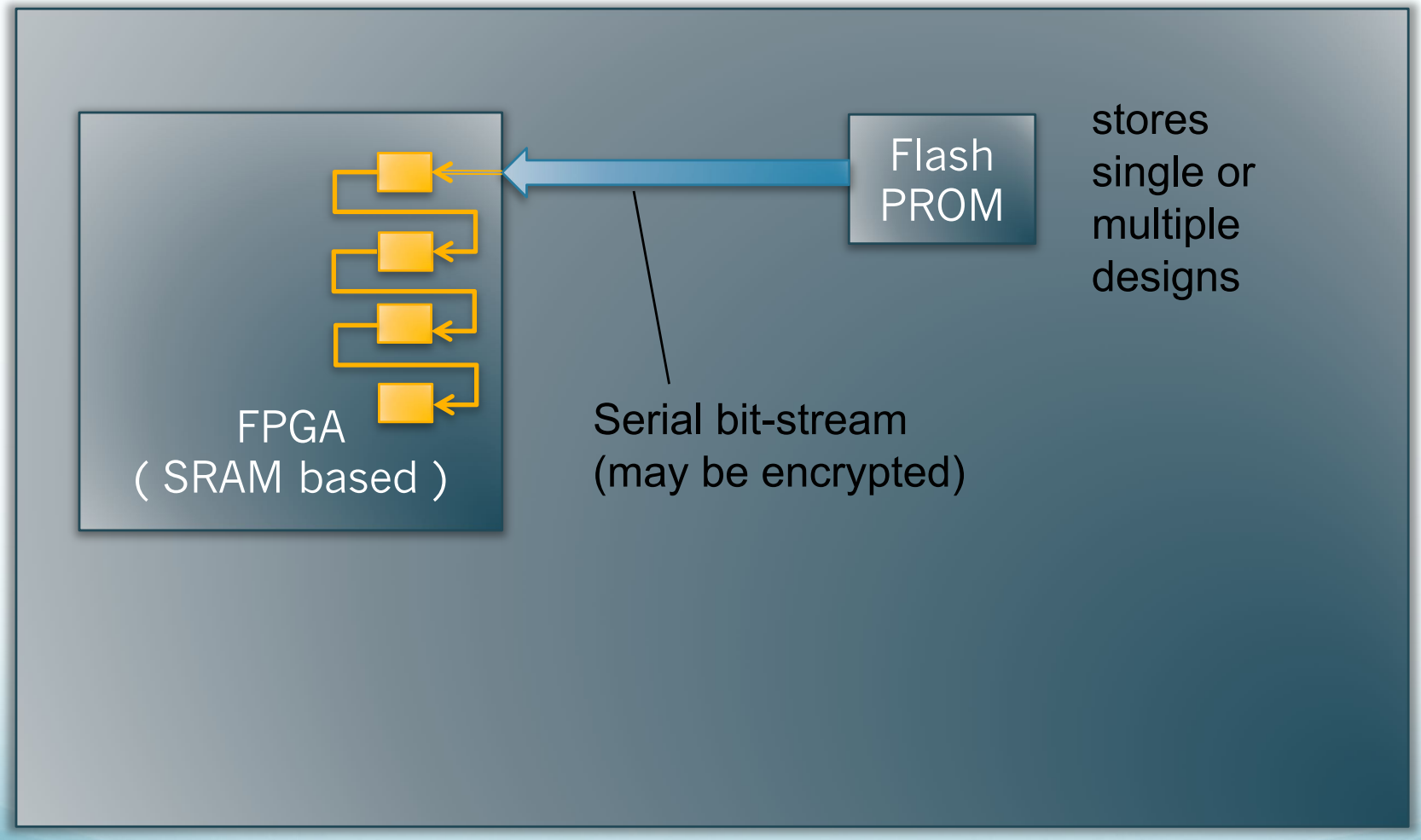
Rad-tolerant (e.g. Alice)

Used in most FPGAs

Design Considerations (SRAM Config.)



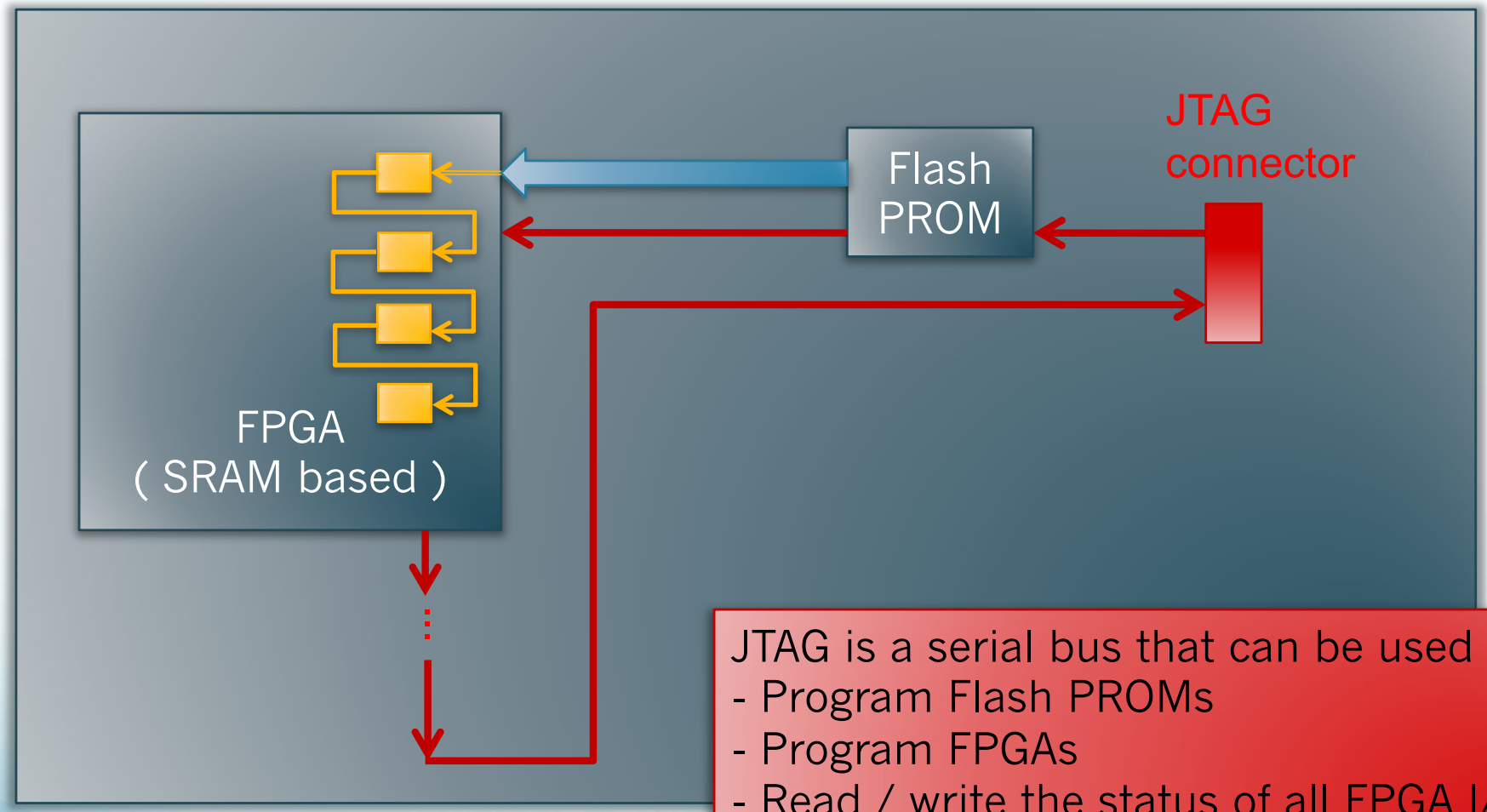
Configuration at power-up



Typical FPGA configuration time: milliseconds

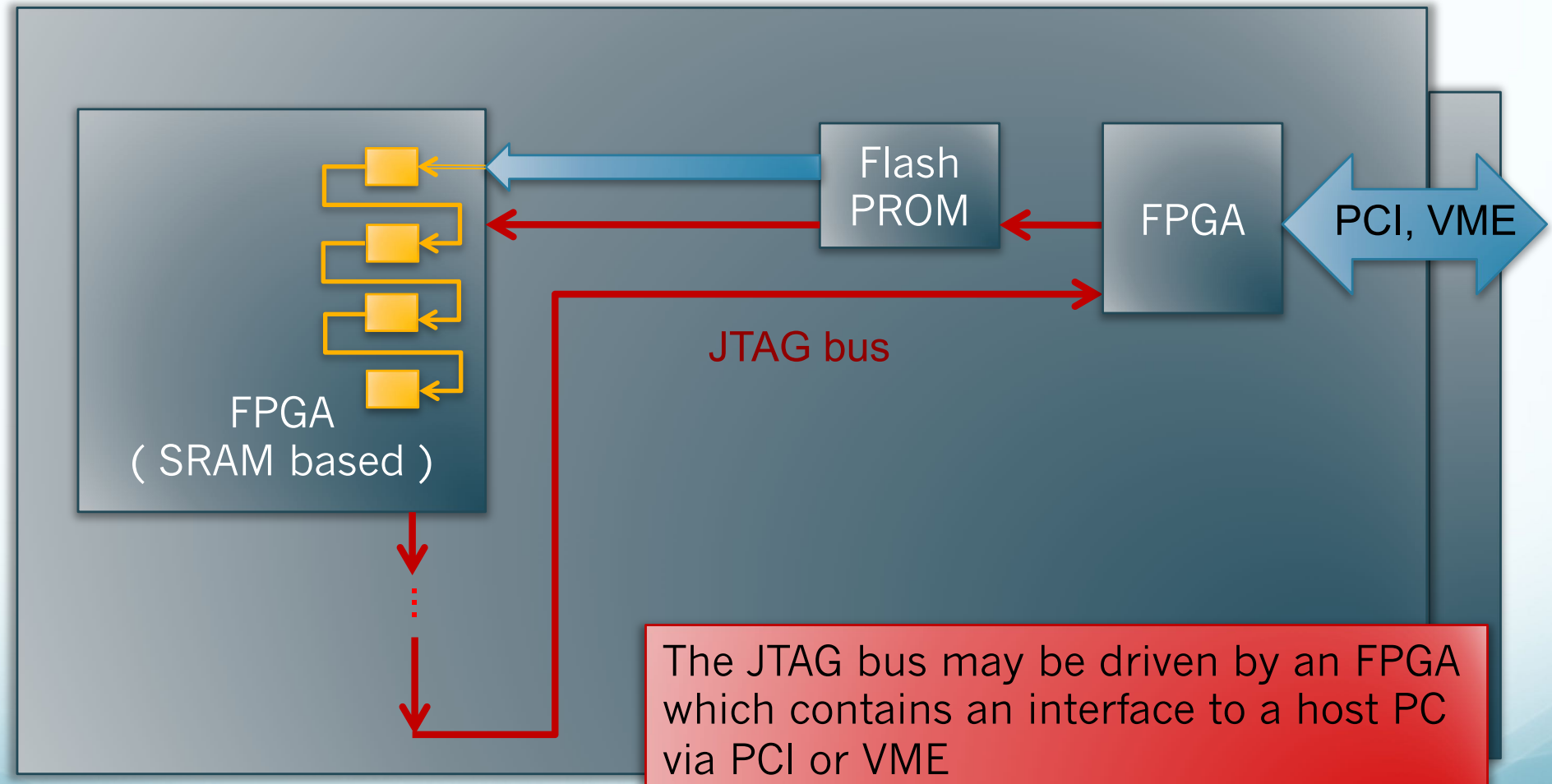
Programming via JTAG

Joint Test Action Group



JTAG is a serial bus that can be used to
- Program Flash PROMs
- Program FPGAs
- Read / write the status of all FPGA I/Os
  (= Boundary scan)

Remote programming



The JTAG bus may be driven by an FPGA which contains an interface to a host PC via PCI or VME

gateware can then be updated remotely

Major Manufacturers

- Xilinx
  - First company to produce FPGAs in 1985
  - About 55% market share, today
  - SRAM based CMOS devices

- Intel FPGA (formerly Altera)
  - About 35% market share
  - SRAM based CMOS devices

- Microsemi (Actel)
  - Anti-fuse FPGAs
  - Flash based FPGAs
  - Mixed Signal

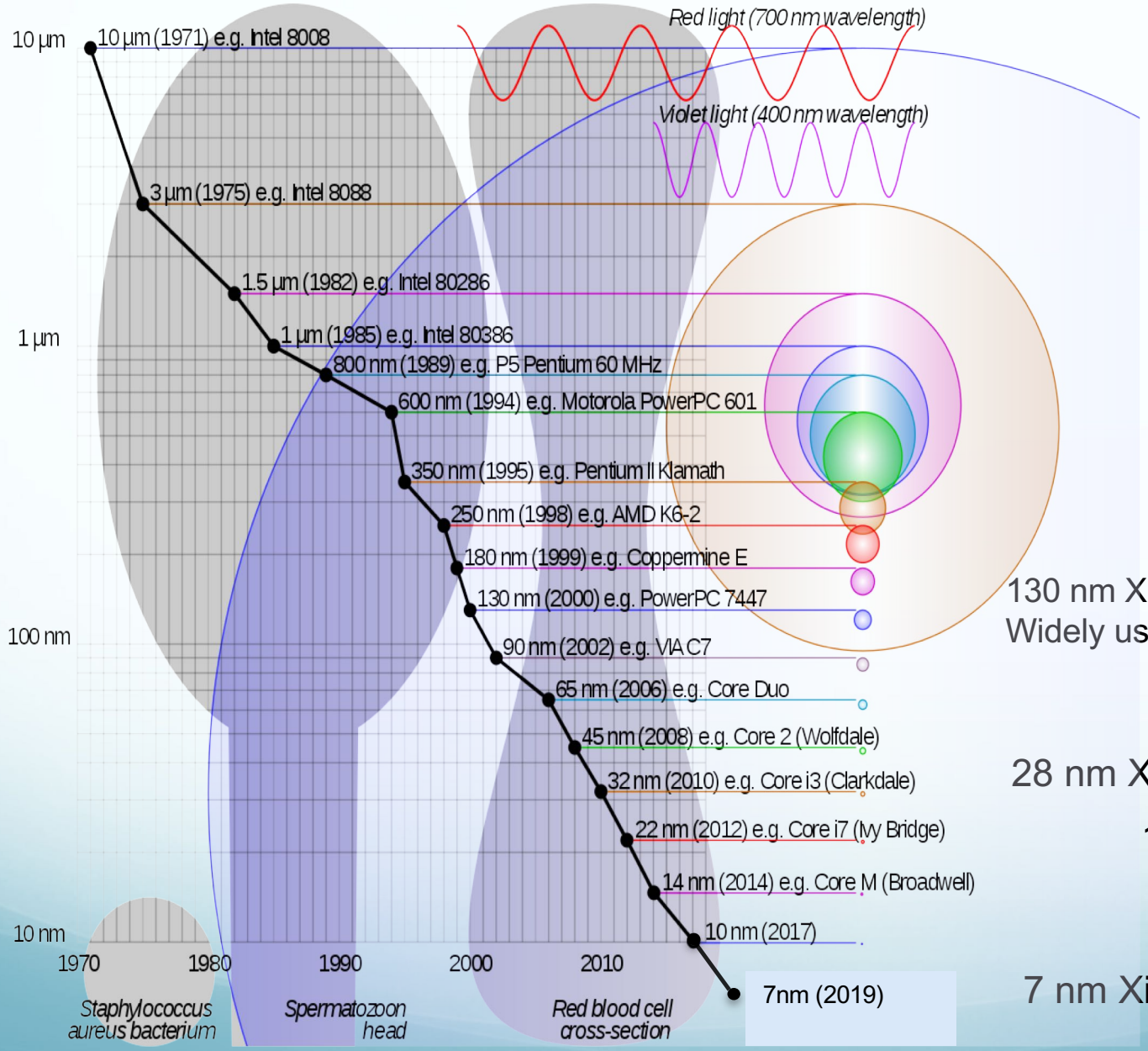
(Formerly 

)

- Lattice Semiconductor
  - SRAM based with integrated Flash PROM
  - low power

Trends

Ever-decreasing feature size



- Higher capacity
- Higher speed
- Lower power consumption

130 nm Xilinx Virtex-2
Widely used at LHC startup

28 nm Xilinx Virtex-7 / Altera Stratix V

16 nm Xilinx UltraScale +

14 nm Intel Stratix 10

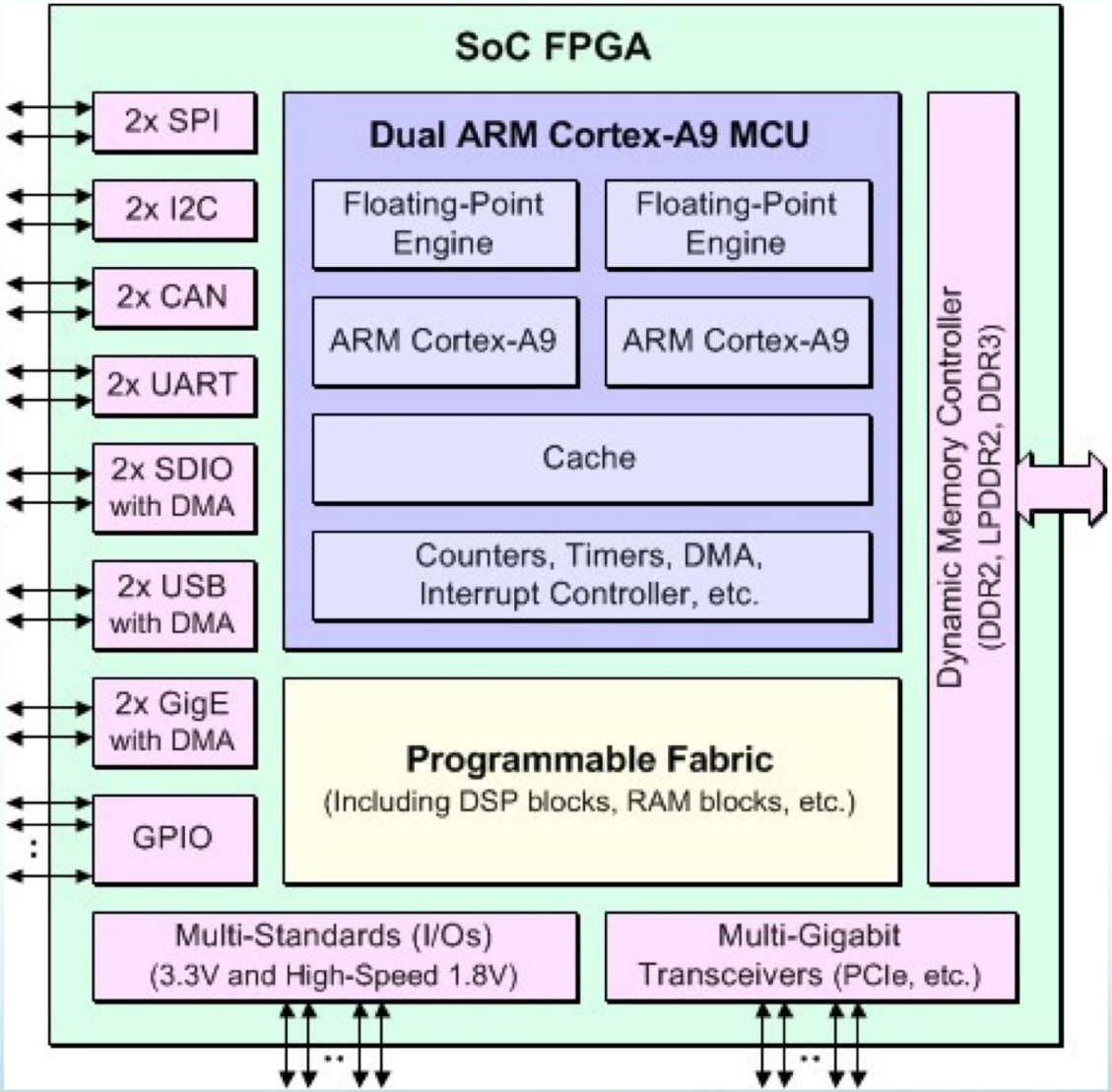
7 nm Xilinx Versal ACAP(*)

(*) Adaptive Compute Acceleration Platform

Trends

- Speed of logic increasing
- Look-up-tables with more inputs (5 or 6)
- Speed of serial links increasing (multiple Gb/s)
- More integrated memory
  - Integrated High Bandwidth Memory (HBM) in-package
    - 10x faster than DDR4 (Xilinx: up to 8 GB, Intel: up to 16GB)
- Additional Flip Flops in routing resources (Intel hyperflex)
- More and more hard macro cores on the FPGA
  - PCI Express
    - Gen2: 5 Gb/s per lane
    - Gen3: 8 Gb/s per lane (typically up to 16 lanes)
    - Gen4: 16 Gb/s per lane
  - 10 Gb/s, 40 Gb/s, 100 Gb/s Ethernet, 150 Gb/s Interlaken
- Sophisticated soft macros
  - CPUs
  - Gb/s MACs
  - Memory interfaces (DDR2/3/4)
- Processor-centric architectures – see next slide

System-On-a-Chip (SoC) FPGAs



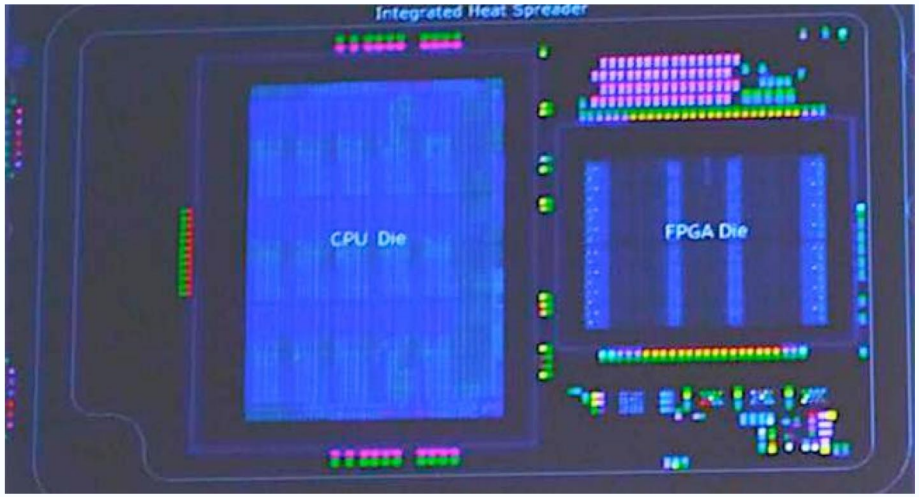
Xlinix Zynq

Intel Stratix 10 SoC

CPU(s) + Peripherals + FPGA in one package

FPGAs in Server Processors and the Cloud

- Released 2018: Intel Xeon Server Processor with FPGA in socket
  - Intel acquired Altera in 2015



  - See: https://www.eejournal.com/article/intel-delivers-xeon-scalable-processor-6138p-with-arria-10-gx-1150-fpga/

- FPGAs in the cloud
  - Amazon Elastic Cloud F1 instances
    - 8 CPUs / 1 Xilinx UltraScale+ FPGA
    - 64 CPUs / 8 Xilinx UltraScale+ FPGA

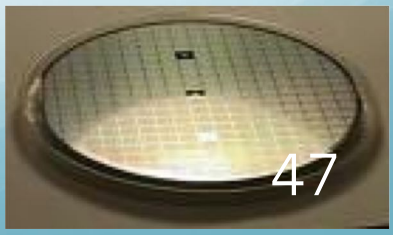
FPGA – ASIC comparison

FPGA

- Rapid development cycle (minutes / hours)
- May be reprogrammed in the field (gateware upgrade)
  - New features
  - Bug fixes
- Low development cost
  - You can get started with a development board (< $100) and free software
- High-end FPGAs rather expensive

ASIC

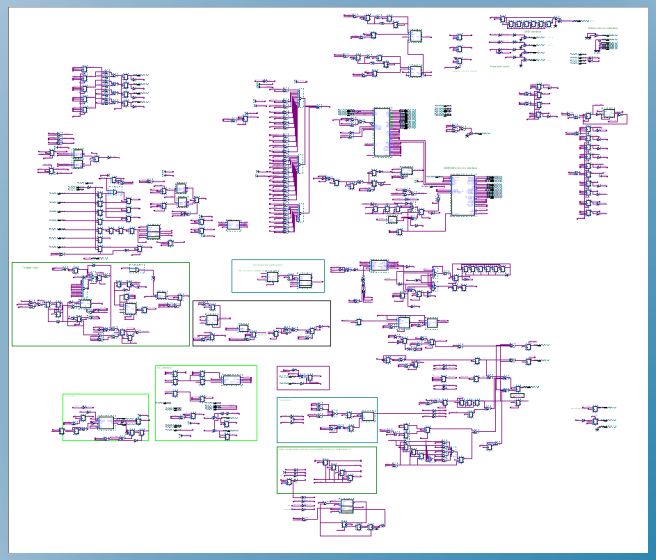
- Higher performance
  - Speed, Area, Power
- Analog designs possible
- Better radiation hardness
- Long development cycle (weeks / months)
- Design cannot be changed once it is produced
- Extremely high development cost
  - ASICs are produced at a semiconductor fabrication facility ("fab") according to your design
- Lower cost per device compared to FPGA, when large quantities are needed



FPGA development

Design entry

Schematics



- Graphical overview
- Can draw entire design
- Use pre-defined blocks

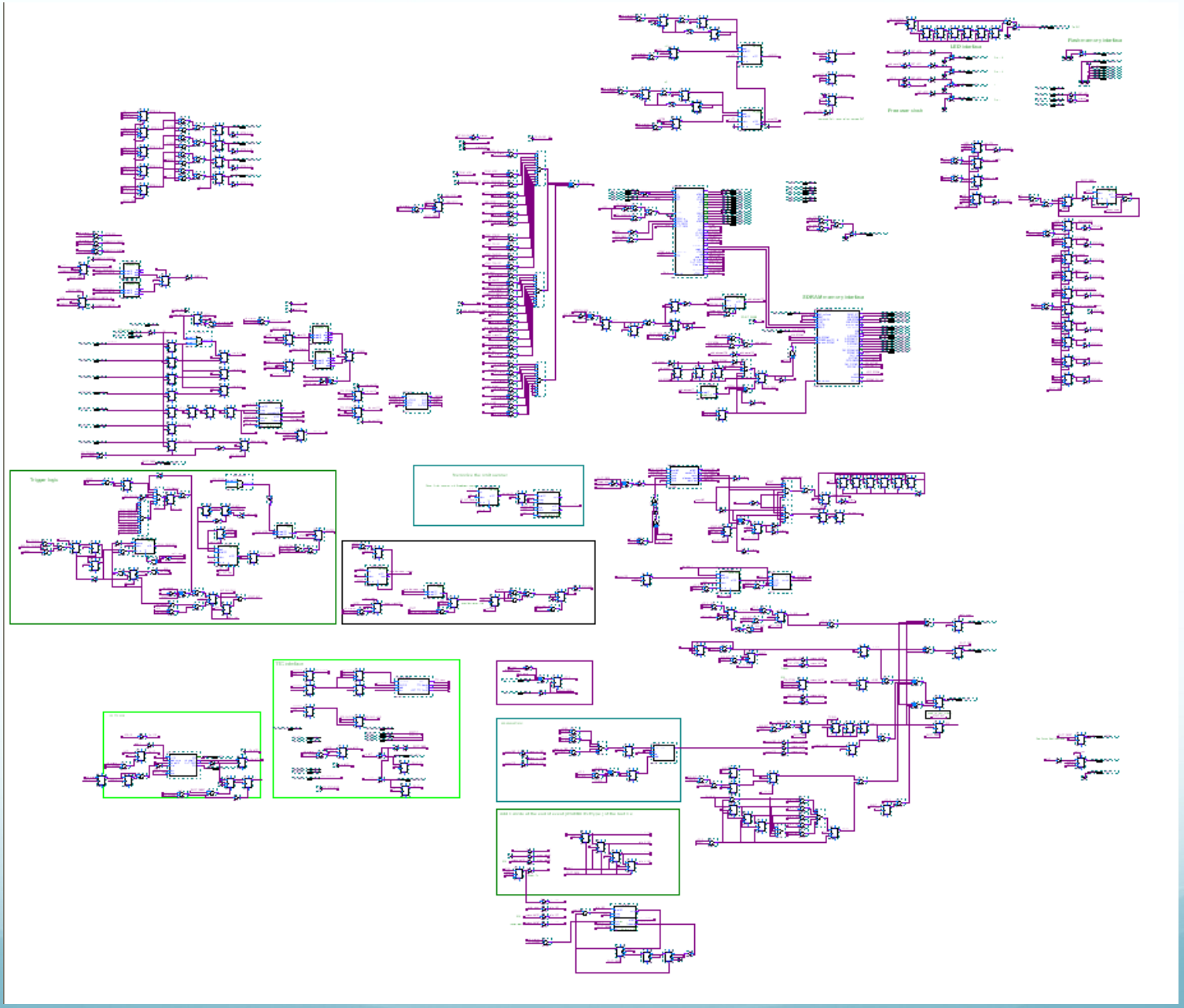
Hardware description language
VHDL, Verilog

```
entity DelayLine is

  generic (
    n_halfcycles : integer := 2);

  port (
    x         : in std_logic_vector;
    x_delayed : out std_logic_vector;
    clk       : in std_logic);

end entity DelayLine;
```

- Can generate blocks using loops
- Can synthesize algorithms
- Independent of design tool
- May use tools used in SW development (SVN, git …)

Mostly a personal choice depending on previous experience

Schematics



Hardware Description Language

- Looks similar to a programming language
  - BUT be aware of the difference
    - Programming Language => translated into machine instructions that are executed by a CPU
    - HDL => translated into gateware (logic gates & flip-flops)
- Common HDLs
  - VHDL
  - Verilog
  - AHDL (Altera specific)
- Newer trends
  - C-like languages (handle-C, System C)
  - Labview
  - High Level Synthesis (HLS) from C/C++

Example: VHDL

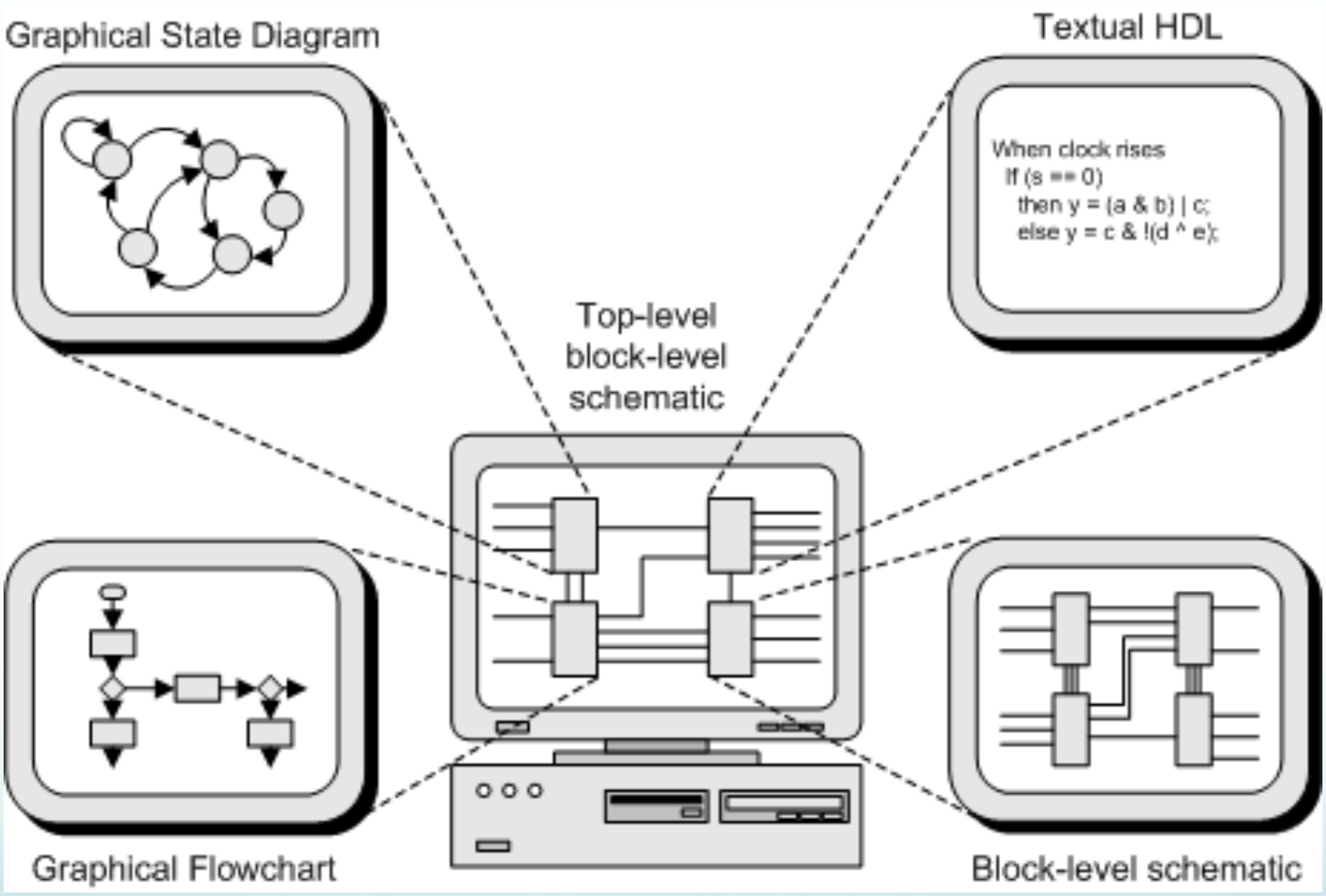
```
architecture behavioral of VMEReg is

  signal vme_en_i   : std_logic;
  signal Q : std_logic_vector(15 downto 0);

begin  -- behavioral

  vme_addr_decode : process (vme_addr, vme_en) is
    variable my_addr_vec : std_logic_vector(vme_addr'high downto 0);
    variable selected    : boolean;
  begin  -- process vme_addr_decode
    my_addr_vec := std_logic_vector( TO_UNSIGNED ( my_vme_base_address, vme_addr'high+1 ) );
    selected    := my_addr_vec(vme_addr'high downto 1) = vme_addr(vme_addr'high downto 1);
    vme_en_i <= '0' ;
    if selected then
      vme_en_i <= vme_en;
    end if;
  end process vme_addr_decode;

  reg: process (vme_clk, reset) is
  begin  -- process reg
    if reset = '1' then                 -- asynchronous reset
        Q <= init_val;
        vme_en_out <= '0';
    elsif vme_clk'event and vme_clk = '1' then  -- rising clock edge
      vme_en_out <= vme_en_i;
      if vme_en_i = '1' and vme_wr = '1' then
        Q <= vme_data;
      end if;
    end if;
  end process reg;

  data <= Q;
  vme_data_out <= Q;

end behavioral;
```

Asynchronous logic
All signals in sensitivity list

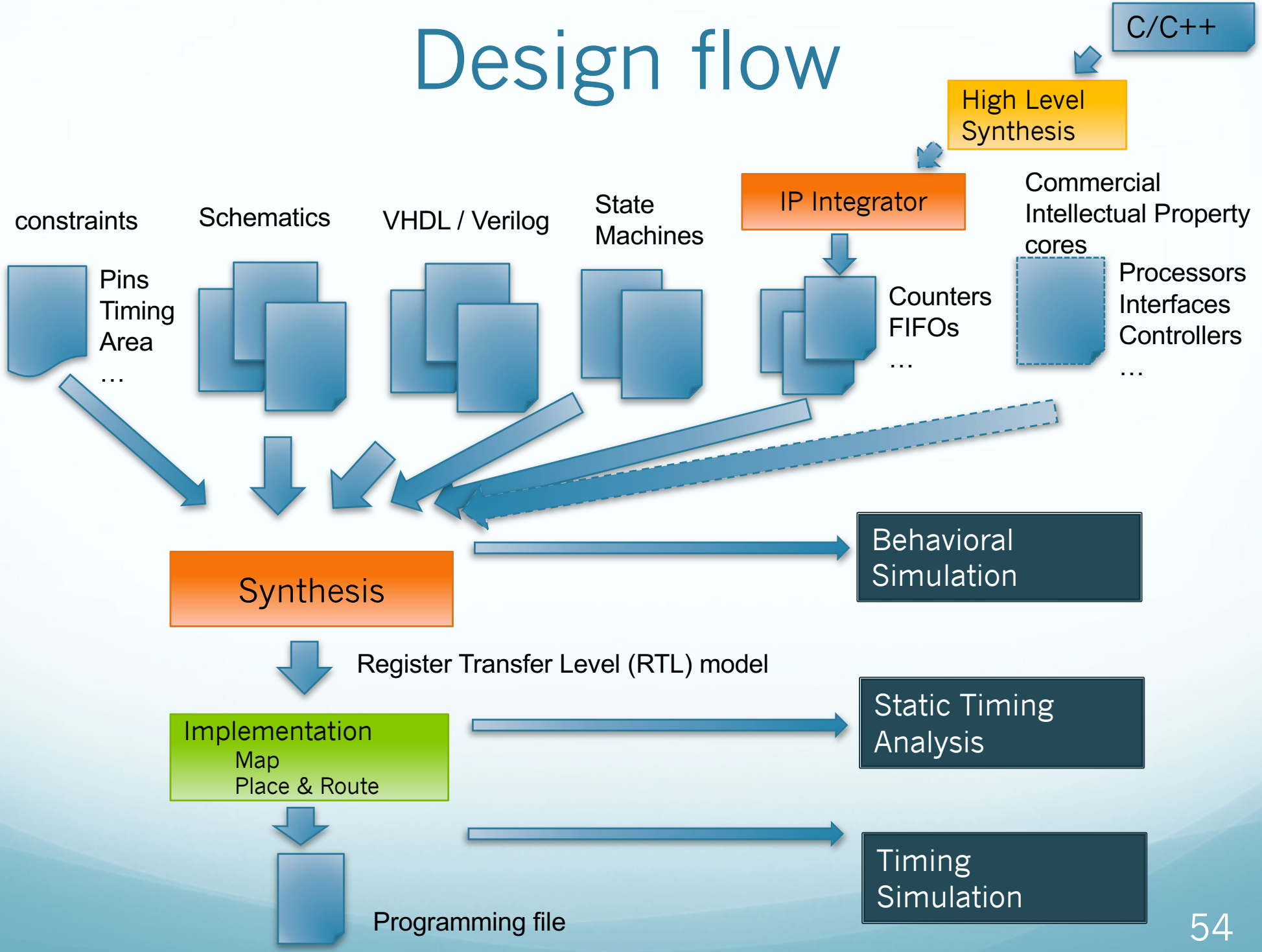
Synchronous logic
Only clock (and reset) in sensitivity list

- Looks like a programming language
- All statements executed in parallel, except inside processes

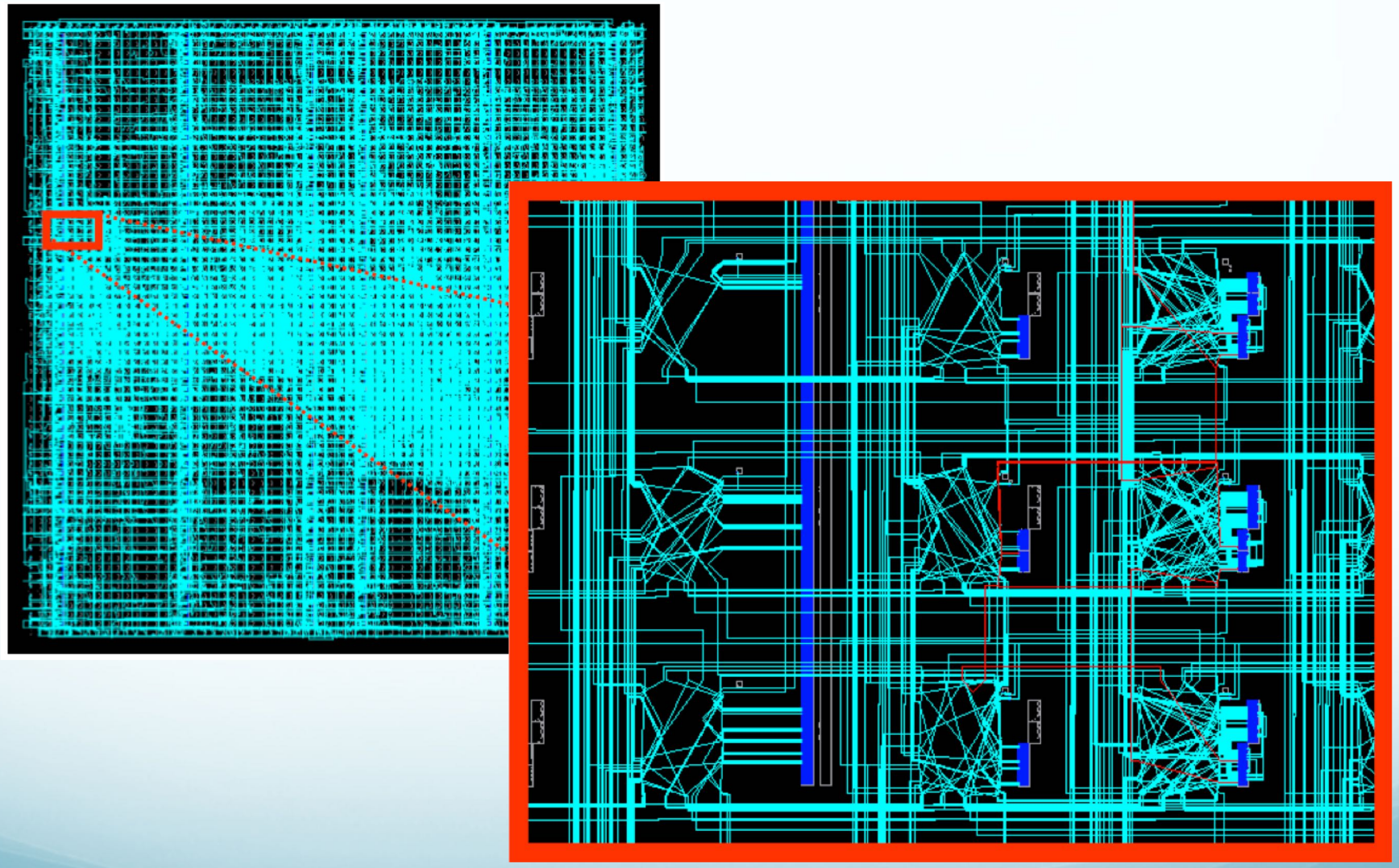
Schematics & HDL combined



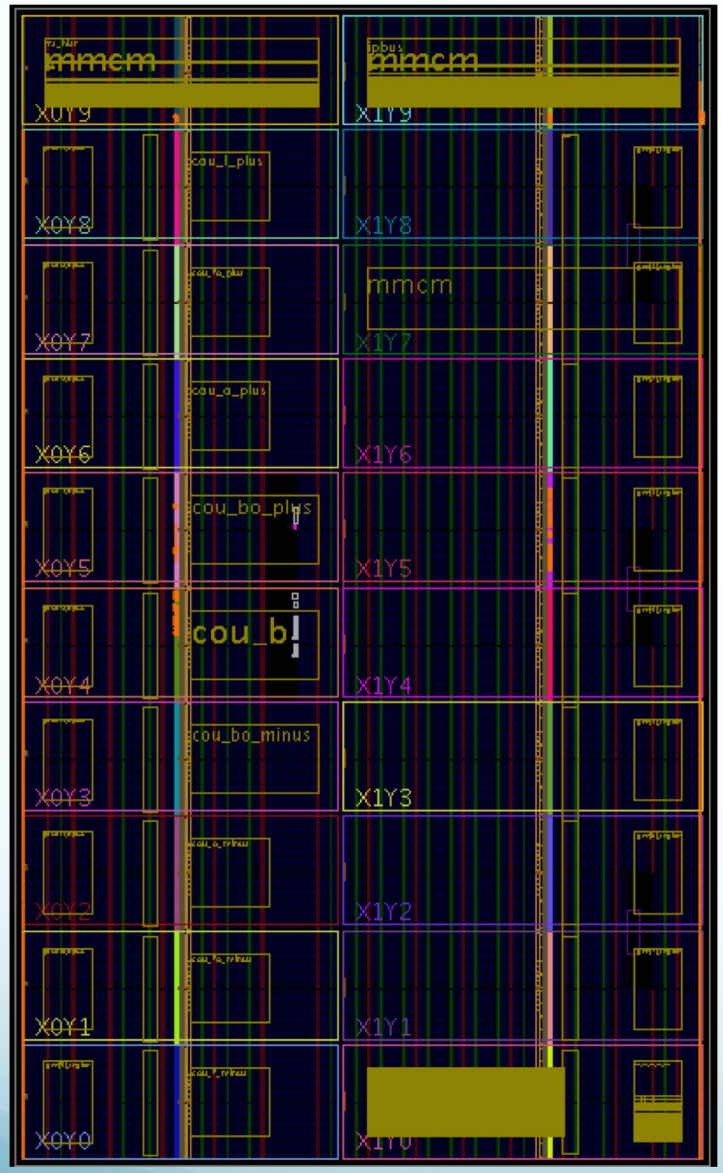
Design flow


C/C++
High Level Synthesis
IP Integrator
Commercial Intellectual Property cores
constraints
Schematics
VHDL / Verilog
State Machines
Pins
Timing
Area
…
Counters
FIFOs
…
Processors
Interfaces
Controllers
…
Synthesis
Behavioral Simulation
Register Transfer Level (RTL) model
Implementation
Map
Place & Route
Static Timing Analysis
Programming file
Timing Simulation

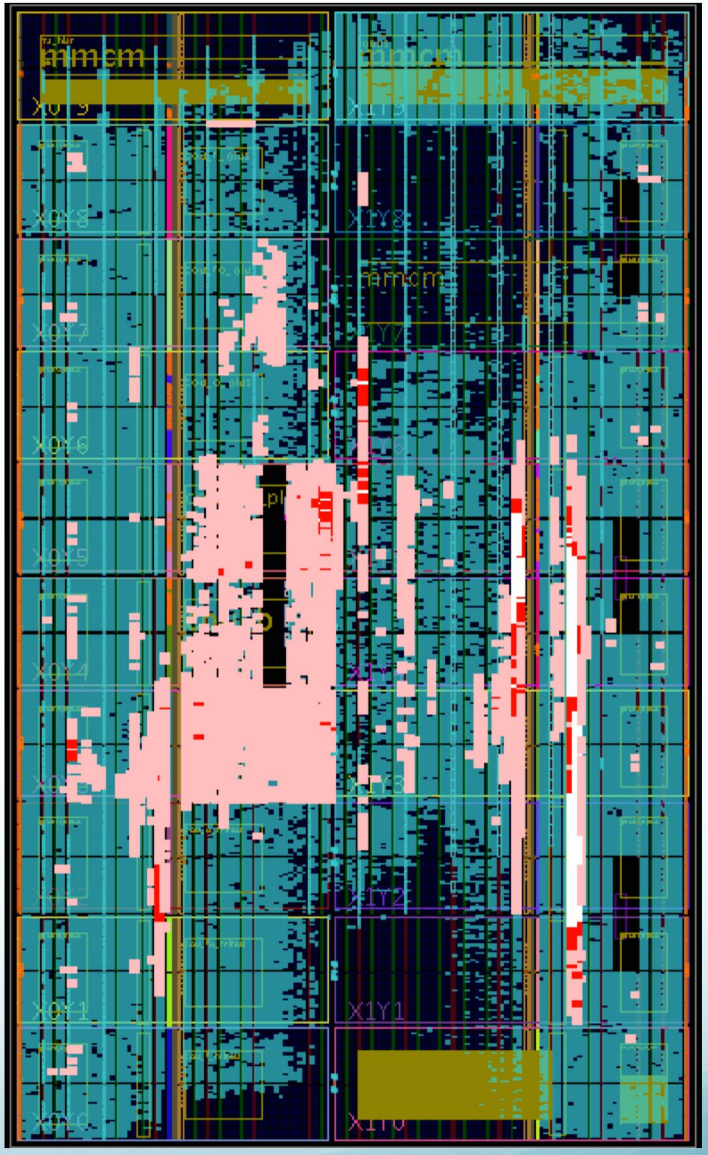
Floorplan (Xlinx Virtex 2)



Manual Floor planning

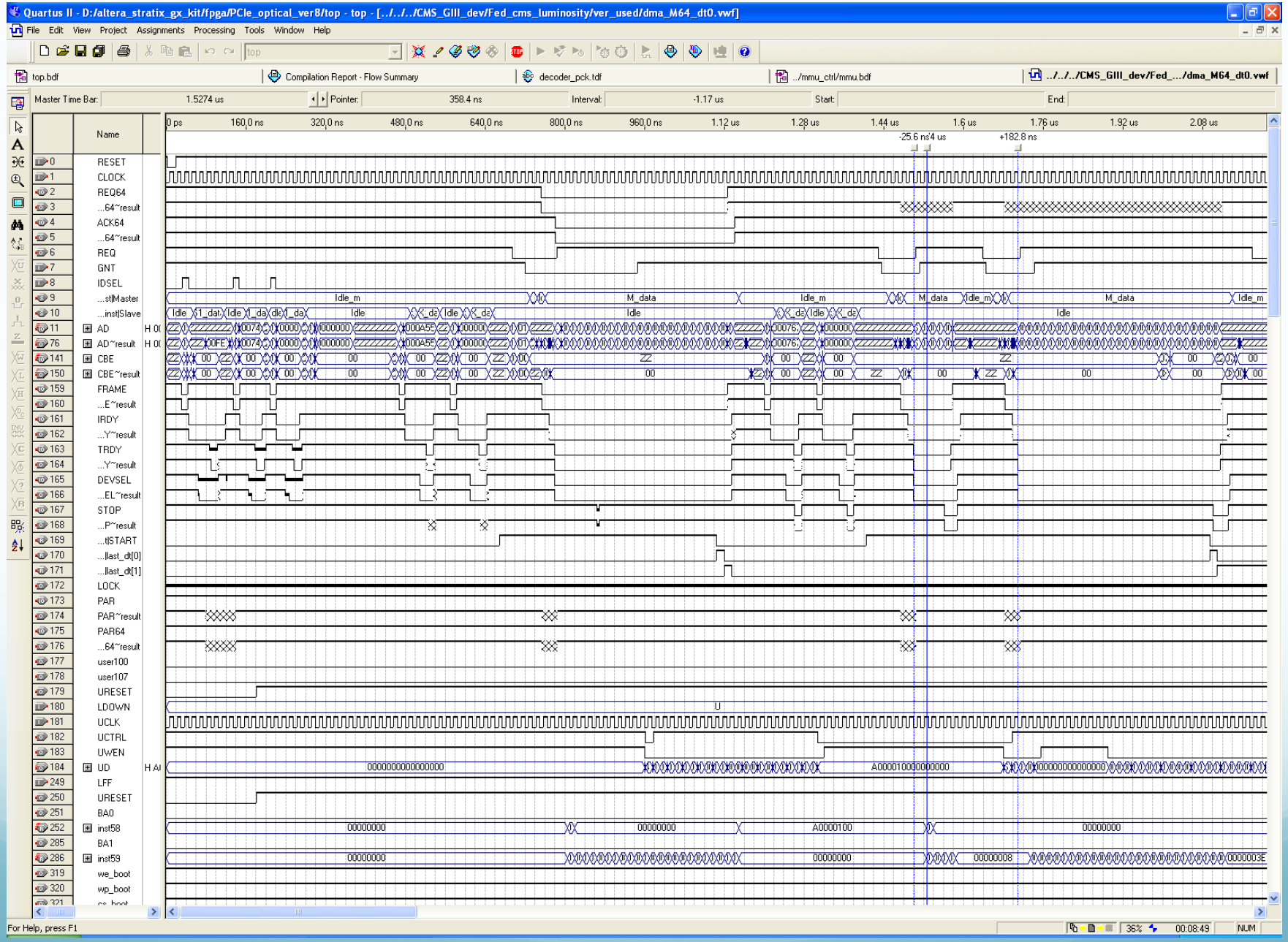


- For large designs, manual floor planning may be necessary

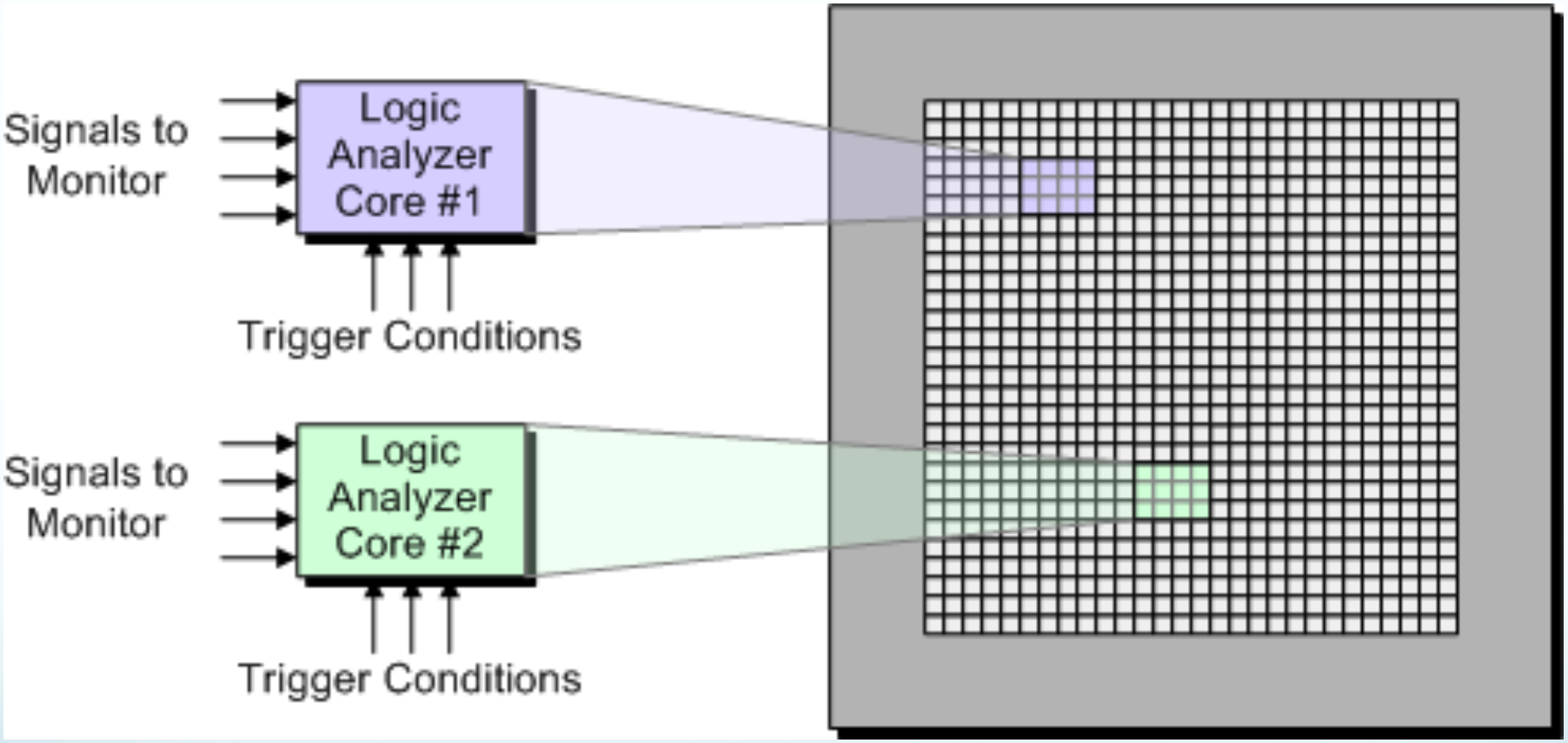


Routing congestion
Xilinx Virtex 7 (Vivado)

Simulation


Quartus II - D:/altera_stratix_gx_kit/fpga/PCIe_optical_ver8/top - top - [../../../CMS_GIII_dev/Fed_cms_luminosity/ver_used/dma_M64_dt0.vwf]
File Edit View Project Assignments Processing Tools Window Help
top.bdf
Compilation Report - Flow Summary
decoder_pck.tdf
../mmu_ctrl/mmu.bdf
../../../CMS_GIII_dev/Fed_.../dma_M64_dt0.vwf
Master Time Bar: 1.5274 us
Pointer: 358.4 ns
Interval: -1.17 us
Start:
End:
Name
RESET
CLOCK
REQ64
ACK64
REQ
GNT
IDSEL
AD
AD~result
CBE
CBE~result
FRAME
IRDY
TRDY
DEVSEL
STOP
LOCK
PAR
PAR64
user100
user107
URESET
LDOWN
UCLK
UCTRL
UWEN
UD
LFF
URESET
BA0
inst58
BA1
inst59
we_boot
wp_boot
Idle_m
M_data
Idle
For Help, press F1
NUM

Embedded Logic Analyzers

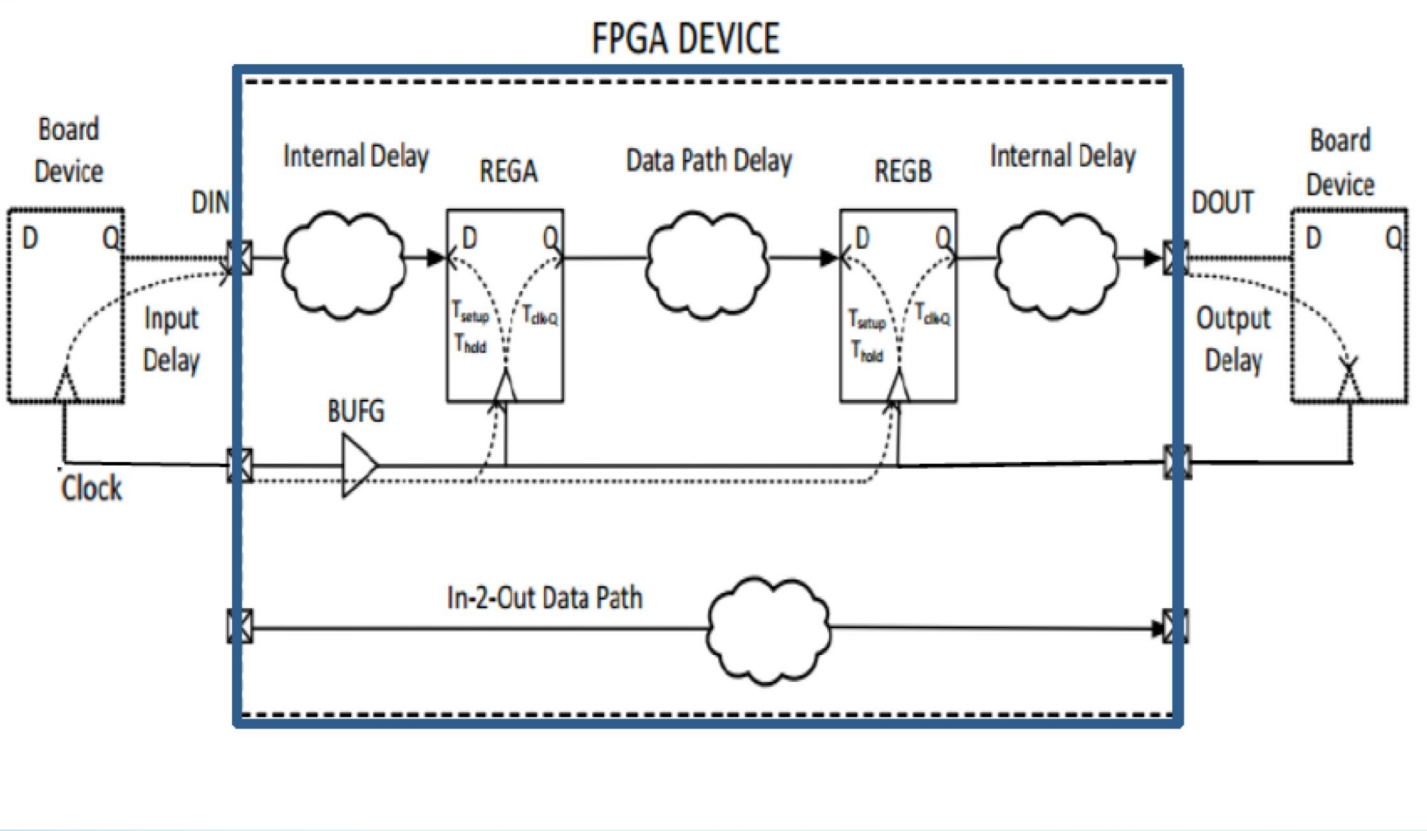


A great tool for debugging your design

Timing

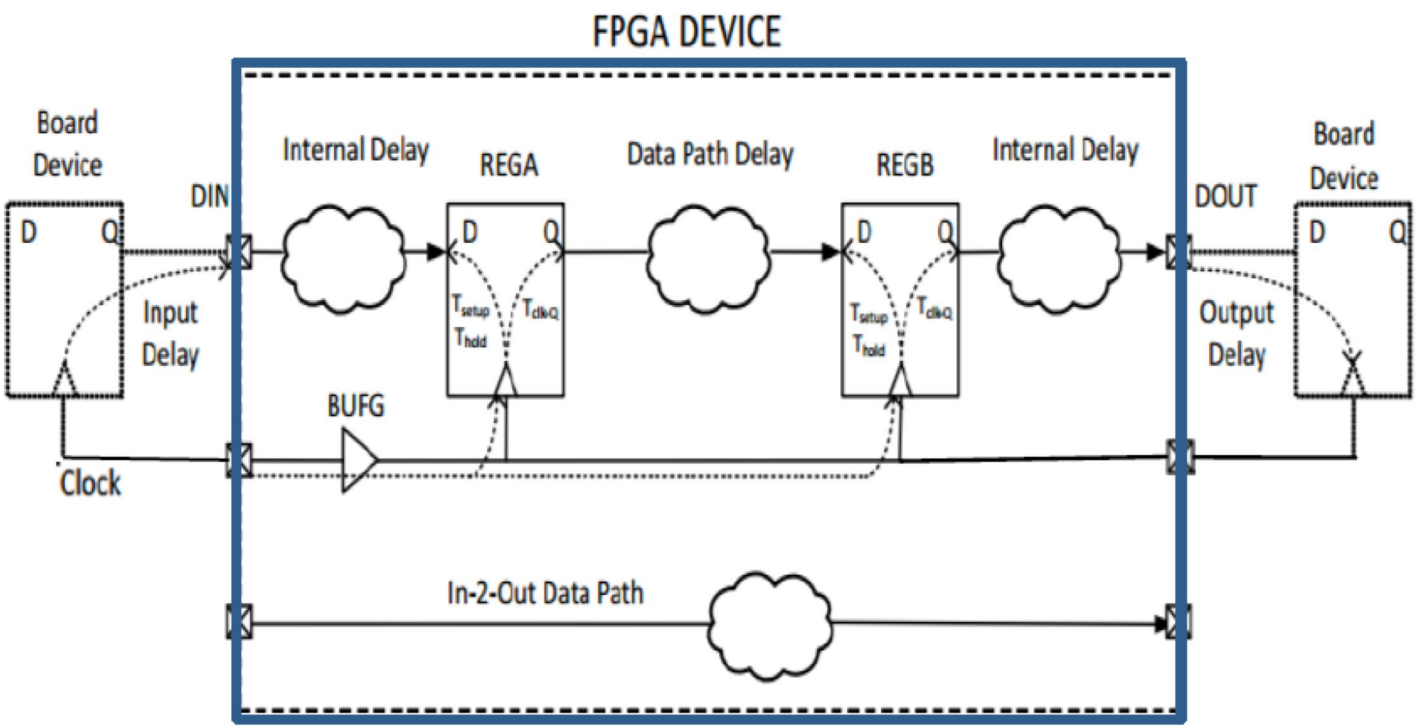
Timing

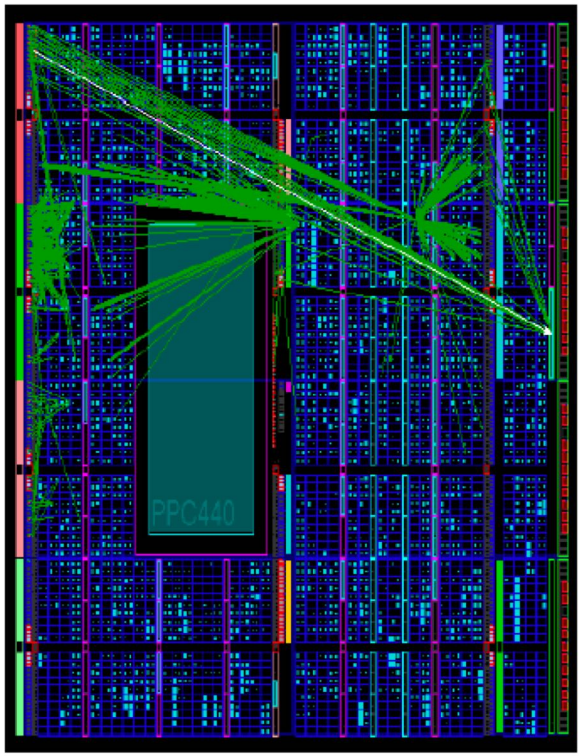
- Timing in FPGA design is critical



Timing

- Timing in FPGA design is critical



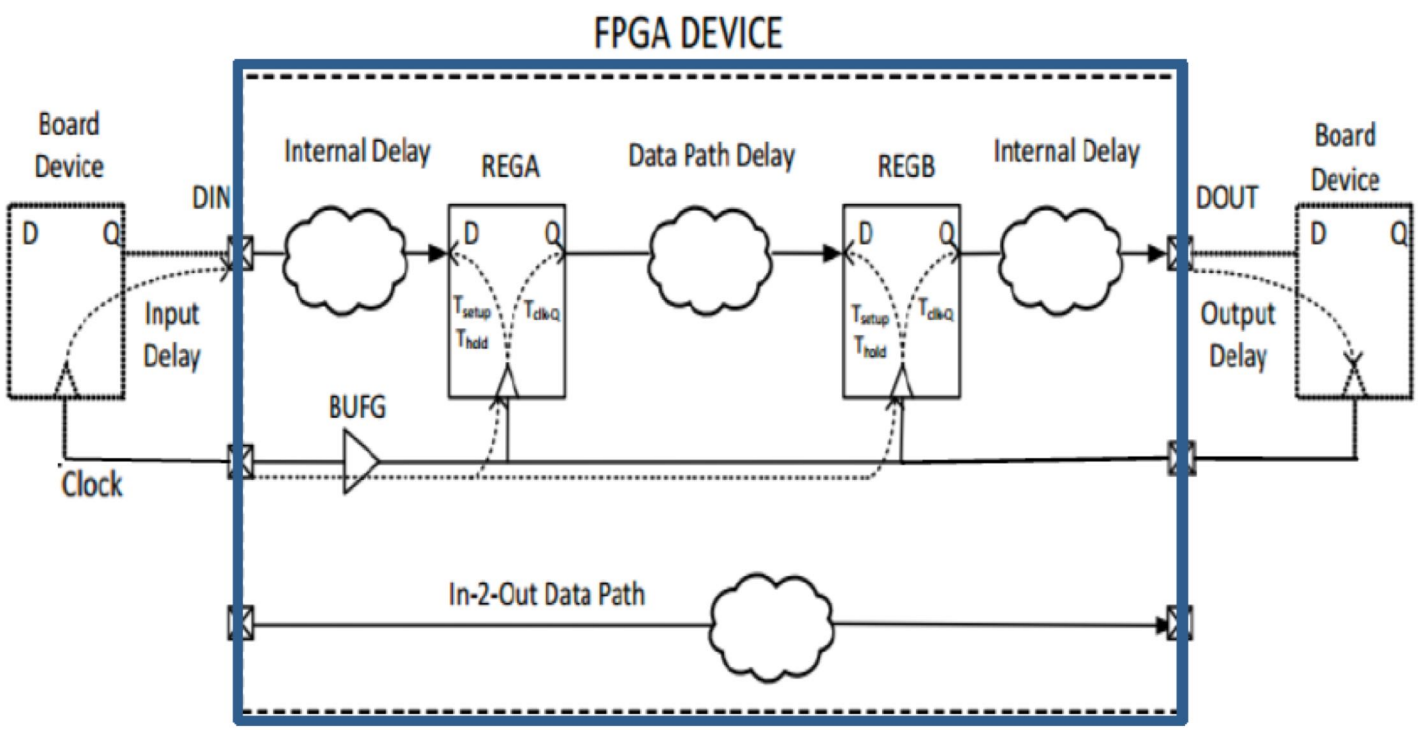


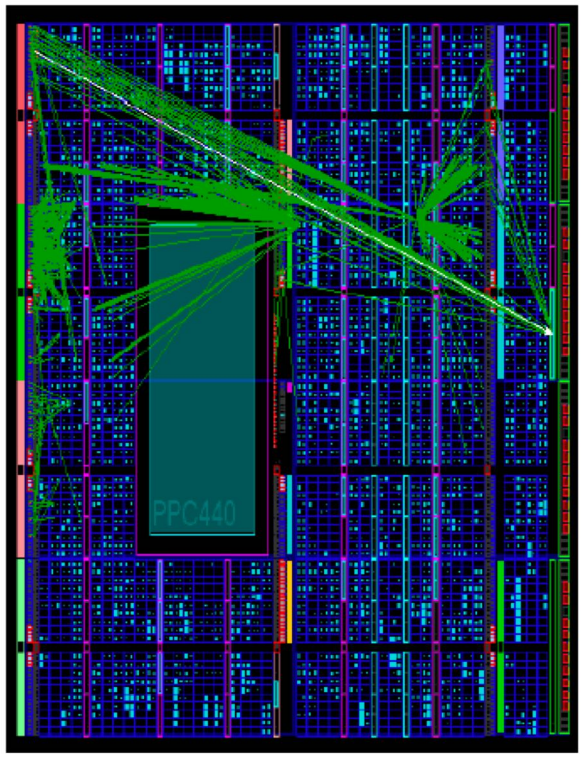
Synthesized RTL (Netlist) is implemented into FPGA

Manoel Barros Marin, ISOTDAQ, https://indico.cern.ch/event/828931/

Timing

- Timing in FPGA design is critical



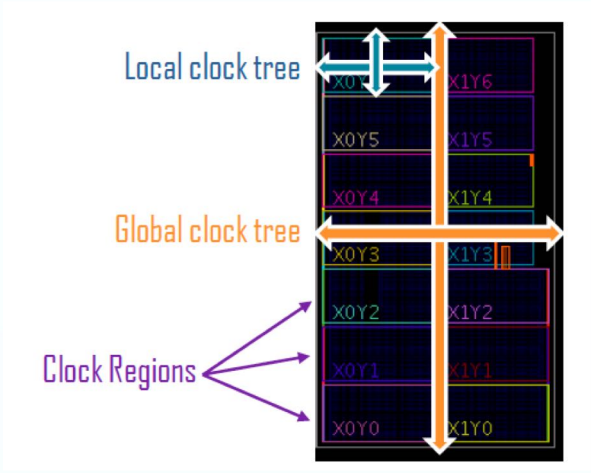


Synthesized RTL (Netlist) is implemented into FPGA

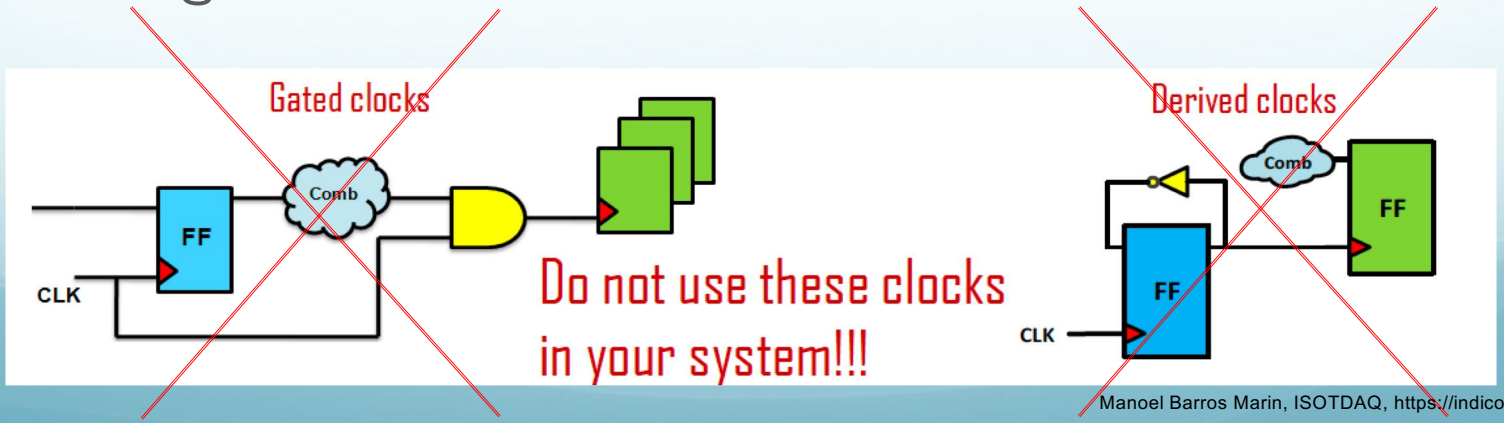
- If signals do not arrive at destination on time
  - Catastrophic consequences

Timing

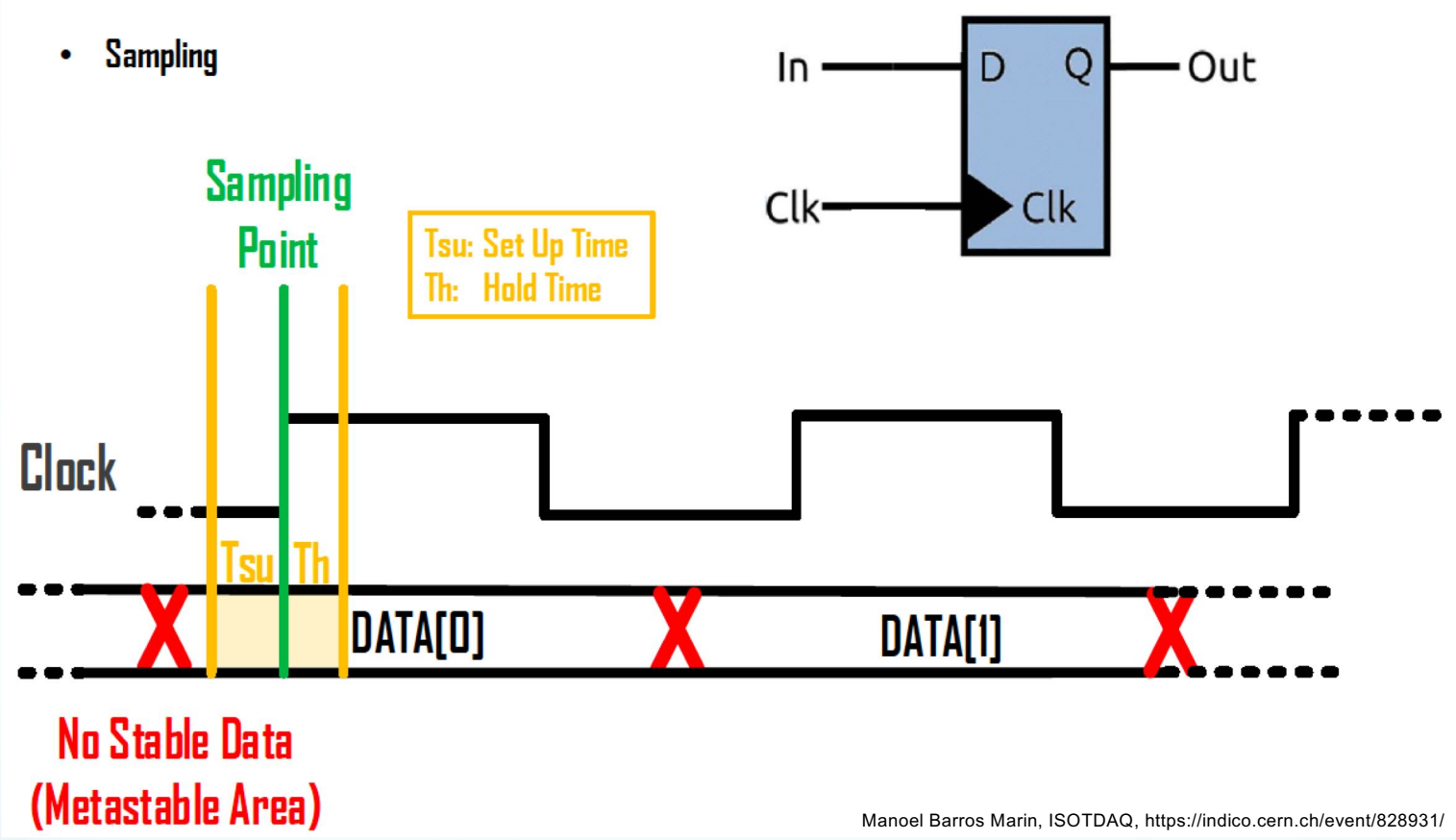
- Always use dedicated clock networks to distribute clocks
  - Assures that clock is seen at all FFs at same time
  - Other clocking resources
    - Clock capable pins
    - Clock buffers
    - Clock Multiplexers
    - Phase Locked Loops
    - Digital Clock Managers



  - Do not gate or derive clocks



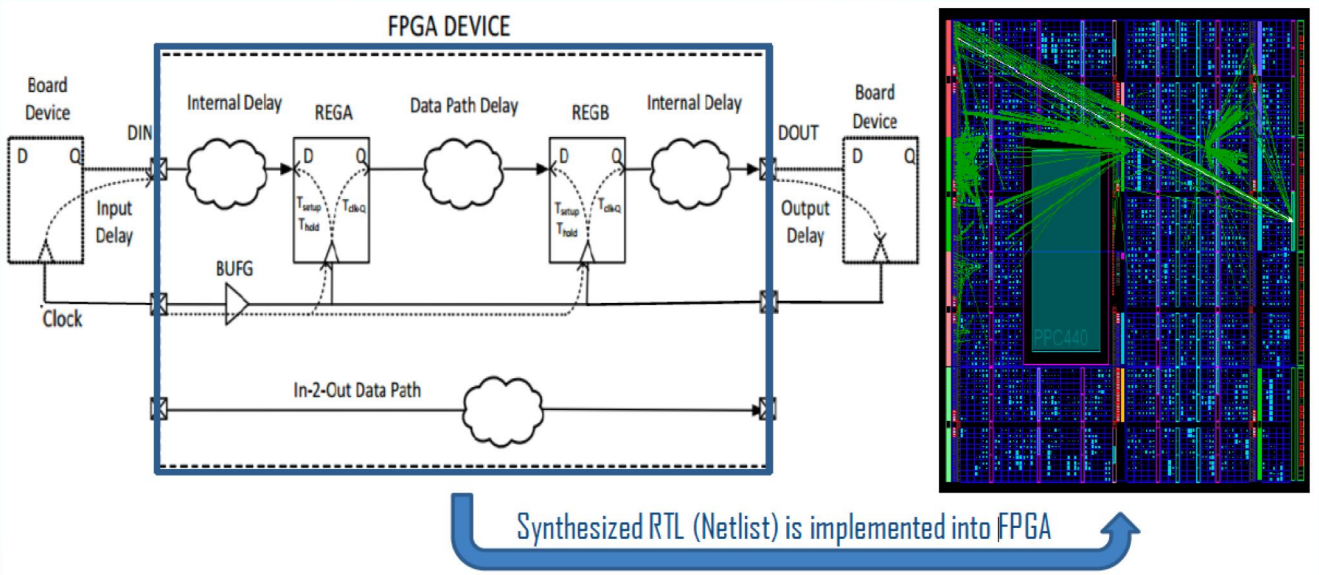
Data paths must respect setup and hold times



Manoel Barros Marin, ISOTDAQ, https://indico.cern.ch/event/828931/

- **Setup time** is the amount of **time** required for the input to a Flip-Flop to be stable before a clock edge. **Hold time** is similar to **setup time**, but it deals with events after a clock edge occurs.

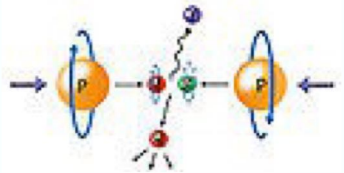
Meeting timing closure



- Place & route step will try to position registers (flip-flops) and logic so that data path delays respect setup and hold times
- Options to meet timing
  - Instruct Place & route to use higher effort level
  - Add register stages & reduce amount of logic in data path (increases latency)
  - Choose location of inputs and outputs (at board design, or through optical patch panel)
  - Placement (area) constraints (give hints to the place & route step)
- Good practice
  - Whenever possible use I/O flip –flops (i.e FFs inside input/output cells)
    - Ensures timing with respect to external components is respected

FPGA applications in the Trigger & DAQ domain

First-Level Trigger at Collider



Timing: beam crossings

LHC: 25 ns

detector

Coarse grain data

Full data
(fine grain)

Delay
FIFO

First Level Trigger

Pipelined
Logic

Fixed Latency
(= processing time
of the first
level trigger)

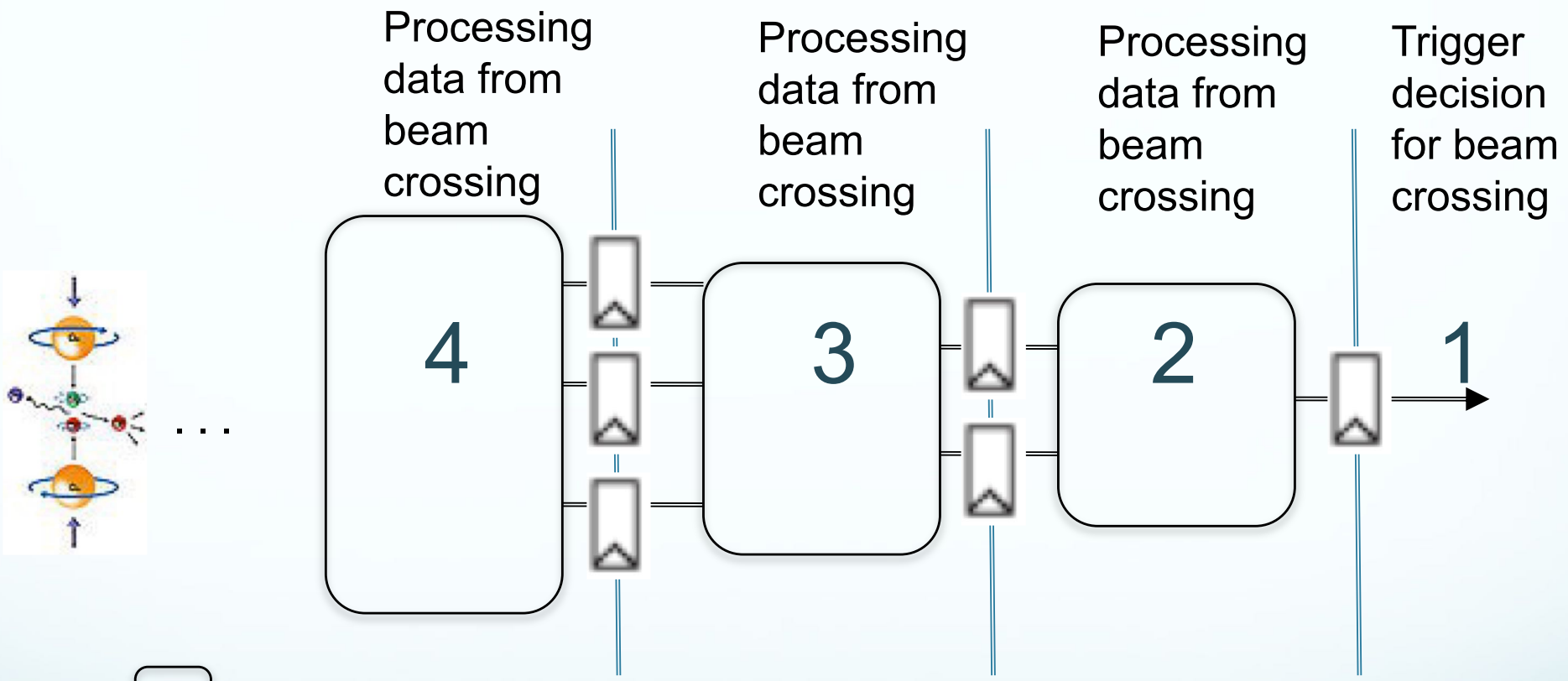
N beam crossings

Trigger decision YES / NO
(for every beam crossing)

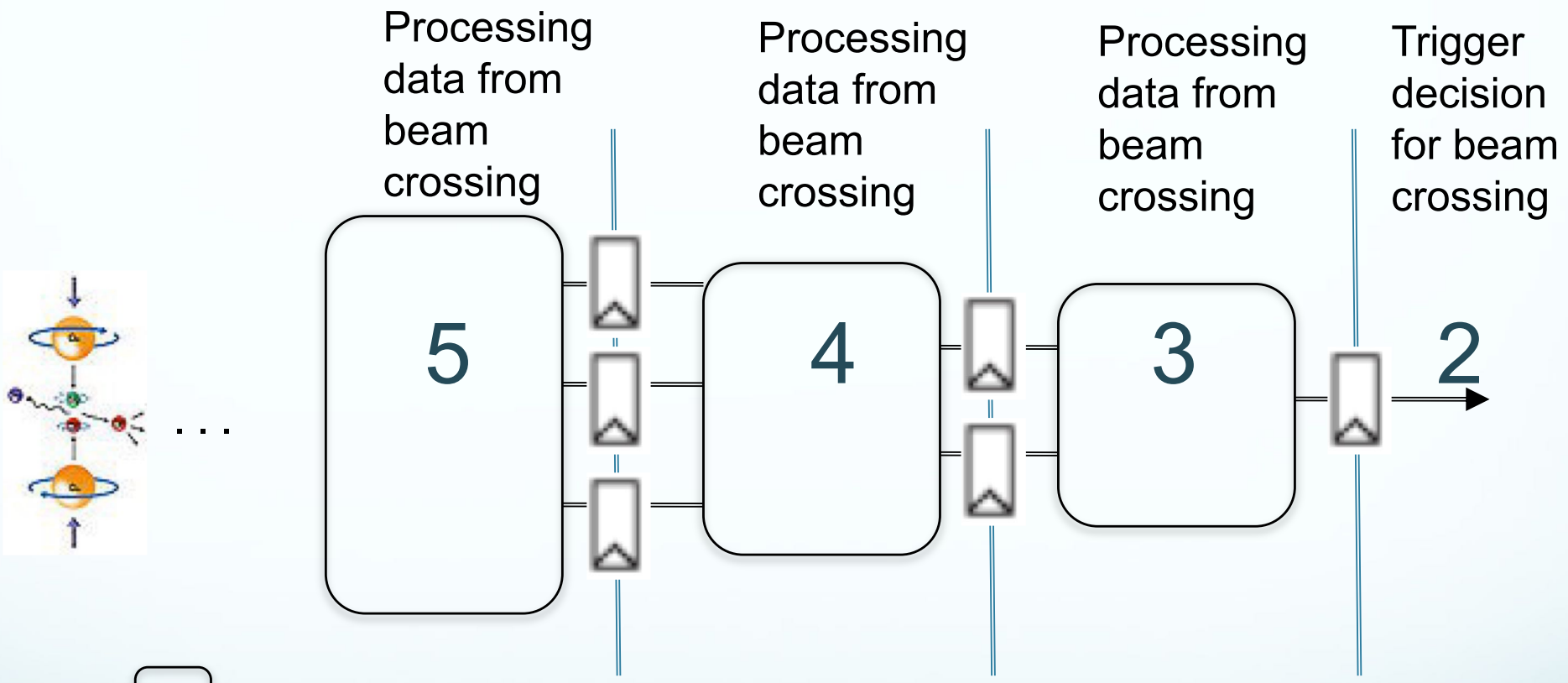
De-
randomizer
FIFO

Latency should be short
In order to limit the length
of the delay FIFOS

Pipelined Logic



Pipelined Logic – a clock cycle later



Why are FPGAs ideal for First-Level Triggers ?

- They are fast
  - Much faster than discrete electronics (shorter connections)
- Many inputs
  - Data from many parts of the detector has to be combined

Low latency

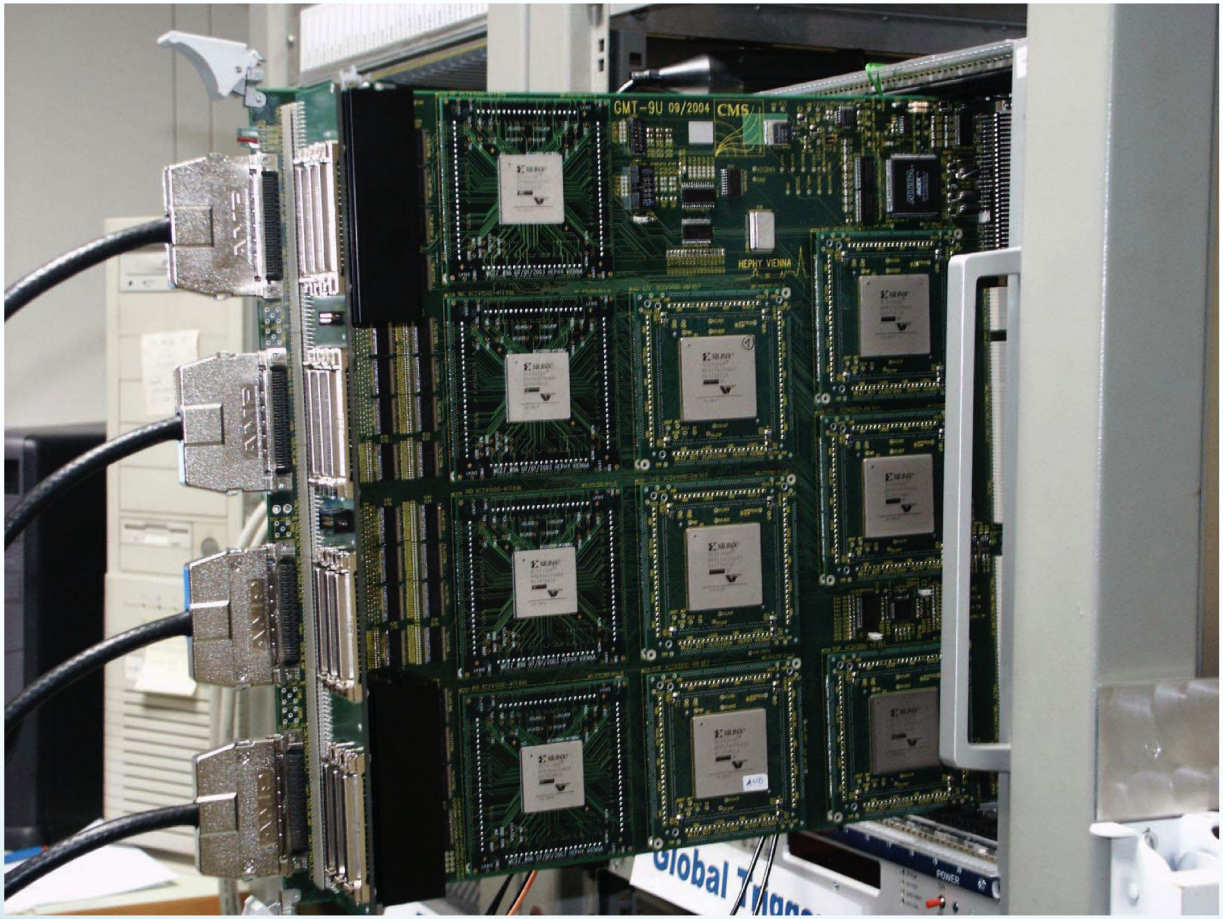
- All operations are performed in parallel
  - Can build pipelined logic
- They can be re-programmed
  - Trigger algorithms can be optimized

High performance

Trigger algorithms implemented in FPGAs

- Peak finding
- Pattern Recognition
- Track Finding
- Clustering / Energy summing
- Sorting
- Topological Algorithms (invariant mass)
- Trigger Control system
- Fast signal merging
- New: Inference with Neural Networks
- Many more …

CMS Global Muon Trigger

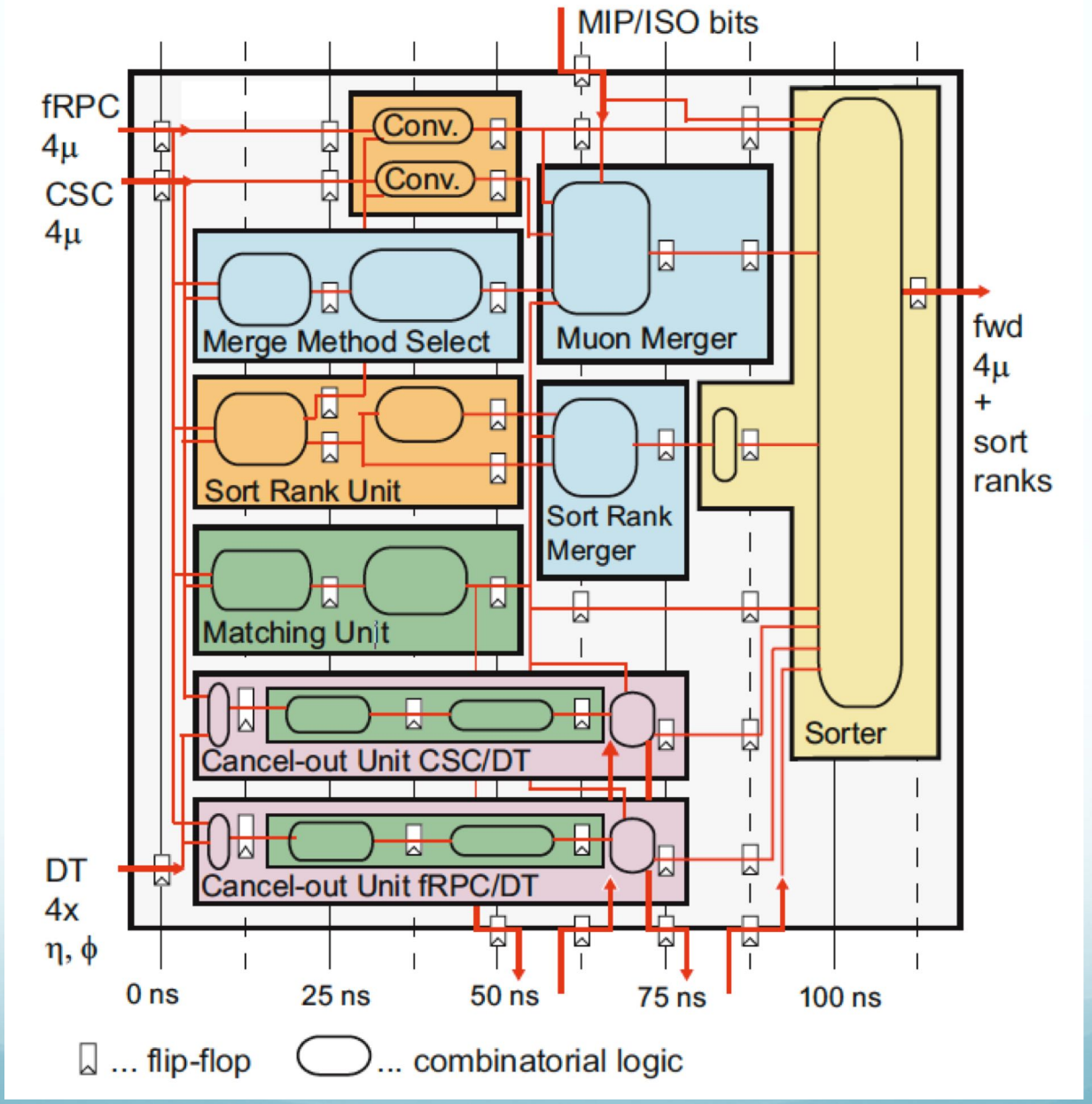


- Input: ~1000 bits
  @ 40 and 80 MHz
- Output: ~50 bits @ 80MHz
- Processing time: 250 ns
- Pipelined logic
  one new result every 25 ns

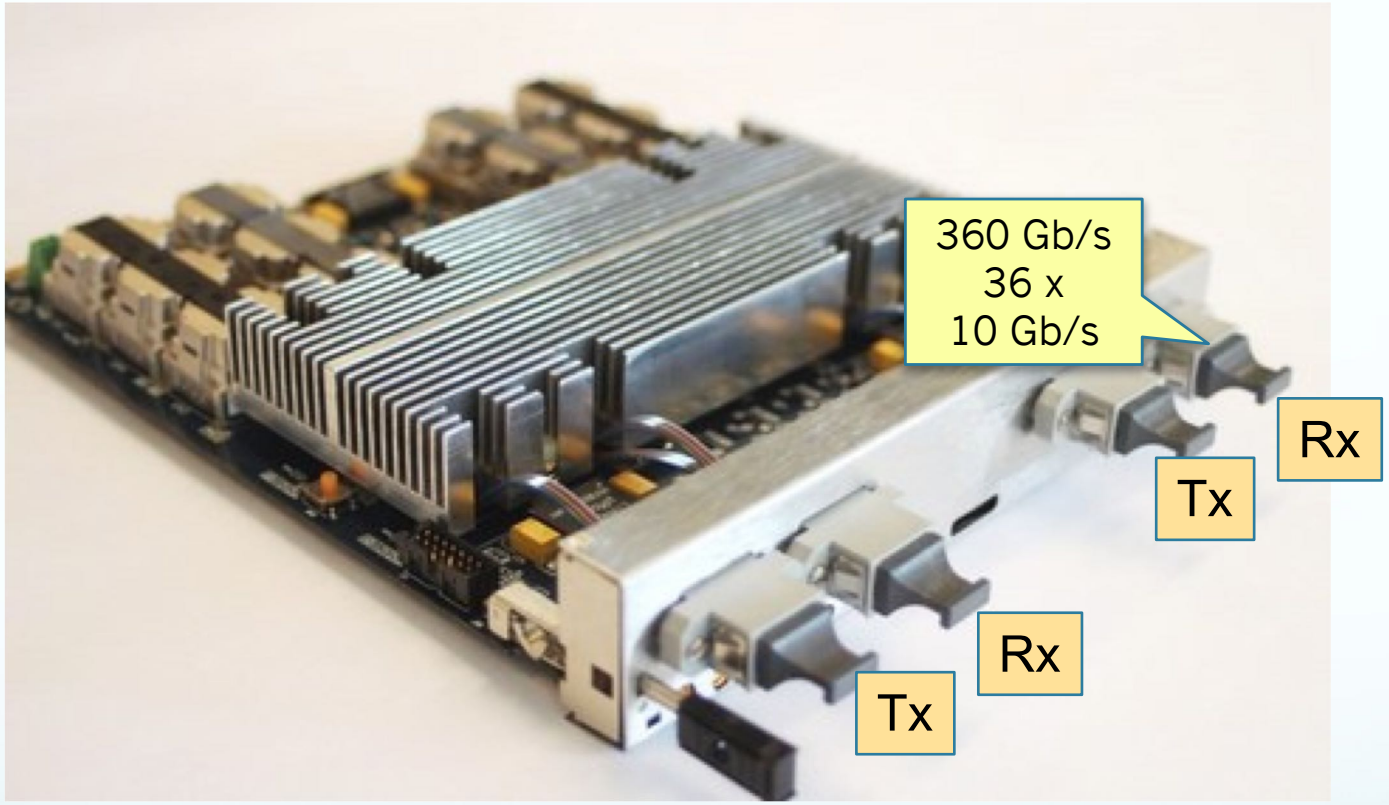
- 10 Xilinx Virtex-II FPGAs
- up to 500 user I/Os per chip
- Up to 25000 LUTs per chip used
- Up to 96 x 18kbit RAM used
- In use in the CMS trigger 2008-2015

- The CMS Global Muon trigger received 16 muon candidates from the three muon systems of CMS
- It merged different measurements for the same muon and found the best 4 over-all muon candidates

CMS Global Muon Trigger main FPGA



µTCA board for Run 2&3
CMS trigger based on Virtex 7



MP7, Imperial College

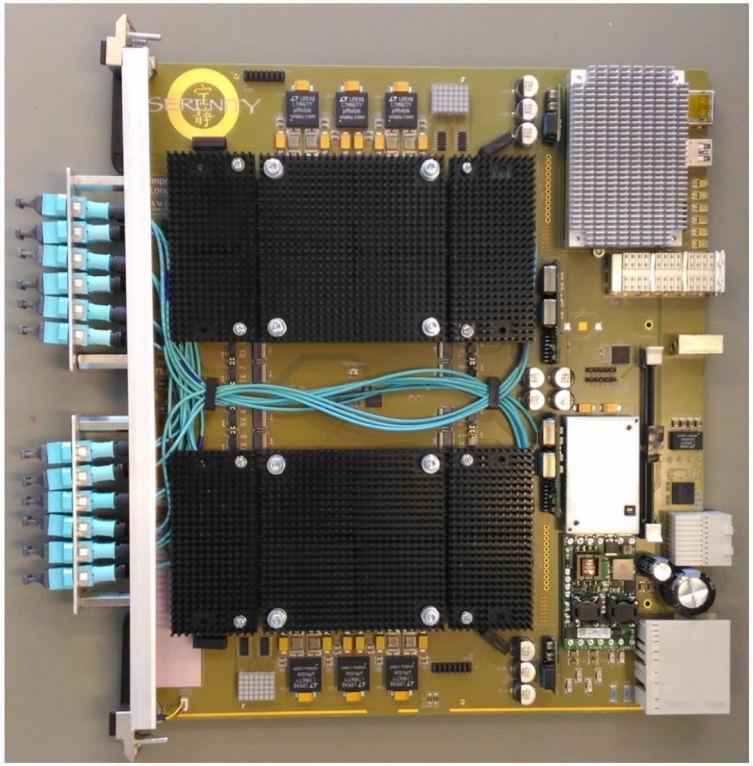
Virtex 7 with 690k logic cells
- 80 x 10 Gb/s transceivers bi-directional
- 72 of them as optical links on front panel
  - 0.75 + 0.75 Tb/s

Being used in the CMS trigger since 2015

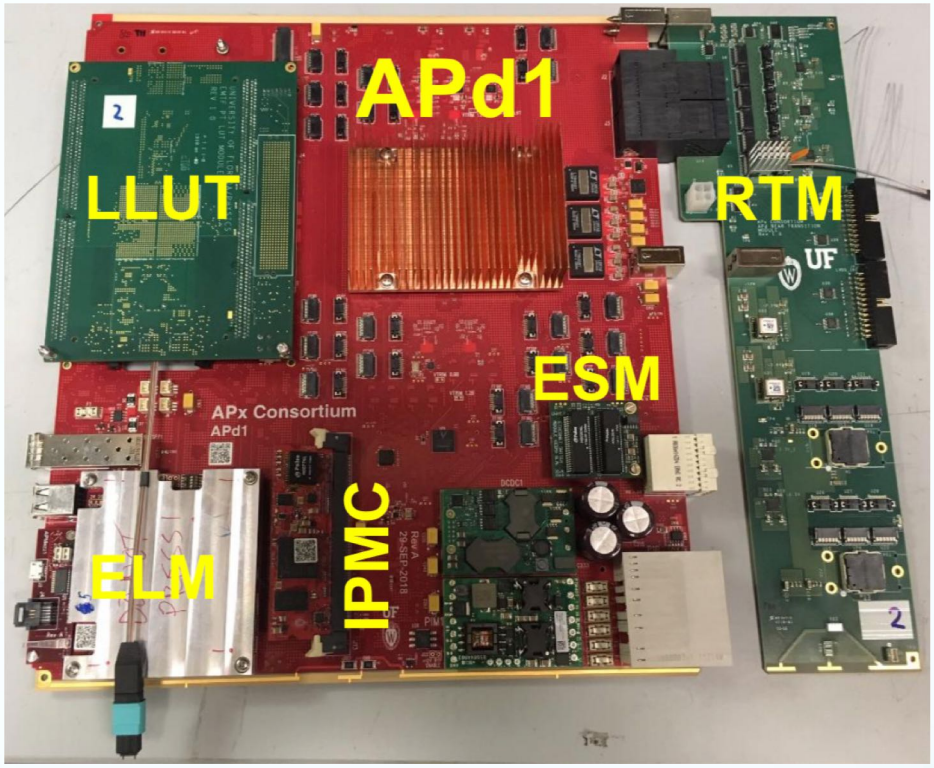
Input/output:
up to 14k bits per 40 MHz clock

Same board used for different functions (different gateware)
Separation of framework + algorithm fw

CMS ATCA Trigger boards for HL-LHC



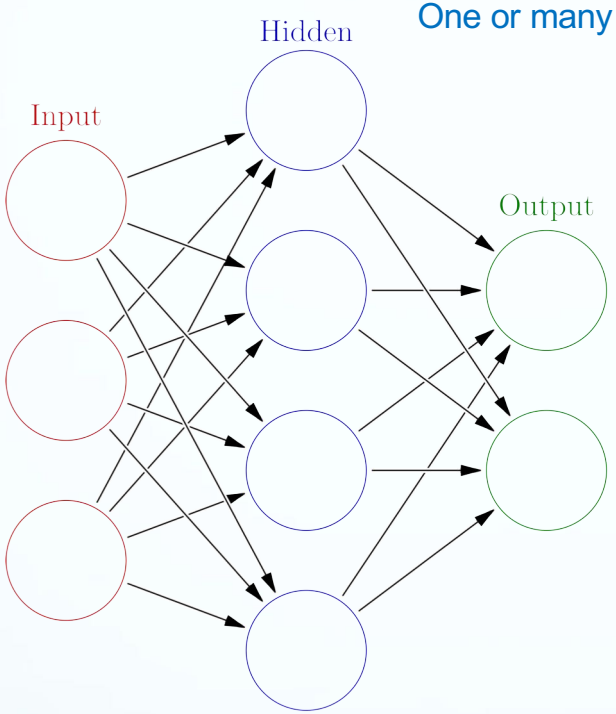
Serenity, UK



APX, US

- Few types of generic boards, ATCA standard
- Xilinx Virtex/Kintex Ultrascale+ FPGAs
- 25-28 Gb/s optical links
- SoC FPGAs used for board control (on some boards)
- Advanced firmware algorithms
  - Vertex finding
  - Particle flow
  - Neural network classifiers

Neural Networks in Trigger



One or many hidden layers

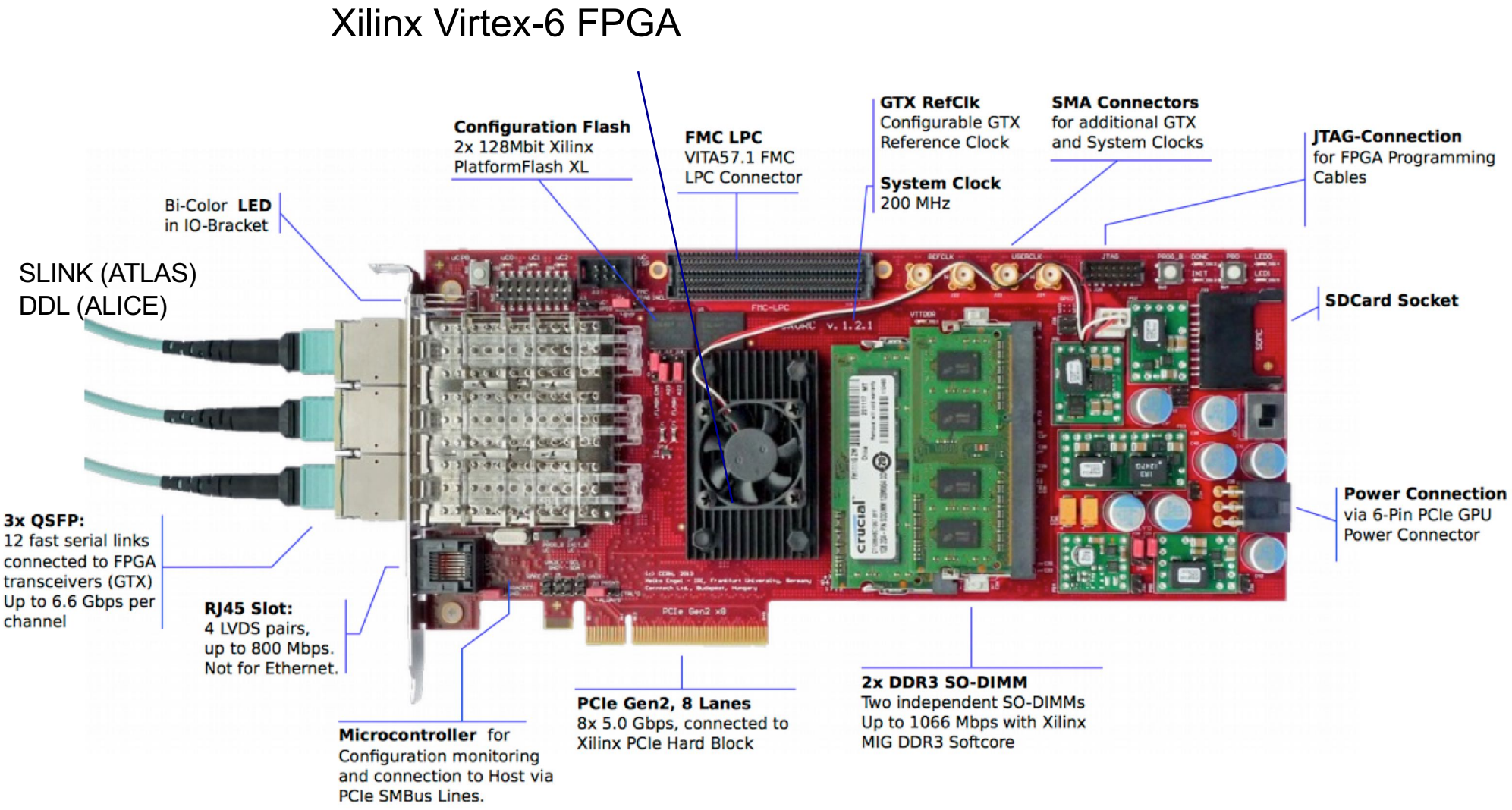
By Glosser.ca - Own work, Derivative of File:Artificial neural network.svg, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=24913461

- Principle
  - Node is assigned a value based on the weighted sum of nodes in the previous layer
  - Maps well to DSP resources in FPGA (multiplier + adder)
- Applications:
  - Jet classification
  - Assignment of transverse momentum based on many measurements
  - ...
- Tools
  - Many commercial tools
  - hls4ml (optimized for latency)
    - Firmware generation from high-level model using Vivado HLS

FPGAs in Data Acquisition

- Frontend Electronics
  - Pedestal subtraction
  - Zero suppression
  - Compression
  - ...
- Custom data links
  - E.g. SLINK-64 over copper
    - Several serial LVDS links in parallel
    - Up to 400 MB/s
  - SLINK/SLINK-express over optical
- Interface from custom hardware to commercial electronics
  - PCI/PCIe, VME bus, Myrinet, 10/40/100 Gb/s Ethernet etc.

C-RORC (Alice) / Robin NP (ATLAS) for Run-2

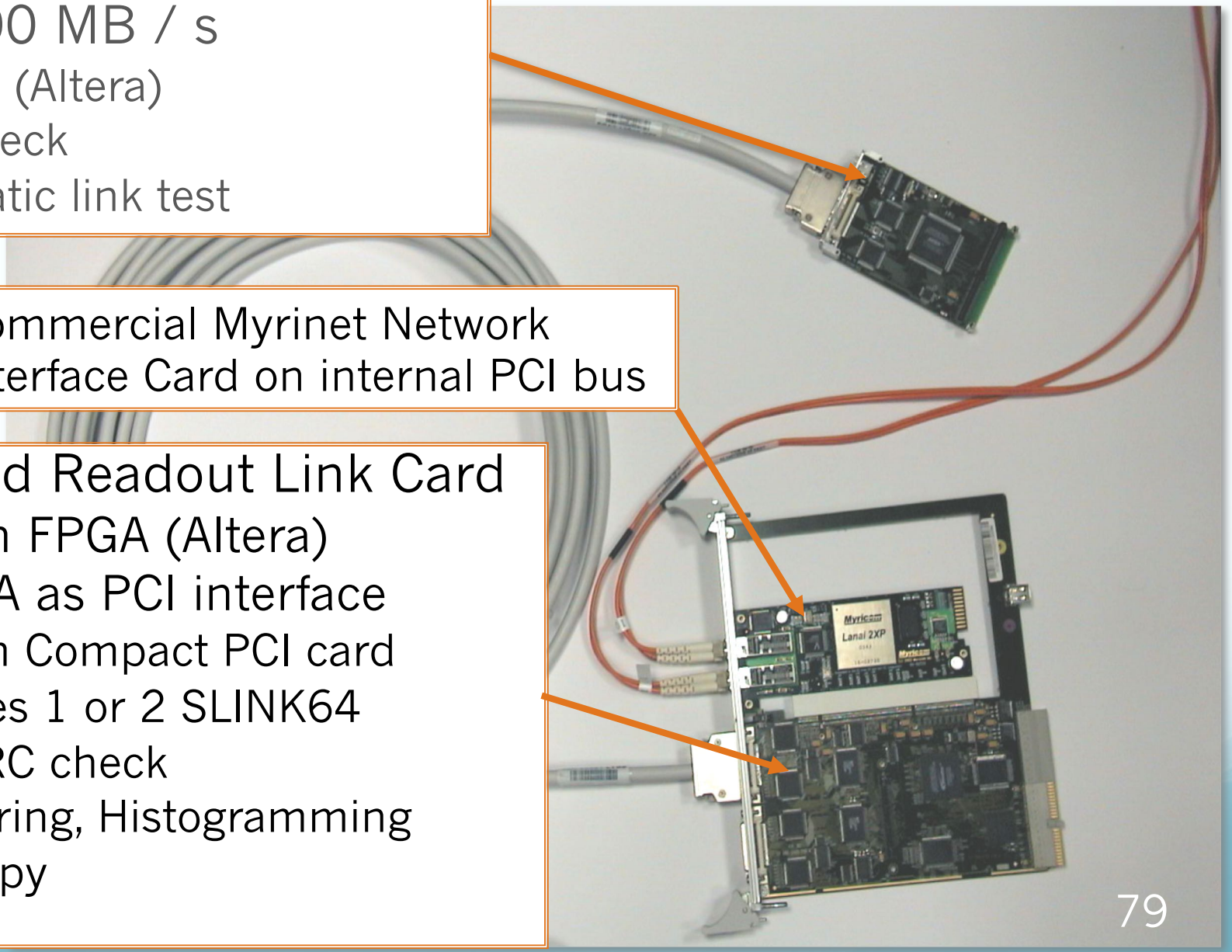


CMS Front-end Readout Link (Run-1)

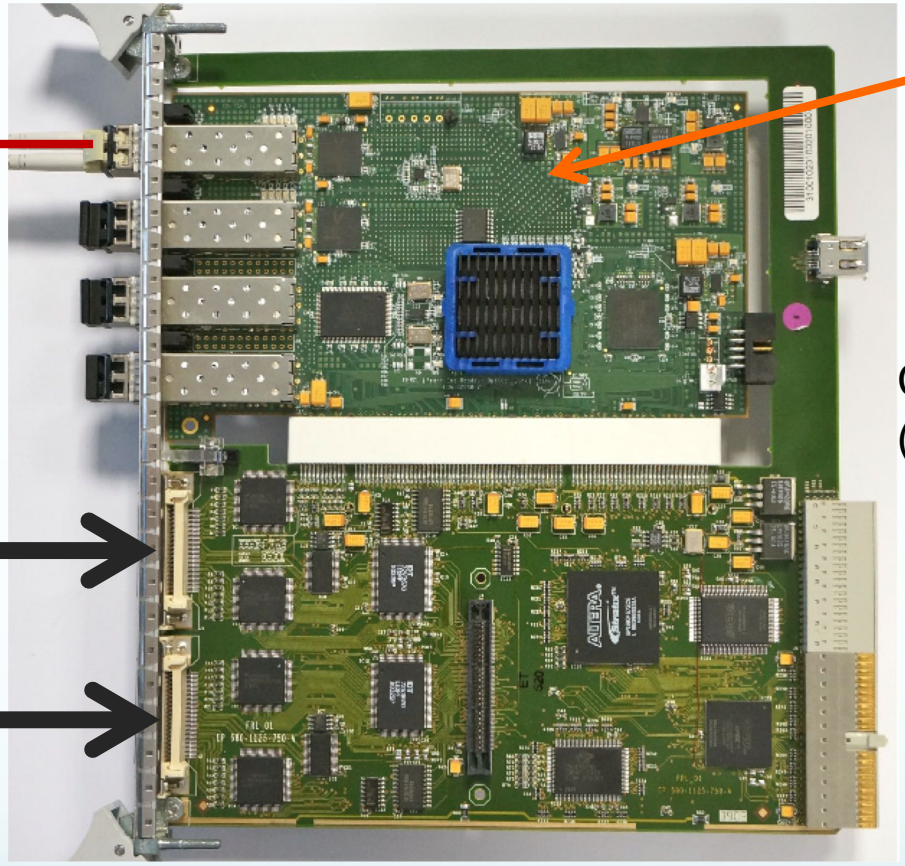
- SLINK Sender Mezzanine Card: 400 MB / s
  - 1 FPGA (Altera)
  - CRC check
  - Automatic link test

Commercial Myrinet Network Interface Card on internal PCI bus

- Front-end Readout Link Card
  - 1 main FPGA (Altera)
  - 1 FPGA as PCI interface
  - Custom Compact PCI card
  - Receives 1 or 2 SLINK64
  - 2nd CRC check
  - Monitoring, Histogramming
  - Event spy



CMS Readout Link for Run-2 in use since 2015



10 Gb/s TCP/IP

SLINK-64 input
LVDS / copper

Myrinet NIC replaced by custom-built card ("FEROL")

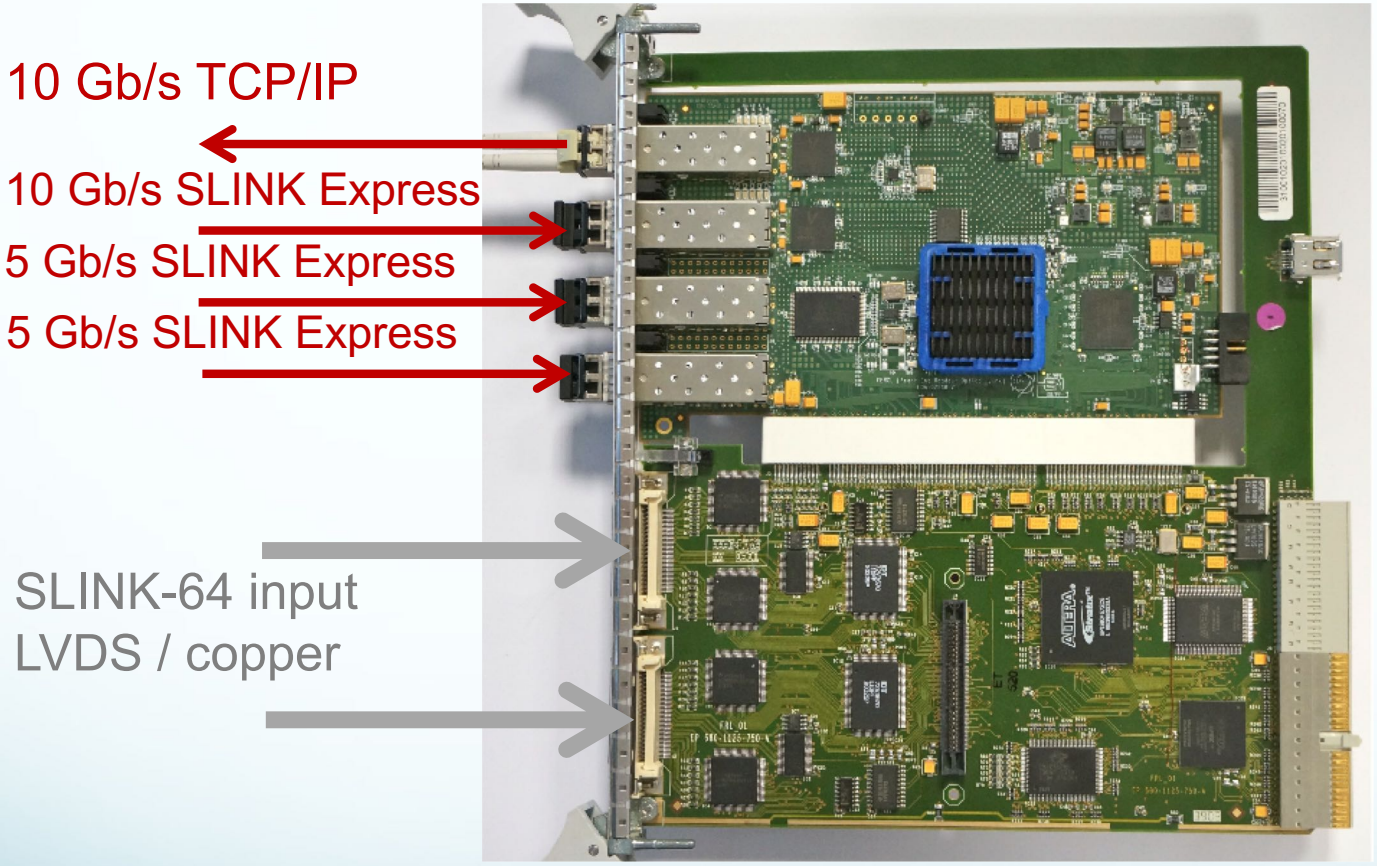
Cost effective solution
(need many boards)
Rather inexpensive FPGA
+ commercial chip to combine
3 Gb/s links to 10 Gb/s

FEROL (Front End Readout Optical Link)

Input: 1x or 2x SLINK (copper)
1x or 2x 5Gb/s optical
1x 10Gb/s optical

Output: 10 Gb/s Ethernet optical
TCP/IP sender in FPGA

CMS Readout Link for Run-2

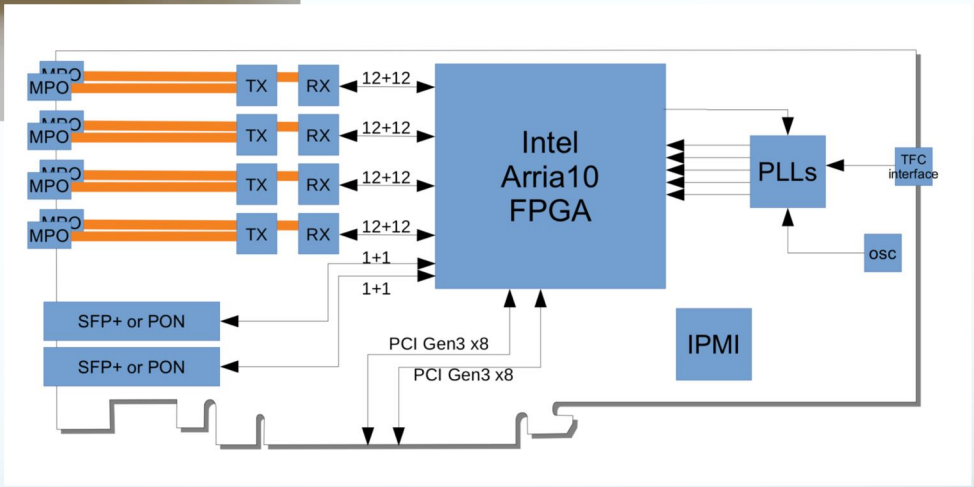


FEROL (Front End Readout Optical Link)

Input: 1x or 2x SLINK (copper)
1x or 2x 5Gb/s optical
1x 10Gb/s optical

Output: 10 Gb/s Ethernet optical
TCP/IP sender in FPGA

PCIe40 – LHCb and ALICE Run-3



- 48 bidirectional links running at up to 10 Gbits/s each (minipods)
- 2 bidirectional links running at up to 10 Gbits/s devoted to time distribution (can use SFP+ or 10G PON devices)
- Sustained 112 Gbits/s interface with CPU through PCIe

CMS DTH (DAQ and Timing Hub) for HL-LHC

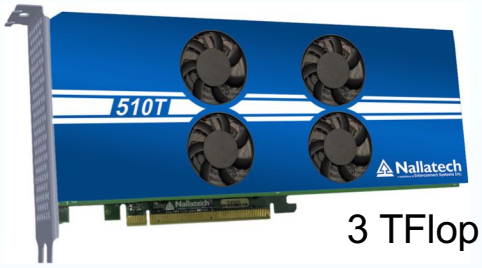
DTH prototype 1

- ATCA board using Xilinx Virtex Ultrascale + FPGAs
- Several DAQ units per board
  - Each unit receiving optical inputs at 16 Gb/s and 25 Gb/s
  - 4x 100 Gb/s Ethernet to commercial network (4 links of 25Gb/s)
  - TCP/IP in FPGA
- Board distributes timing and control
- Board contains switch for control network

FPGAs in other domains

- Medical imaging
- Advanced Driver Assistance Systems (Image Processing)
- Speech recognition
- Cryptography
- Bioinformatics (Genome sequencing)
- Aerospace / Defense
- (Bitcoin mining)
- 5G Wireless

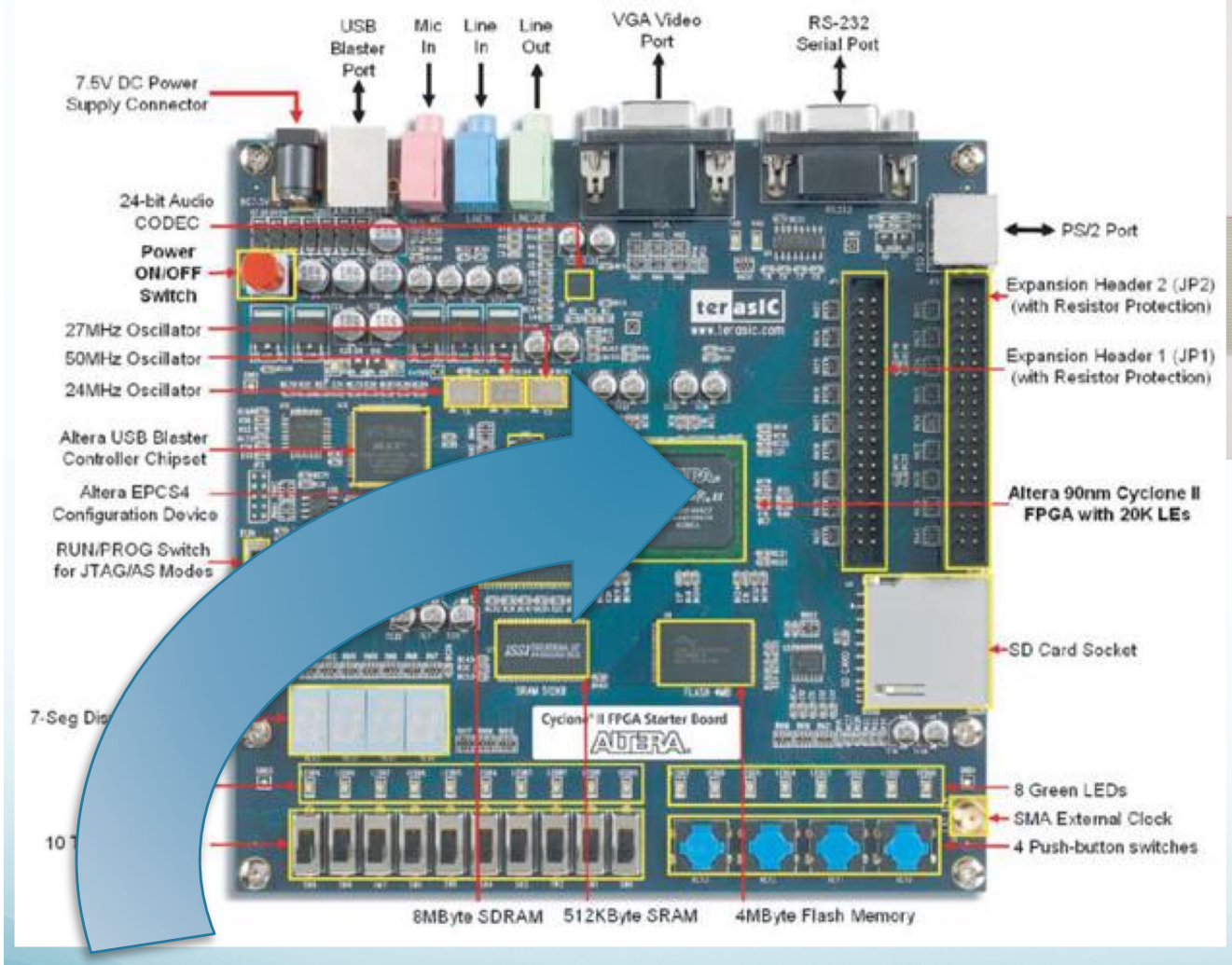
- ASIC Prototyping
- Compute accelerators
  - Accelerator cards

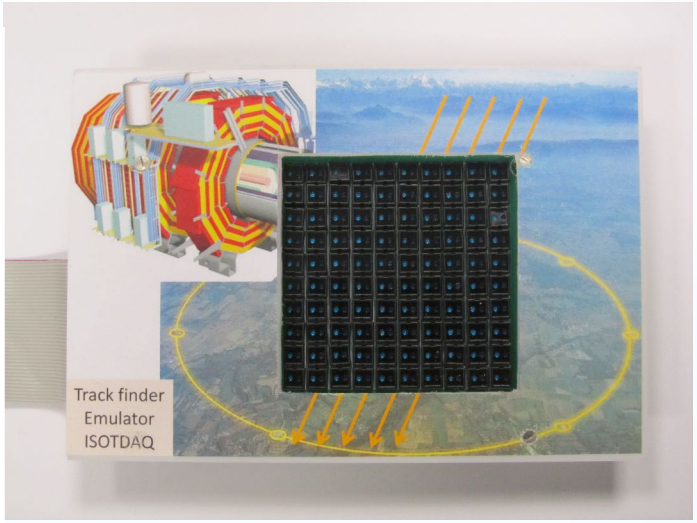


3 TFlop

  - Server processors w. FPGA
  - Financial
  - Inferencing
  - Video transcoding
  - ...

Lab Session 5: Programming an FPGA





At the annual ISOTDAQ school

https://isotdaq-schools.web.cern.ch/

You are going to design the digital electronics inside this FPGA !

Lab Session 13: System-on-a-chip FPGA

At the annual ISOTDAQ school

https://isotdaq-schools.web.cern.ch/

Z-turn board
Zynq w. dual-core ARM

Design the digital electronics and software in this SoC FPGA!

Top-of-the-line Xilinx devices

Device Name			VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU27P	VU29P	VU31P	VU33P	VU35P	VU37P
System Logic Cells (K)			862	1,314	1,724	2,586	2,835	3,780	2,835	3,780	962	962	1,907	2,852
CLB Flip-Flops (K)			788	1,201	1,576	2,364	2,592	3,456	2,592	3,456	879	879	1,743	2,607
CLB LUTs (K)			394	601	788	1,182	1,296	1,728	1,296	1,728	440	440	872	1,304
Max. Dist. RAM (Mb)			12.0	18.3	24.1	36.1	36.2	48.3	36.2	48.3	12.5	12.5	24.6	36.7
Total Block RAM (Mb)			25.3	36.0	50.6	75.9	70.9	94.5	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM (Mb)			90.0	132.2	180.0	270.0	270.0	360.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)			–	–	–	–	–	–	–	–	4	8	8	8
HBM AXI Interfaces			–	–	–	–	–	–	–	–	32	32	32	32
Clock Mgmt Tiles (CMTs)			10	20	20	30	12	16	16	16	4	4	8	12
DSP Slices			2,280	3,474	4,560	6,840	9,216	12,288	9,216	12,288	2,880	2,880	5,952	9,024
Peak INT8 DSP (TOP/s)			7.1	10.8	14.2	21.3	28.7	38.3	28.7	38.3	8.9	8.9	18.6	28.1
PCIe® Gen3 x16			2	4	4	6	3	4	1	1	0	0	1	2
PCIe Gen3 x16/Gen4 x8 / CCIX[1]			–	–	–	–	–	–	–	–	4	4	4	4
150G Interlaken			3	4	6	9	6	8	6	8	0	0	2	4
100G Ethernet w/ KR4 RS-FEC			3	4	6	9	9	12	11	15	2	2	5	8
Max. Single-Ended HP I/Os			520	832	832	832	624	832	520	676	208	208	416	624
GTY 32.75Gb/s Transceivers			40	80	80	120	96	128	32	32	32	32	64	96
GTM 58Gb/s PAM4 Transceivers									32	48				
100G / 50G KP4 FEC									16 / 32	24 / 48				
Extended[2]			-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial			-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	–	–	–
Footprint[3,4,5]		Dim. (mm)	HP I/O, GTY						HP I/O, GTY, GTM		HP I/O, GTY			
Footprint compatible with 20nm UltraScale Devices with same footprint identifier	C1517	40x40	520, 40											
	F1924[6]	45x45					624, 64							
	A2104	47.5x47.5		832, 52	832, 52	832, 52								
		52.5x52.5[7]						832, 52						
	B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76							
		52.5x52.5[7]						702, 76						
	C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96							
		52.5x52.5[7]						416, 104						
	D2104	47.5x47.5				676, 76	572, 76							
		52.5x52.5[7]						676, 76	676, 16, 30	676, 16, 30				
	A2577	52.5x52.5				448, 120	448, 96	448, 128	448, 32, 48	448, 32, 48				
	H1924	45x45									208, 32			
	H2104	47.5x47.5										208, 32	416, 64	
	H2892	55x55											416, 64	624, 96

Virtex® UltraScale+™ FPGAs

Intel® Stratix® 10

INTEL® STRATIX® 10 GX/SX PRODUCT TABLE

	PRODUCT LINE	GX 400 SX 400	GX 650 SX 650	GX 850 SX 850	GX 1100 SX 1100	GX 1650 SX 1650	GX 2100 SX 2100	GX 2500 SX 2500	GX 2800 SX 2800	GX 4500 SX 4500	GX 5500 SX 5500
Resources	Logic elements (LEs)[1]	378,000	612,000	841,000	1,092,000	1,624,000	2,005,000	2,422,000	2,753,000	4,463,000	5,510,000
	Adaptive logic modules (ALMs)	128,160	207,360	284,960	370,080	550,540	679,680	821,150	933,120	1,512,820	1,867,680
	ALM registers	512,640	829,440	1,139,840	1,480,320	2,202,160	2,718,720	3,284,600	3,732,480	6,051,280	7,470,720
	Hyper-Registers from Intel® HyperFlex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric									
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees									
	M20K memory blocks	1,537	2,489	3,477	4,401	5,851	6,501	9,963	11,721	7,033	7,033
	M20K memory size (Mb)	30	49	68	86	114	127	195	229	137	137
	MLAB memory size (Mb)	2	3	4	6	8	11	13	15	23	29
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,520	3,145	3,744	5,011	5,760	1,980	1,980
	18 x 19 multipliers	1,296	2,304	4,032	5,040	6,290	7,488	10,022	11,520	3,960	3,960
	Peak fixed-point performance (TMACS)[2]	2.6	4.6	8.1	10.1	12.6	15.0	20.0	23.0	7.9	7.9
	Peak floating-point performance (TFLOPS)[3]	1.0	1.8	3.2	4.0	5.0	6.0	8.0	9.2	3.2	3.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection									
	Hard processor system[4]	Quad-core 64 bit ARM* Cortex*-A53 up to 1.5 GHz with 32 KB I/D cache, NEON* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I²C x5, general-purpose timers x7, watchdog timer x4									
	Maximum user I/O pins	392	400	736	736	704	704	1160	1160	1640	1640
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	192	192	360	360	336	336	576	576	816	816
	Total full duplex transceiver count	24	48	48	48	96	96	96	96	24	24
	GXT full duplex transceiver count (up to 30 Gbps)	16	32	32	32	64	64	64	64	16	16
	GX full duplex transceiver count (up to 17.4 Gbps)	8	16	16	16	32	32	32	32	8	8
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	1	2	2	2	4	4	4	4	1	1
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys									
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[5]											
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)		392,8,192,24	392,8,192,24	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		–	400,16,192,48	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		–	–	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	736,16,360,48	736,16,360,48	–	–	–	–	–	–
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96	–	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	–	–	–	1160,8,576,24	1160,8,576,24	1640,8,816,24	1640,8,816,24

Intel® Stratix® 10

INTEL® STRATIX® 10 TX PRODUCT TABLE

	PRODUCT LINE	TX 1650		TX 2100		TX 2500			TX 2800		
Resources	Logic elements (LEs)[1]	1,679,000		2,073,000		2,422,000			2,753,000		
	Adaptive logic modules (ALMs)	569,200		702,720		821,150			933,120		
	ALM registers	2,276,800		2,810,880		3,284,600			3,732,480		
	Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric									
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees									
	eSRAM memory blocks	2		2		–			–		
	eSRAM memory size (Mb)	90		90		–			–		
	M20K memory blocks	6,162		6,847		9,963			11,721		
	M20K memory size (Mb)	120		134		195			229		
	MLAB memory size (Mb)	9		11		13			15		
	Variable-precision digital signal processing (DSP) blocks	3,326		3,960		5,011			5,760		
	18 x 19 multipliers	6,652		7,920		10,022			11,520		
	Peak fixed-point performance (TMACS)[2]	13.3		15.8		20.0			23.0		
	Peak floating-point performance (TFLOPS)[3]	5.3		6.3		8.0			9.2		
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection									
	Hard processor system	Quad-core 64-bit ARM* Cortex*-A53 up to 1.5 GHz with 32KB I/D cache, NEON* coprocessor, 1 MB L2 Cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I²C x5, general purpose timers x7, watchdog timer x4									
		–		–		Yes			Yes		
	Maximum user I/O pins	544	440	544	440	544	440	296	544	440	296
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	264	216	264	216	264	216	144	264	216	144
	Total full duplex transceiver count	72	96	72	96	72	96	144	72	96	144
	GXE transceiver count - PAM-4 (up to 58 Gbps) or NRZ (up to 30 Gbps)	12 PAM-4 24 NRZ	36 PAM-4 72 NRZ	12 PAM-4 24 NRZ	36 PAM-4 72 NRZ	12 PAM-4 24 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ	12 PAM-4 24 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	32	16	32	16	32	16	16	32	16	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	16	8	16	8	16	8	8	16	8	8
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	2	1	2	1	2	1	1	2	1	1
	100G Ethernet MAC (no FEC) hard IP blocks	2	1	2	1	2	1	1	2	1	1
	100G Ethernet MAC + FEC hard IP blocks	4	12	4	12	4	12	20	4	12	20
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys									

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O count, LVDS pairs, GXE (E-Tile) Transceiver Count, and GXT+GX (H-Tile) Transceiver Count[4]

F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)	544,16,264,24,48	544,16,264,24,48	544,16,264,24,48	544,16,264,24,48
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)	440,8,216,72,24	440,8,216,72,24	440,8,216,72,24	440,8,216,72,24
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)	–	–	296,8,144,120,24	296,8,144,120,24

Intel® Stratix® 10

INTEL® STRATIX® 10 MX (DRAM SYSTEM-IN-PACKAGE) PRODUCT TABLE

	PRODUCT LINE	MX 1100	MX 1650	MX 1650	MX 1650	MX 2100	MX 2100	MX 2100	MX 2100
Resources	Logic elements (LEs)[1]	1,092,000	1,679,000	1,679,000	1,679,000	2,073,000	2,073,000	2,073,000	2,073,000
	Adaptive logic modules (ALMs)	370,080	569,200	569,200	569,200	702,720	702,720	702,720	702,720
	ALM registers	1,480,320	2,276,800	2,276,800	2,276,800	2,810,880	2,810,880	2,810,880	2,810,880
	Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric							
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees							
	HBM2 high-bandwidth DRAM memory (GBytes)	3.25	8	16	8	8	8	16	8
	eSRAM memory blocks	1	2	2	2	2	2	2	2
	eSRAM memory size (Mb)	45	90	90	90	90	90	90	90
	M20K memory blocks	4,401	6,162	6,162	6,162	6,847	6,847	6,847	6,847
	M20K memory size (Mb)	86	120	120	120	134	134	134	134
	MLAB memory size (Mb)	6	9	9	9	11	11	11	11
	Variable-precision digital signal processing (DSP) blocks	2,520	3,326	3,326	3,326	3,960	3,960	3,960	3,960
	18 x 19 multipliers	5,040	6,652	6,652	6,652	7,920	7,920	7,920	7,920
	Peak fixed-point performance (TMACS)[2]	10.1	13.3	13.3	13.3	15.8	15.8	15.8	15.8
	Peak floating-point performance (TFLOPS)[3]	4.0	5.3	5.3	5.3	6.3	6.3	6.3	6.3
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection							
	Hard processor system	Quad-core 64 bit ARM* Cortex*-A53 up to 1.5 GHz with 32 KB I/D cache, NEON* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I²C x5, general-purpose timers x7, watchdog timer x4							
		Yes	–	–	–	–	–	–	–
	Maximum user I/O pins	448	656	656	584	640	656	656	584
	LVDS pairs 1.6 Gbps (RX or TX)	216	312	312	288	312	312	312	288
	Total full duplex transceiver count	48	96	96	96	48	96	96	96
	GXE transceiver count - PAM4 (up to 58 Gbps) or NRZ (up to 30 Gbps)	0	0	0	72	0	0	0	72
	GXT transceiver count - NRZ (up to 28.3 Gbps)	32	64	64	16	32	64	64	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	16	32	32	8	16	32	32	8
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	2	4	4	1	2	4	4	1
	100G Ethernet MAC (no FEC) hard IP blocks	2	4	4	1	2	4	4	1
	100G Ethernet MAC + FEC hard IP blocks	0	0	0	12	0	0	0	12
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys							
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[4, 5]									
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		448,16,216,48	–	–	–	–	–	–	–
F2597 pin (52.5 mm x 52.5 mm, 1.0mm pitch)		–	656, 32, 312, 96	656, 32, 312, 96	–	640, 16, 312, 48	656, 32, 312, 96	656, 32, 312, 96	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	584, 8, 288, 96	–	–	–	584, 8, 288, 96