TPC DAQ for Pilot Run

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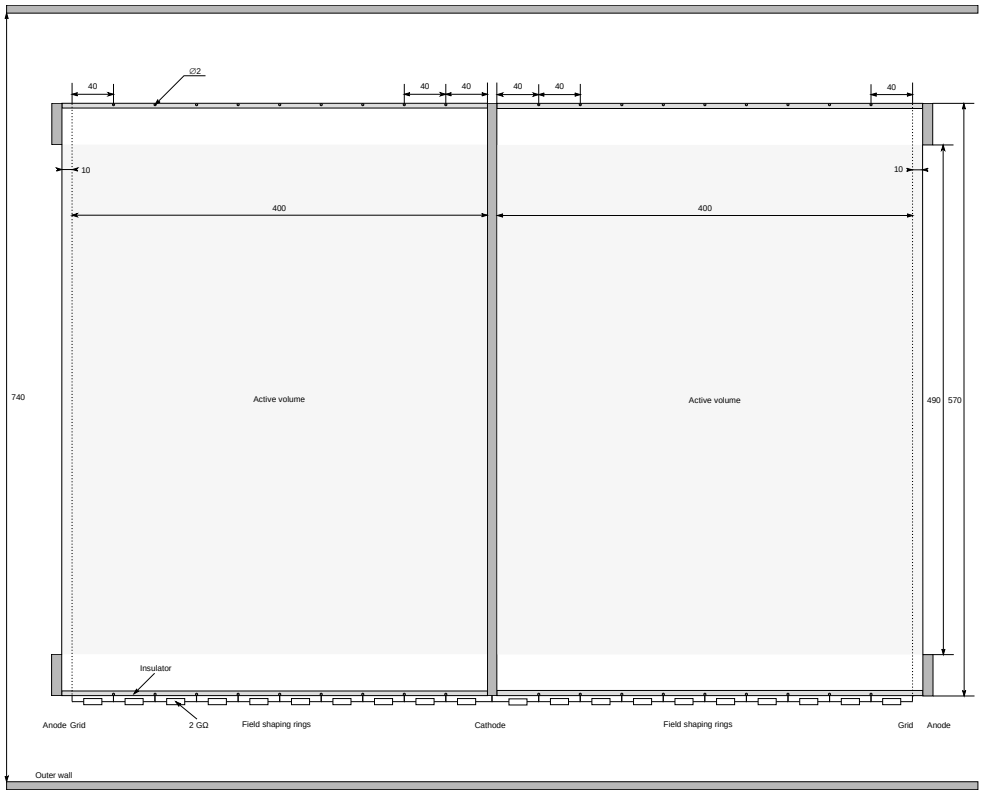
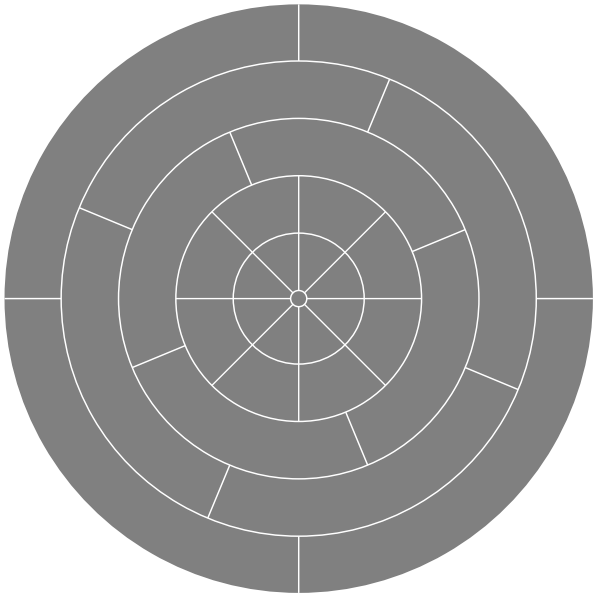
TPC for Pilot Run





Anode segmentation for Pilot Run:

- ~Half beam intensity on central pad
- Other half divided by 8 segments
- Less φ segments – less track splitting

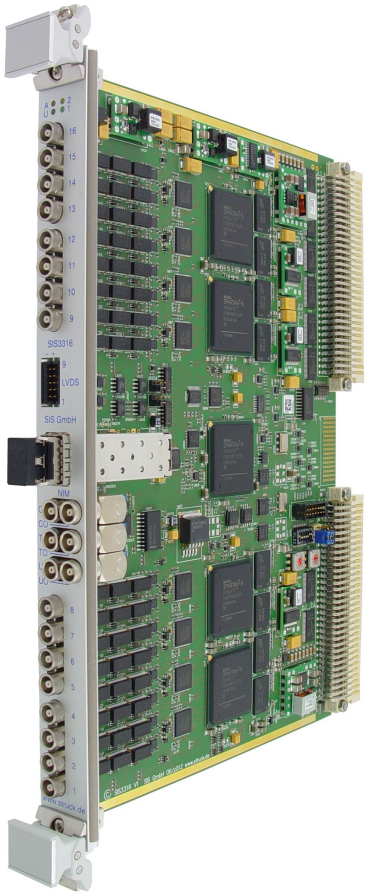
Planned readout

- Continuous trigger-less readout of raw TPC signals
- Timestamp synchronization in FADC firmware

Resolution requirements

- Energy: 20 keV
  - Demonstrated with 1.4 μs preamps in the test run
- Time: 40 ns
  - Demonstrated with 1.4 μs preamps in the test run
  - Z_v can be reconstructed with sufficient precision (e. g. using MVA)

Struck SIS3316 VME FADC



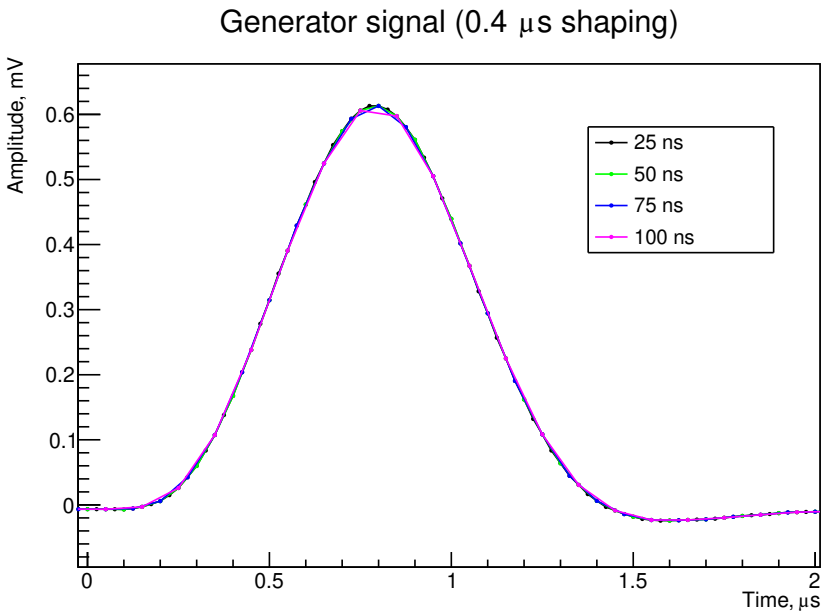
- Single width 6U VME card
- 16 channels
- 250 MSPS per channel (simultaneous sampling)
- 14-bit resolution
- 64 MSamples memory/channel
- Two programmable input ranges
- Offset DACs
- Internal/External clock
- Multi event mode
- Double bank mode
- Readout in parallel to acquisition
- Pre/Post trigger capability
- Internal trigger generation
- Trigger OR output (16 individual thresholds)
- Front panel clock/trigger bus (FP-Bus)
- LEMO NIM Clock, Trigger and User (Veto) in
- LEMO NIM Clock, Trigger and User out
- SFP cage (Gigabit Ethernet or Multi-Gigabit optical link connection)
- A32 / D32 / BLT32 / MBLT64 / 2eVME / SSTVME
- In field JTAG and VME firmware upgrade capability

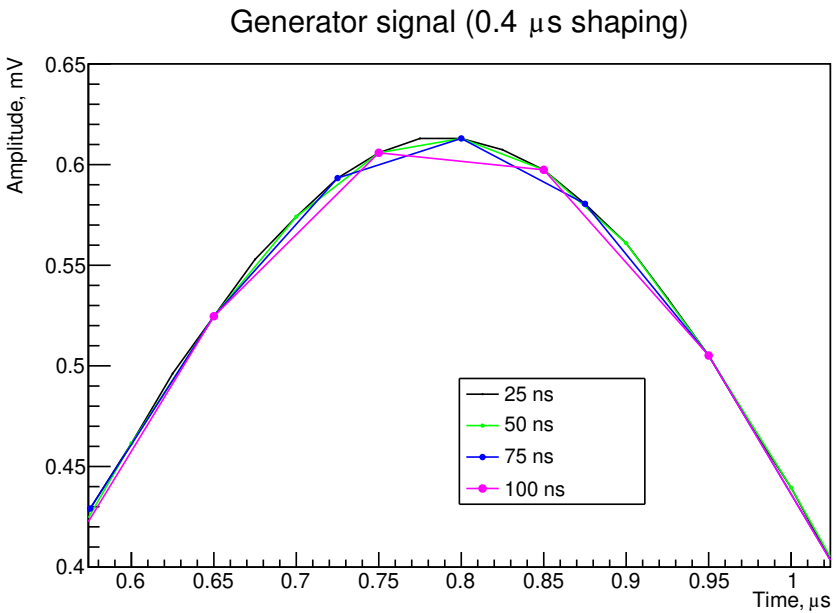
SIS3316 modifications

- Fast 1Gb/s Ethernet readout *tested*
  - 25 MHz * 2 Bytes * 16 channels = 800 MB/s + overhead (more FADCs?)
  - 60 channels (4 FADCs): 3 GB/s
  - Main run (~160 channels): 8 GB/s
- Timestamp processing in firmware *needs testing*
- Lossless trace compression[1] (~70%) *in progress*
  - 800 MB/s → ~250MB/s

[1] DPTC, G. Bruni et al. https://doi.org/10.1109/TCSI.2019.2945179

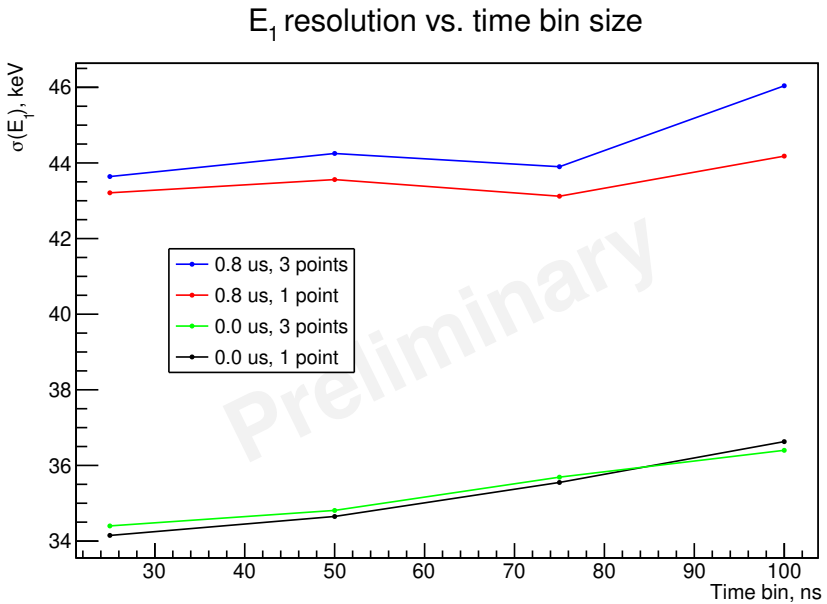
Signal downsampling

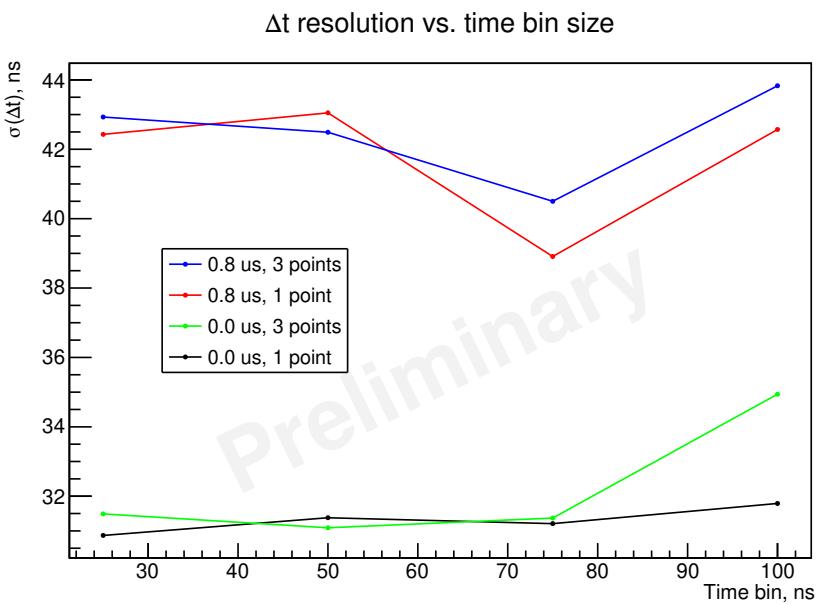




650 keV, fast signal (0.1° recoil angle)

Signal downsampling





- 20 MHz → 10 MHz: -6% energy, -12% time resolution
- Fine-tuned parameters for fast signals (small recoil angle)
- Low E resolution: short shaping time (0.4 μs), poor lab conditions (noise, pickups)

Plan B

- Fast readout, no compression:
  - Lower sampling rate
    - Time sync with Si/SciFi must remain precise for Z_v calculation
- No fast readout (<100 MB/s VME):
  - Self-triggering mode (FADC internal trigger)
- No timestamp processing in FADCs:
  - External module?

Online monitoring

- Must-haves:
  - TPC count rates (individual/plane) – FADC(?)/software discriminator (MAW)
  - Energy spectra (individual/ring/plane)
  - Generator spectra for each channel (on- and off-spill, external signal)
  - Alpha spectra (off-spill or separated from recoil by energy/location)
- Good to have:
  - Correlation with Si tracker and SciFis

Thank you!

Reduced sampling rate data rates

- (19.44 MHz * 2 Bytes * 16 ch)×30% ≈ 187 MB/s
- (19.44 MHz * 2 Bytes * 8 ch)×30% ≈ 93 MB/s (8 FADC boards)
  - Option: reduce number of used FADC channels
- 60 channels + compression: **~700 MB/s**