



Boost your high bandwidth data acquisition
by adding OpenCAPI and memory coherency to FPGA

Introduction to OpenPOWER

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Toshaan Bharvani (toshywoshy)

- From Antwerp, Belgium
- IT Engineer / Consultant / Trainer @ VanTosh
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- Involved in Open Source
- Involved with Enterprise OS : PowerEL, CentOS, RHEL, IBM AIX, IBM z/OS, BSD, ...
- Provide virtual container solutions : KVM, Podman, PowerVM, z/VM, OpenStack, OpenNebula, ...
- Provide automation CfgMgmt / DevOps : Ansible, Foreman, mgmtconfig, Puppet, ...
- Security focused : SELinux, OWASP, WebSec, ...
- Involved in hardware, software and conferences
- OpenPOWER Foundation : Silver 2017 & TSC Chair 2020
- Twitter : [@toshywoshy](https://twitter.com/toshywoshy)
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Introduction

OpenPOWER Foundation History

- Founded in 2013
- More than 300+ members
- Working Groups lead initiatives for members to work together
- New Leadership in 2019
 - More than just specification driven
 - More reference & product driven again
 - Software & Hardware combination
 - New interaction with the wider community
- Board Members :
 - Artem Ikoiev (Chairman) - YADRO
 - Mendy Furmanek (President) - IBM
 - James Kulina (Executive Director) - OpenPOWER Foundation
 - James Huang (Director) - Inspur Power Systems
 - Tim Ansell (Director) - Google
 - Timothy Pearson (Director) - Raptor Computing Systems
 - Sameer Shende (Director) - University of Oregon

OpenPOWER Foundation Future

- Goals :
 - To create an open ecosystem around the OpenPOWER Architecture
 - To create specifications and documentation on the OpenPOWER Architecture
 - To create reference designs of OpenPOWER Architecture
 - To create value for OpenPOWER Foundation Members
- Focus Areas :
 - Build Academic communities for multi-discipline incentives
 - Build Developer communities across the entire Open Source landscape
 - Build Silicon/Chiplet communities for integrated solutions
- Moving towards being an Open Foundation from all levels
 - POWER ISA
 - Hardware Architecture
 - Interfaces : OpenCAPI / OMI
 - Software enablement : OPF HUB
 - Running the foundation on OpenPOWER

OpenPOWER Working Groups

- Technical Work Group (TWG)
 - POWER ISA TWG
 - Accelerator TWG
 - Memory TWG (OMI ↔ OpenCAPI)
 - Compliance TWG
- Special Integration Group (SIG)
 - LibreBMC SIG
 - HPC SIG¹ (↔ HPC OCP)
 - POWERpi SIG²
 - Machine Learning & AI SIG (↔ LF AI/DATA)
- OpenPOWER READY
- OpenPOWER HUB
- OpenPOWER Ambassadors

¹being stood up

²being stood up

OpenCAPI

- Coherent Accelerator Processor Interface (CAPI)
- Designed by IBM for IBM POWER8
- Consortium created in 2016
- Currently implemented on POWER8, POWER9, POWER10, ...
- However other architectures are working on their implementations
- OpenCAPI is all about Coherent Acceleration
 - I/O
 - Memory
 - Storage
 - Processing
- Other players on the market :
 - Gen-Z
 - CCIX
 - TileLink

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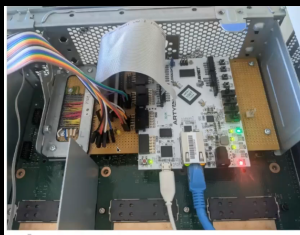
Acceleration

Accelerator WG

- Getting Acceleration into OpenPOWER
- Working on getting FPGA tooling better in open source
- Working on ASIC, FPGA, GPGPU, . . . Acceleration
- Acceleration Specifications for
 - HPC applications
 - Business applications
 - Academic applications

LibreBMC SIG

- Build an Open Source Base Management Controller
- Using an FPGA as board design
- Use a POWER softcore (Microwatt)
- Fully open source, software, hardware and implementation



POWER ISA TWG (1)

- OpenPOWER ISA
 - POWER1 → POWER3 (POWER ISA v1)
 - POWER4 → POWER8 (PowerPC ISA v2)
 - POWER9 → POWER? (OpenPOWER ISA v3)
 - POWER10 has 1419 instruction of which 246 are new

OpenPOWER Books

- Book I : User Instruction Set Architecture
- Book II : Virtual Environment Architecture
- Book III : Operating Environment Architecture
- Anyone, skill permitting, can contribute
- Opening the documentation
- New RFC process
- Listen to Core Designer feedback

POWER ISA TWG (2)

Compliance Instruction Sub-Sets

- Full : Complete Subset (including optional) [1419i (320i)]
 - Copy-paste-accel (CPA), Non-coherent-mem (M=0), Matrix-math-assist (MMA) Secure-mem-facility (SMF), Wr-tru-req-mem (W=1), Data-stream-prefetch (STM), Power-management (PM)
- ACS : AIX Subset (BE) [1099i]
 - AIL-HAIL-programmability, EVIRT-programmability, Quad-prec-float (QFP), Atomic-mem-ops (AMO), SLB/HPT xlate, Decimal-float (DFP), Big-endian (BE), Proc-compat-reg (PCR), Load-store-multiple (LM), Branch-history-buf (BHRB), Broadcast-TLBIE Load-store-string (LS), Event-based-branch (EBB), Control-reg (CTRL), SMT
- LCS : Linux Subset (LE) [962i]
 - SIMD-VMX-VSX, SF=1 (64-bit mode), Nested radix xlate (ROR), LE-mode, OV modifying ops, LPAR
- SFFS : Scalar Fixed-Point + Floating-Point Subset [214i]
- SFS : Scalar Fixed-Point Subset [129i]

OpenPOWER Cores

- Microwatt
- A2I
- A2O
- Libre-SOC
- Chips11
- A2P
- VexPOWER

HPC SIG³

High Performance Computing Special Integration Group

- Work with HPC OCP design to enable more OpenPOWER usage
- Will design and build reference design for HPC workloads
- Will engage with the HPC software community to make HPC software ported to ppc64le
- Is currently focussed on getting OMI adoption more wide spread

³SIG still to be stood up, charter being worked on

POWER π SIG⁴

- Embedded Single Board Computer (SBC)
- Will have several versions and generations
 - Dual Core vs Quad Core
 - OMI acceleration
 - BMC integrated
 - ...
- Enablement platform for developers
 - "I can put it on/under my desk"

⁴SIG still to be stood up, initial charter draft

Conclusion

OpenPOWER + OpenCAPI (OMI) + FPGA
⇒ ACCELERATION

emPOWER your **SPEED**

The End



Thank You for your attention



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