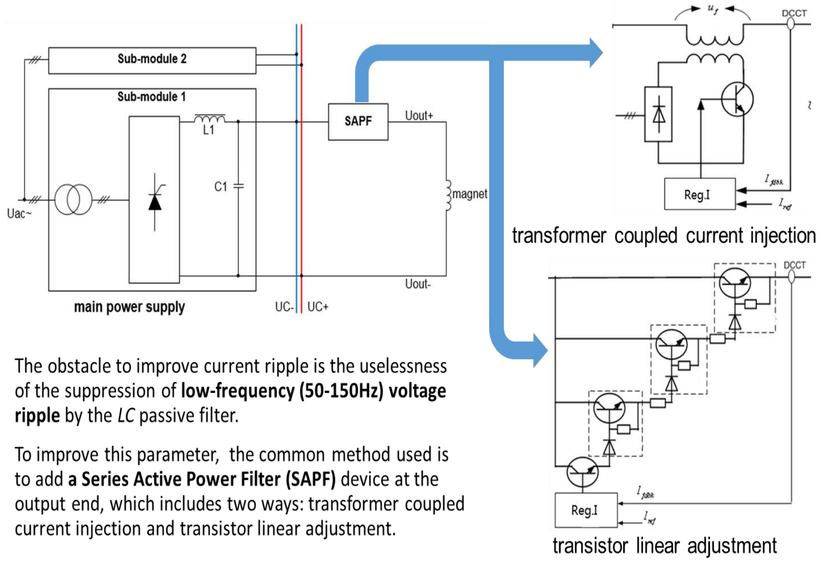
Design and study of a novel series active filter for the 10MW-level high power and high stability DC power supply

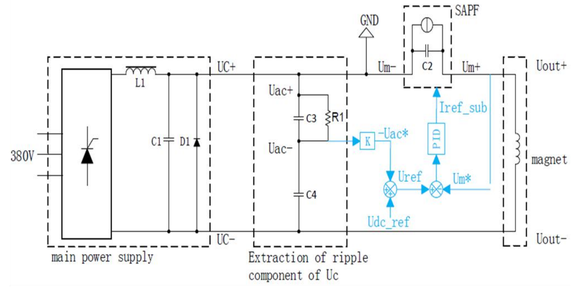
1. SAPF for 10MW-level high power and high stability DC power supply



The obstacle to improve current ripple is the uselessness of the suppression of **low-frequency (50-150Hz) voltage ripple** by the *LC* passive filter.

To improve this parameter, the common method used is to add **a Series Active Power Filter (SAPF)** device at the output end, which includes two ways: transformer coupled current injection and transistor linear adjustment.

2. Operating Principle of the novel SAPF



2. The voltage set value of SAPF is set to:

$$U_{ref} = -U_{ac}{}^{*} + U_{dc\_ref} > 0$$

The novel SAPF only works in the first quadrant.

1. The novel SAPF is designed as a voltage source that directly tracks the negative value of the output voltage ripple of the main power supply ($-U_{ac}{}^{*}$).

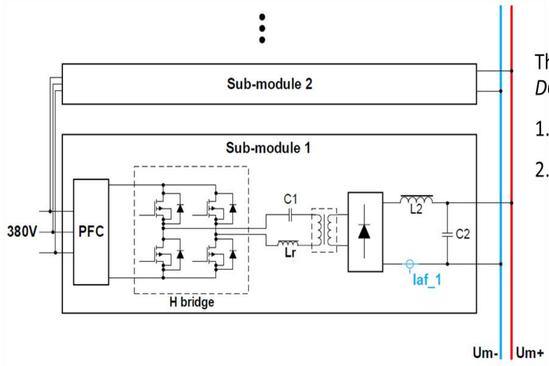
if its response speed is fast enough, it can be regarded as an ideal voltage source. Then **it can be directly connected in series with the main power supply without changing its control strategy.**

3. Working sequence of main power supply and SAPF:

(1) The SAPF is started first to control the rise of magnet current by controlling the rise rate of U_{dc_ref}. **It can effectively solve the problem of uneven output waveform in the initial stage of current climbing.**

(2) When the output voltage of the SAPF is stabilized, the main power supply is started to control the magnet current according to the given rise rate and final value.

3. Topology structure of the novel SAPF



The novel SAPF is a conventional *AC-DC-DC* switching power supply:

1. It only works in the first quadrant.
2. It is designed as a voltage source, capable of effectively tracking signals up to *300Hz*.

- It is feasible to refer to the design rules of conventional switching power supply when selecting the related device parameters.
- extra attention should be paid to the parameter selection of output capacitance *C2* (equivalent output capacitance value).

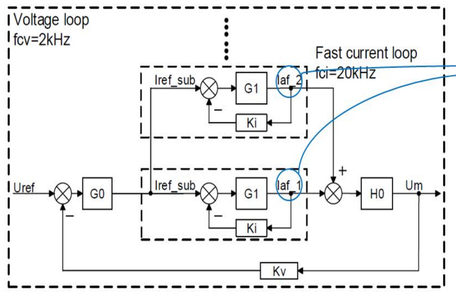
It is recommended that C2 be calculated according to the following formula:

$$\frac{I_{C2}}{I_{out}/n} \geq 1\%$$

I_{C2} → Current flowing through *C2*

I_{out}/n → Number of submodules / Magnet current

4. Control policy of the novel SAPF



Iaf_k is taken from the current before the *LC* passive filter, or the primary current of the high-frequency transformer.

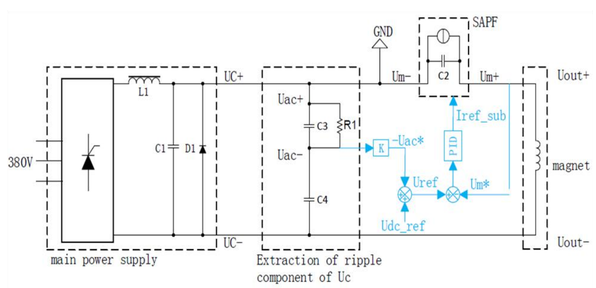
- 1. Fast current inner loop is used to realize automatic current equalization between sub-modules.

If the response speed of the fast current loop is fast enough, the sub-module can be considered as an ideal current source. Theoretically, infinite sub-modules can be directly connected in parallel to obtain a larger output current.

The recommended response speed of the **current loop is *10* times that of the voltage loop.**

2. The total voltage loop is used to track the output voltage ripple of the main power supply in real time. In order to achieve effective tracking of **the maximum frequency of *300Hz***, it is reasonable to design **the bandwidth of the voltage loop as *2kHz***.

5. Extraction of the output voltage ripple of the main power supply



- The extraction ratio of the AC component on *Uc* is:

$$K_1 = C_4 / C_3$$

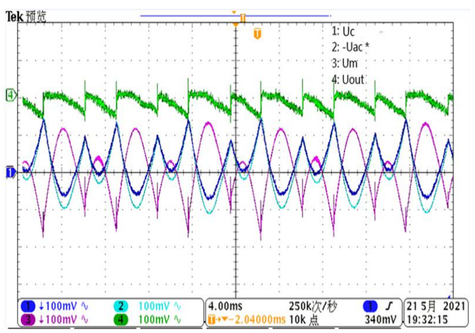
- The extraction of the DC component on Uc is:

$$K_2 = R_1 / R_{C4}$$

insulation resistance of *C4*

- 1. The novel SAPF is in operation during the whole period of the power system. In the whole process, the output voltage of the main power supply **contains a large *DC* component** in addition to a small number of low-frequency ripple components. And the DC component **changes dynamically** in the process of current rising and steady state, and the variation changes in a **large scale**.
- 2. The extraction scheme needs to meet two requirements: **first, the extraction of low-frequency AC components** needs no delay and precise; **second, reduce the *DC* component** as much as possible, in order to avoid the feedback controller quickly saturated and then lose control.
- 3. **Common extraction schemes** include analog filters (low-pass or bandpass filters), or digital filters. In addition to the **delay problem**, the conventional extraction method may also cause a ***180°* phase shift** in a certain frequency band, which will eventually amplify the ripple voltage and then lead to the power supply output oscillation.

6. Experimental verification



- Experimental results:
- 1. The ripple components in *Uc* are mainly *150Hz* and *300Hz*.
- 2. Peak-to-peak value of *Uc* is about *0.2V*.
- **3. *–Uac** is basically coincident with *Uc*, and there is no phase lag.**
- **4. *Um* and *–Uac** basically coincide, and there is no phase lag.**
- **5. Peak-to-peak value of *Uout* after novel SAPF filtering is about *50mV*.**

- Related experimental parameters:
- 1. Main power supply is a ***50V50A* SCR rectifier bridge**.
- 2. The dummy load is ***5m*H/0.7ohms** copper coil**.**
- 3. The small prototype uses two groups of sub-modules in **parallel**. Each submodule outputs 10V30A.
- 4. The **response speed** of the **current inner loop** is designed as ***20kHz***, and the voltage outer loop is designed as *2kHz*.
- 5. H bridge adopts silicon carbide *MOSFET*, and the **working frequency is *100kHz***.
- 6. According to the above calculation formula, the **output capacitance *C2* is set to *1.6mF***. Accordingly, the output capacitance of each submodule is set to *0.8mF*.