200th Meeting of the Machine Protection Panel

Injectors topics

December 4th, 2020 via Zoom

Participants:

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The slides of all presentations can be found on the website of the Machine Protection Panel and on Indico (200th meeting).

Minutes from the 199th MPP meeting (LHC topics)

The minutes of the 199th MPP meeting were not available at the time of the meeting.

BLMs in the injectors (PS, PSB, Linac4)

Overview and architecture (Christos Zamantzas)

Christos introduced the scope of the injectors BLM project. The project aims to build a generic, highly configurable system, with the acquisition layer able to work with multiple detector types and using reprogrammable parts so that all the injector requirements can be met. The system architecture is similar to the one of the LHC BLM system. The electronics is not radiation tolerant and will therefore be located outside the radiation area of the machines. The acquisition layer is based on an FPGA with two acquisitions modes. The processing layer collects the data and processes the running sums. They are sent to the combiner which connects to the interlock system or to the CPU. The high-voltage power supply is controlled by the combiner. A signal can be injected in the detectors to allow a test of the whole acquisition and processing chain.

The system was deployed in Linac4 in 2016, in the PSB & PS rings during the 2016-17 EYETS and to all transfer lines during LS2. The legacy systems have been decommissioned during LS2. The new system has 291 ionization chambers of the LHC type, 32 flat ionization chambers FIC, developed to fit in-between the beam pipes of the PSB and 25 diamond detectors. A total

of 14 racks are deployed, this used to be 3 racks before LS2, and 2 OASIS systems are used to acquire the signals from the diamond detectors.

A new coaxial cable with triple shielding was developed in partnership with DRAKA to prevent electromagnetic interference issues. A triaxial connector, developed in partnership with POLAMCO has been developed for the new shielded coaxial cable. In addition, the high voltage cable screens are open on the IC side to remove the ground loop (the ICs are floating).

The dynamic range of the current acquisition goes from 10 pA to 200 mA. Two acquisition methods are in place, with overlapping ranges, to cover the full range without gain change. The switch between the two ranges is managed by the FPGA. The sum of all parts is calculated in the acquisition FPGA and transmitted as a 2 micro-second integral. The acquisition module acquires signals with an internal clock (asynchronous to the beam). A synchronization is required with the start of the cycle and is achieved using the timing signals coming from a timing card included in the system.

The software layer is an integral part of the system and performs the following functions:

- Remote firmware deployment.
- Configuration parameters.
- Group detectors into per-destination-families and publish them accordingly.
- Concentrate data from multiple cards or crates.
- Tracking of loss limits per user.

The interlock functionality is split in two parts: the hardware implementation performs the machine protection aspects, while the software implementation is used to limit radiation levels due to repeated beam losses. For the HW part, all running sums are checked against their threshold values at each refresh period (every 2 microseconds). In case the measured values exceed one of the thresholds, the beam permit will be removed for all users. The blocked beam permit will be latched until an operator acknowledges. For the SW part, each integration period value is checked against a second set of thresholds which is user dependent. The comparison happens at the end of every cycle and if the measurement exceeds the threshold, the beam permit is removed for the user. The blocked beam permit signal for this user is latched until an operator acknowledges.

Questions and comments:

Andrzej asked what procedure will be followed to determine the hardware thresholds. Christos replied that the operational (software) thresholds will be set during operation. The hardware thresholds will not be used immediately and will be determined by the BLM threshold working group. They will be used when the full LIU beams will be available, after establishing operational experience. Both limits (HW and SW) interlock the BIS, except in the case of the PS where it goes to the tail clipper as it is the only machine without a BIS.

Jorg commented that in the case of the SPS, the thresholds are set close to the operational losses. For the SPS arcs the thresholds are then set orders of magnitude below the damage threshold.

Daniel asked how the processing distinguishes the two sets of thresholds. Christos replied that the hardware thresholds are stored in the processing electronics and the software thresholds are stored in the CPU unit. The threshold values come from INCA in both cases.

Jan asked if both types of interlocks go to the BIS. Christos confirmed that they do.

Andrea asked about the injection in the PSB and the determination of the H- dump thresholds. Christos replied that 6 ICs and 8 diamond detectors are located in that region. Bettina commented that the H0/H- beam current monitors will be the main element for the protection of the H- dump. It has to be calibrated at the start of the commissioning.

Christos added that after LS3 three different systems will be in place: the injectors system (presented here) will cover all injectors up to TT10 (included). The SPS and its extraction lines will be covered by the new LHC-type BLM system, while the LHC will remain on the prior LHC BLM system.

Systems deployment (William Vigano)

William presented the status of the deployment: 15 racks have been installed, 14 VME crates, 9 acquisition crates, 51 processing cards, 51 acquisition cards and a total of 322 detectors. The racks installation is unified over all the machines. For Linac4, special floor supports have been put in place to position the detectors. Flat ionization chambers (32 in total) have been installed in the booster to cover the two bottom-most and the two upper-most beam pipes. Regular IC detectors are installed in all the PSB transfer lines (injection and all extraction lines, including ISOLDE). 100 ionization chambers and 17 diamond detectors are installed on top of the PS main magnets. For the TT2 line, 42 detectors are installed. Due to the space limitation, a new cabling system has been put in place: the detectors are grouped, and distribution boxes collect the signals from the detectors of the group and distribute them. Ionization chambers have been installed in the FTA line (4) and in the nTOF target area (6). 28 detectors are installed in the TT10 beamline. All installations are completed, except for 8 detectors in the East Area target zone and 3 for the East Area transfer line.

A failsafe high voltage distribution system has been designed. It features 2 inputs and 64 output channels (limited to 2 mA and 1500 V). It has a double power supply input and is tolerant to the failure of a single input. It is also tolerant to a permanent short-circuit. In addition, it is able to discharge the internal capacitors of the detectors.

The system is able to superimpose a modulation to the high voltage of the detectors. This allows to test the complete acquisition chain: the modulation induces a pico-ampere current proportional to the input.

Questions and comments

Daniel asked is there is a mechanism in place to prevent a detector from drawing too much current from the distribution system. William replied that the high-voltage distribution ensures that all outputs will be able to provide 2 mA even if one of them fails. Christos added that the protection put in place by the distribution mechanism is in place for human protection primarily. Each channel has its own bias voltage cable, and they are all individually powered.

Jan asked how often the high voltage modulation test will be performed. William replied that the possibility to keep a constant modulation (and to filter it out from the acquisition) has been studied. However, at the moment it is planned to manually run the test. This should be run on a daily basis. Christos added that there is enough time without beam at the start of the cycle to

run the modulation. The system can be checked during that time window. It is foreseen to deploy the constant modulation in a second stage.

Upon a question from Frank, William commented that the East Area deployment will take place in January-February 2021.

Ruben asked about the two diamond BLMs in CHARM. They will not be touched, as they are of the LHC type.

Acquisition principle (Eva Calvo Giraldo)

Eva first presented the characteristics of the acquisition card (BLEDP, front end electronics). It has 8 independent acquisition channels. The dynamic range extends from 10 pA to 200 mA, using two acquisition methods with overlapping ranges: the fully differential frequency converter (FDFC), active from 10 pA to 10 mA, and the direct digital to analog conversion (DADC), active from 10 µA to 200 mA. The minimum acquisition period is 2 micro-second. The digitized value is transmitted through optical fiber to the post-processing module or through Ethernet to a client application, if the stand-alone mode is in use.

Eva presented the details of the FDFC acquisition method. The FPGA will automatically inhibit the FDFC chains and switches to the DADC. The input to the FPGA is fundamentally different depending on which acquisition method is used. The FPGA will reconstruct the integral between samples.

The system has been fully simulated with various input signals before being implemented in the FPGA.

Data processing and measurements (Mathieu Saccani)

Mathieu detailed the new processing electronics (BLMINJ). Three firmware codes are developed, for a total of 18 FPGAs. The same firmware version is deployed for all the injectors. The hardware is common to all machines, but the configuration depends on the machine. The following data streams are considered:

- The on-line controls (input)
- The on-line displays (output)
- The logging data (for database storage) (output)
- The parameters database (input)
- The timing information (input)
- The BIC (output).

The timing telegram is received by the local CTRV and the LTIM signals are distributed to the FPGAs. Four timing events are used: the start of BP, the start of cycle, the beam in and out events.

The loss measurement acquisition is treated as 31 bits samples transferred at a 2 micro-second rate. After processing, the buffers, integrations and running sums are published at the BP rate (1.2 s). There is no synchronization, the system is in free-running acquisition and potential jitters can appear in the measurements. Two buffers are used, one for reading and one for writing, the system toggles between the two at each BP.

The integrals of the 2 micro-seconds samples are reset based on the cycle timings and are published at each BP. The threshold comparator is active at all times in between. Four types of measurements are defined:

- Loss over the whole cycle (published at each BP but only reset at the end of the cycle)
- Loss over basic period (reset at each BP)
- Loss over beam presence (similar to the loss over cycle but starts only after the beam in timing)
- Loss over ambient (background) which is active only outside the beam presence period; it is published at each BP and reset at the end of the cycle

The running sums are implemented using a variable length shift register. Three running sums are defined: 1 sample (2 μs), 300 samples (600 μs) and 500 samples (1 ms). The maximum over a BP is published (and reset at each BP). The threshold comparison is performed continuously (for each sample).

The diagnostics values, errors and states are published at all BP.

Diagnostics and losses are compared to thresholds to produce errors. The acquisition board, the processing board and the software produce maskable errors. HW and SW interlocks are generated. The hardware interlocks are sent to two CIBUs. The SW interlocks are also sent to two CIBUs. Watchdogs are also present to generate interlocks, they must be re-armed periodically. All outputs to the CIBUs are first sent to the combiner board (BLECS).

The control parameters are sent to the electronics via the CPU. The parameters are saved locally (FLASH memory) and can be updated with the INCA values.

The firmware has been validated using three test-benches and an additional one for the integration testing. The firmware is also validated in the lab, using timing signals.

Questions and comments:

Jan asked if the CTRB interface is protected and if it is set via FESA. Mathieu replied that it is done at the SW level. There is no RBAC protection for these. At the moment the values can be changed via the FESA navigator.

Action: Propose how to protect the CTRB interface of the BLMs to the timing system against accidental changes and overwriting via FESA, in collaboration with the timing team (S. Jackson, J. Uythoven).

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Daniel asked at which rate the threshold comparison is performed. Mathieu replied that it is done at the clock rate of the FPGA but that the data only changes every 2 μs.

Daniel asked how the diagnostics is performed if an interlock is generated. Mathieu replied that it is visible in the application; it is possible to identify what triggered the interlock.

Software and controls (David Medina Godoy)

David presented the crate configuration and the FESA instantiation. Some crates have monitors that belong to different accelerator zones and the INCA settings should be split within the crate. To overcome this problem, the monitors are grouped in families. There is one FESA device per family in the crate. A maximum of 8 families is allowed. As an example, the *cfv-361-blmbt* instantiates 4 FESA devices: BT.BLM, BTM.BLM, BTP.BLM and BTY.BLM.

Three configurations are deployed: Linac4 & PSB, PS ring and TT10. At the electronics level, the PS configuration is different from the other two as it does not have a connection to the BIS. At the FESA level, the PS configuration features a connection to the tail clipper and the TT10 configuration features a connection to the SPS SIS. All configurations provide LASER alarms. Virtual FESA devices for each monitor are provided in the Linac4&PSB and PS ring configurations. The OP GUI is built using the information from the virtual FESA devices. The expert GUI uses directly the main FESA class. The diagnostics data from the main class are logged with NXCALS. The operational data (virtual devices) are processed with a UCAP node and sent to NXCALS.

The monitors of the PS ring are split over two VME crates. They are concentrated with the "BLMSYNC". It adds one loss type measurement: the sum of all losses from all monitors. It is interlocked, can be masked and provides alarms. It can also act on the tail clipper LTIM to provide an interlock. The "beam loss evolution" Vistar fixed display of the PS uses the data from the BLMSYNC. The sum of the losses for each monitor is calculated and published every 100 ms.

For TT10, a "summary acquisition" property is added, to retrieve the data from the possibly two injections. A special timing configuration is used. The TT10 configuration publishes data read by the SW interlock after each injection, to be used by the SPS SIS.

Commissioning status (Mathieu Saccani)

Mathieu summarized the commissioning status:

- LINAC4: installation and dry-run successful.
- PSB: installation and dry-run successful, the modulation test on all 104 channels is functional.
- PS Ring: installation done and tested.
- East Area: installation on-going, individual system tests (IST) not yet done. The modulation tests must be done. The VME crate is operational.
- TT2: installation and modulation tests done. Noise peaks in the cables detected in the switchyards area.
- TT10: installation is done.

Summary of actions

The actions from the meeting are:

- Data processing and measurements:

1. Propose how to protect the CTRB interface of the BLMs to the timing system against accidental changes and overwriting via FESA, in collaboration with the timing team (S. Jackson, J. Uythoven)