

# MPP Meeting BLMINJ Acquisition

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#### **1. BLMINJ Electronics**

- BLEDP card
- FDFC and DADC acquisition modes

### 2. FPGA logic

- Data combination
- Automatic switching logic









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### Introduction





## **Acquisition card: BLEDP**



#### Main characteristics:

- 8 independent acquisition channels per card
- Measurement range : 10pA to 200 mA (2.10<sup>10</sup>), using 2 acquisition methods with overlapping dynamic ranges:
  - Fully Differential Frequency Coverter (FDFC) : 10pA-10mA
  - Direct Digital to Analog Conversion (DADC) of the current through a shunt reference: 100uA-200mA
- Minimum acquisition period is 2 us
- The digitised value is transmitted through optical fiber to the post-processing module or through a Gigabit Ethernet link to a client application (stand-alone mode)
- Both acquisition chains are acquired with the same ADC.
- No gain change required
- The switching between the 2 ranges is managed by the FPGA and is independent to each channel.





### Principle of the FDFC acq. method



- A charge-balanced differential integrator circuit integrates the current from the beam loss detector.
- Two comparators check the voltage of each branch against a threshold. Whenever the any of the voltages
  exceeds the threshold, the signals controlling the switches change to their complementary and the input
  current is then routed to the other integrator branch.
- A 16-bit ADC periodically samples the differential voltage at the integrator output.



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## Acquisition method switching (I)





### Acquisition method switching (II)





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### Data combination for the FDFC acq. Mode (II)



- In order to evaluate the integral between two samples the algorithm needs to cover eight cases.
- By tracking the slope and using the absolute value of the differences the realisation in the FPGA is significantly optimised.



 The above is for an ideal circuit. In reality additional stages are introduced to compensate for switching delays and other effects.

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1.1	A <sub>n+1</sub> -A <sub>n</sub>
1.2	A <sub>n</sub> -A <sub>n+1</sub>
2.1	$(max-A_n) + (max-A_{n+1})$
2.2	$(A_n - min) + (A_{n+1} - min)$
3.1	$(max-A_n) + (max-A_{n+1}) + (M-1) * (max-min)$
3.2	$(A_n-min) + (A_{n+1}-min) + (M-1) * (max-min)$
4.1	(A <sub>n</sub> -min) + (max-A <sub>n+1</sub> ) + (M-1) * (max- min)
4.2	$(max-A_n) + (A_{n+1}-min) + (M-1) * (max-min)$

Calculation

Case



### Automatic acq. method switching



- Default mode at startup is FDFC
- Every time we receive a new sample, the next sample is estimated based on the increment seen between the last two (using a linear interpolation).
- If the estimated value goes beyond the switching threshold, the command to change switches position is sent.



- Switches are not instantaneous. So the first FDFC sample did not integrate all the current.
- After switching, a previous FDFC sample is estimated, assuming that for about ~100ns the last DADC current calculated was constant and integrated.



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### **Python simulations**





### HDL simulation (I)





### HDL simulation (II)

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### Lab demo (I)





### Lab demo (II)







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