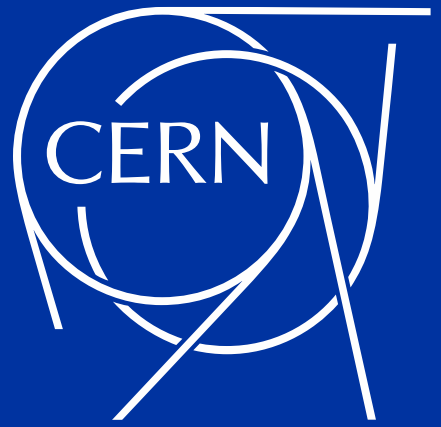


MPP Meeting
BLMINJ Processing & Measurements

Mathieu Saccani, Digital Electronics, BE-BI-BL

04/12/2020

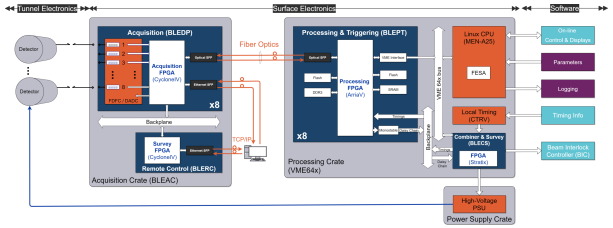
Outline

1. **BLMINJ Electronics**

2. **FPGA Data Streams**
   - Timings events
   - Loss measurements
   - System Self Monitoring
   - Diagnostics
   - Controls and Parameters

3. **Firmware Validation**

Outline



1. **BLMINJ Electronics**

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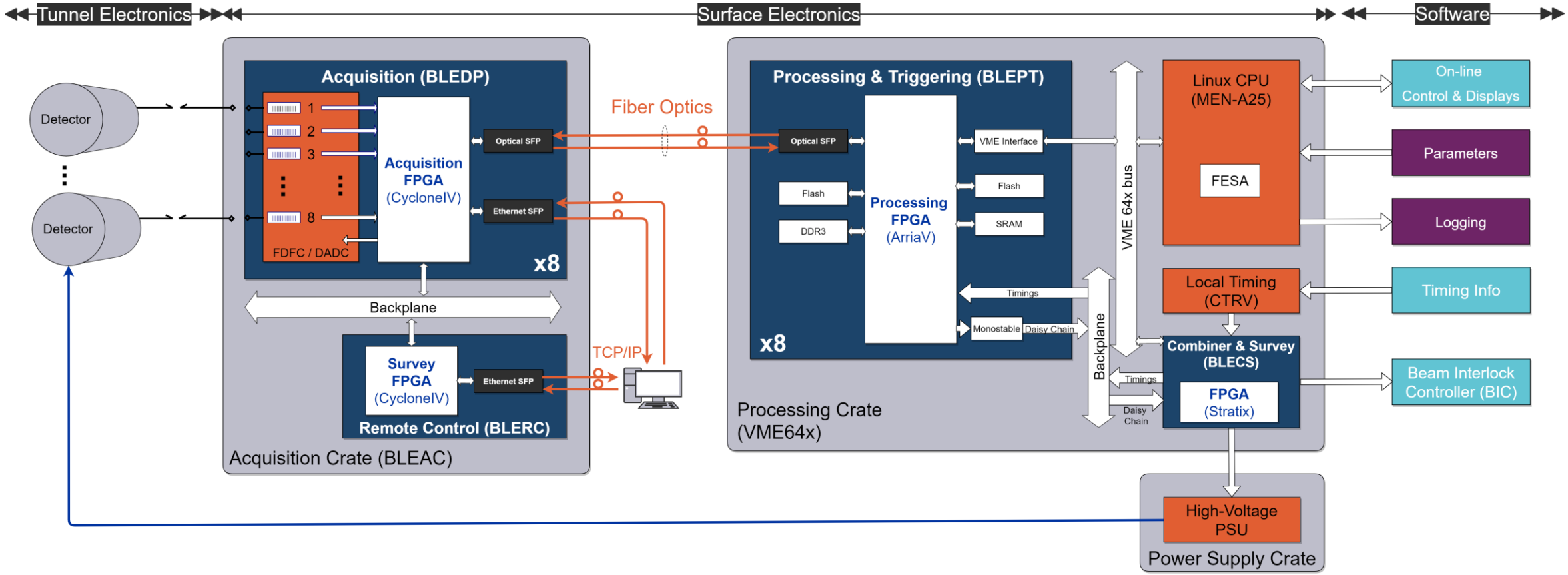
3. **Firmware Validation**

System Electronics

- ✓ **3 Firmware** (for 18 FPGA), 8*BLEPD, 8*BLEPT, 1*BLECS, 1*BLERC (not yet deployed)
- ✓ **New CPU**: MEN-A20 (Intel-L865) replaced by **MEN-A25** (Xeon D-1500)
- ✓ **New Processing board**: DAB64x (Stratix) + Mezzanine (CycloneIV) replaced by **VFC-HD** (ArriaV)



Outline

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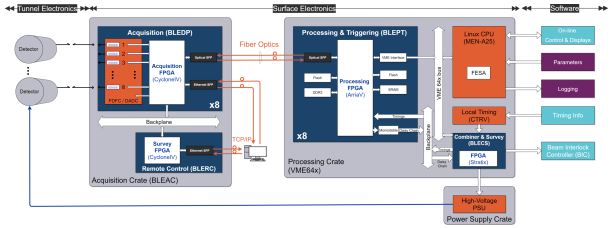

2. FPGA Data Streams

- Timings events
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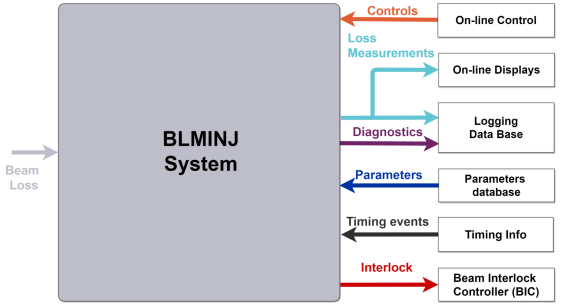
- System Self Monitoring
- Diagnostics
- Controls and Parameters

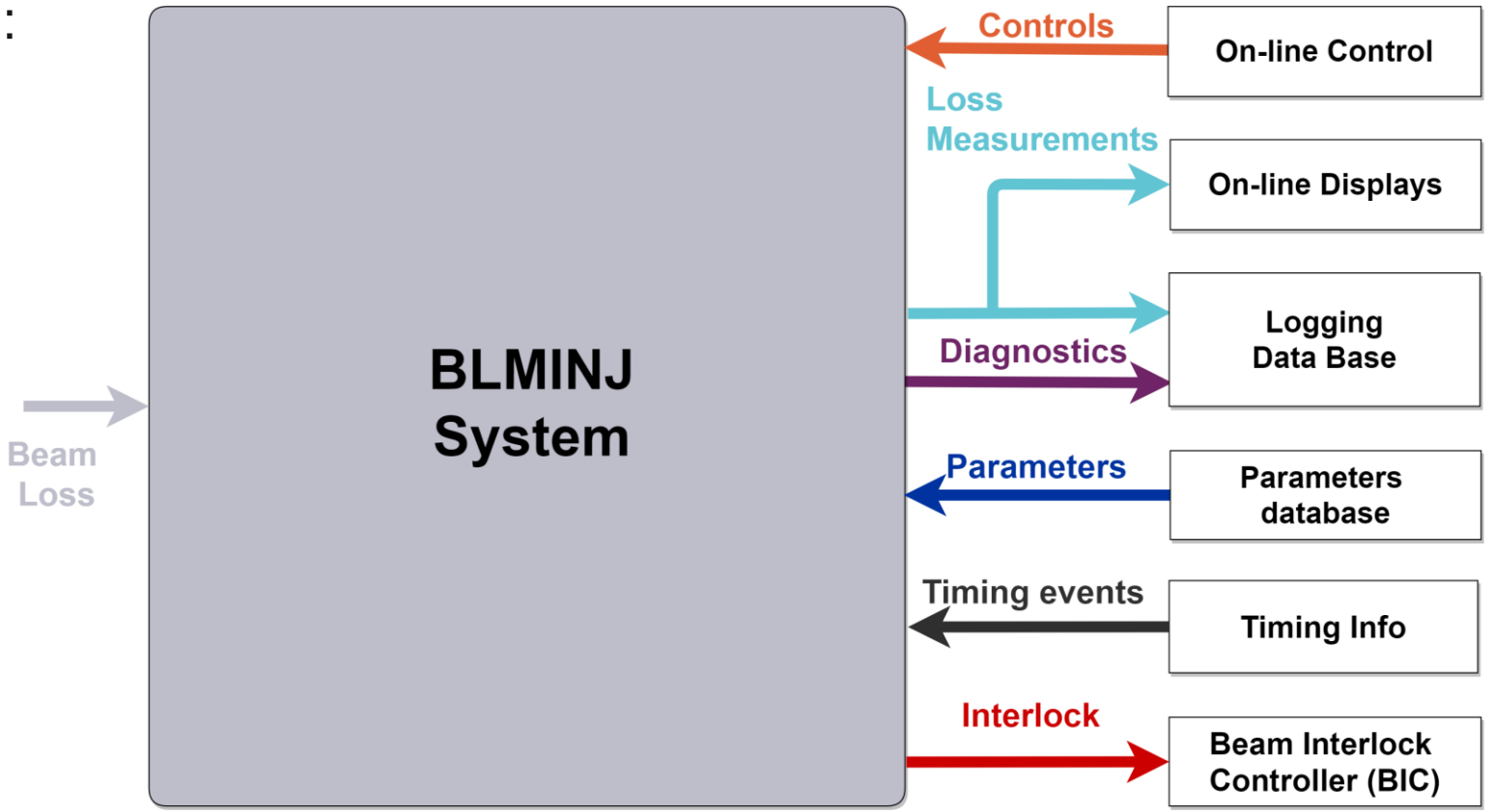


3. Firmware Validation

3 FPGA in the BLMINJ system

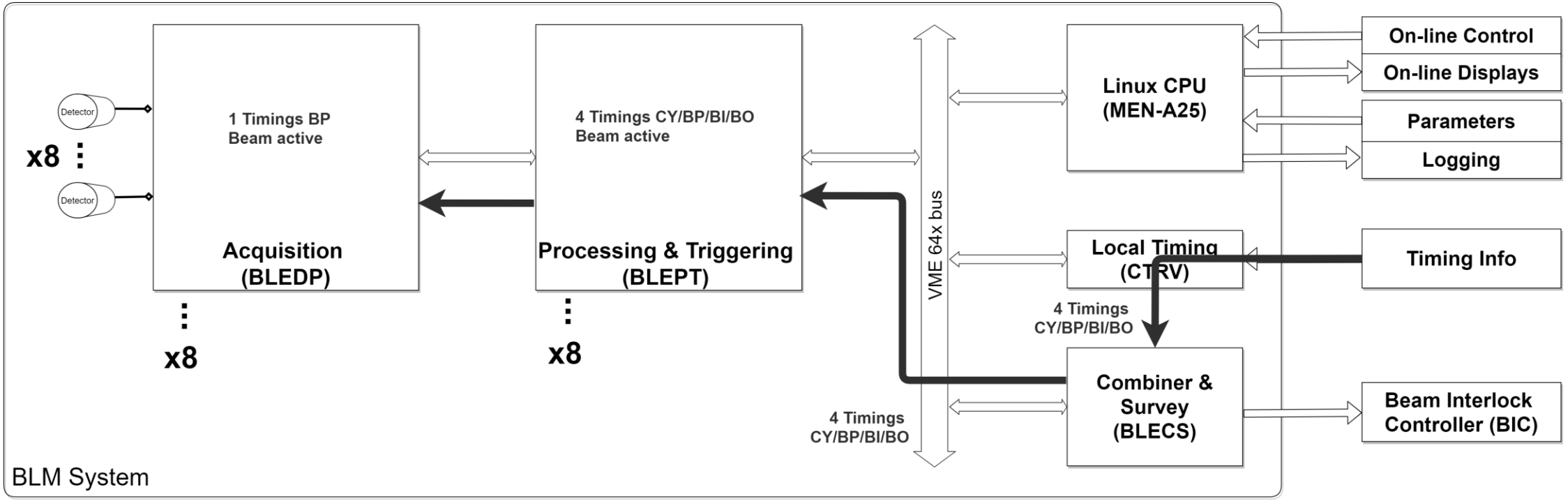
Timing events | Loss | Diagnostics | Interlocks | Control & Parameters

- The **same FW version** is deployed for all the injectors.
- The BLMINJ **HW is common** and the **configuration** depends on the machine.
- Data Streams:



BLMINJ Timings events

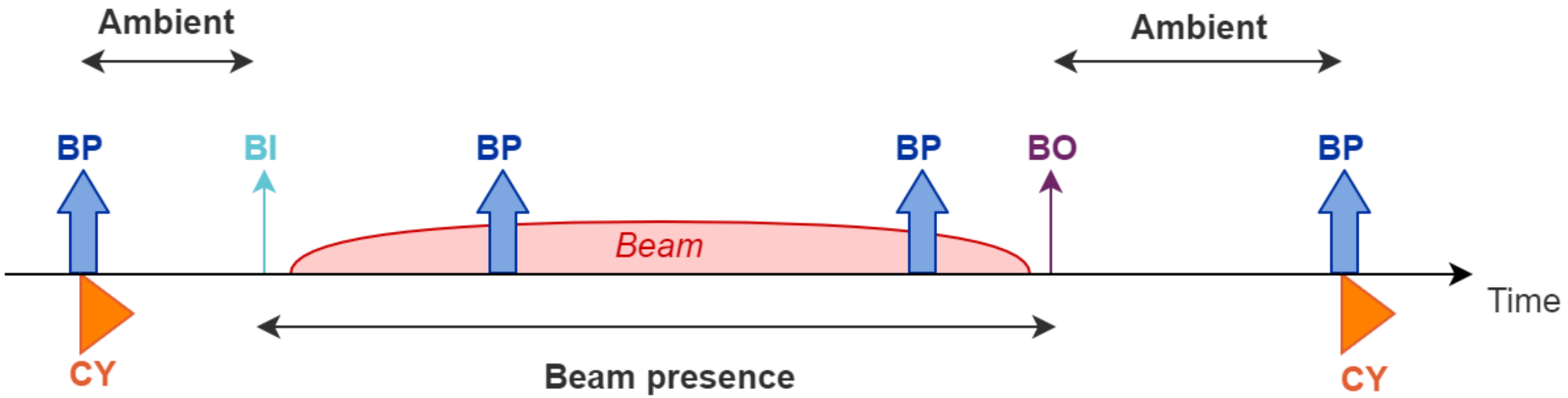
- The timing telegram is received by the local the CTRV
- 4 LTIM signals are generated and distributed to the FPGAs



BLMINJ uses 4 timings events

- Start of Basic Period BP : 1.2 s
- Start of Cycle CY : 1 to 5 BP per Cycle
- Beam In BI
- Beam Out BO

} Beam Presence versus Ambient



Timing Configuration

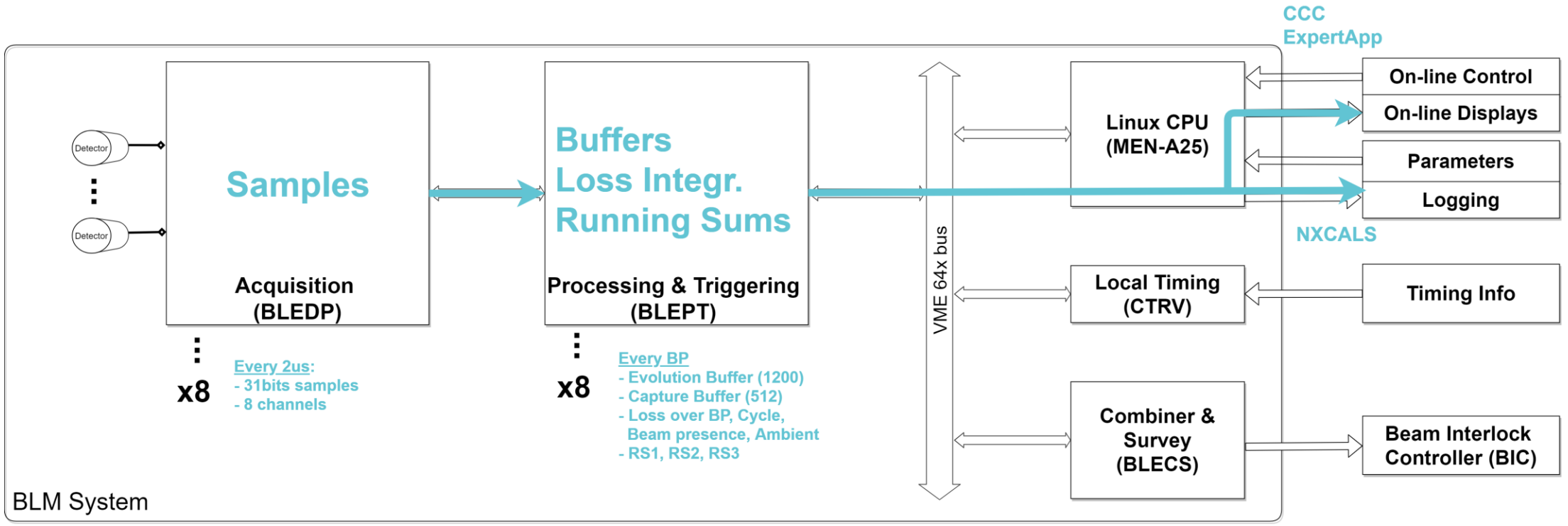
- 4 timings inputs but custom configuration **per machine**
- The CTRV manages the **local timing configuration**
- Two special hardwired timing signals for Linac4

Machine	Area	FEC	BP			BI			BO			CY		
			Name	Load Event	Delay	Name	Load Event	Delay	Name	Load Event	Delay	Name	Load Event	Delay
LN4	L4, LT	cfv-400-blmln4a	BX.SBP-BLMLN4A	BX.SBP-CT	0 ms	LEMO input L4X.SR4CHOPPER			LEMO input L4X.TAILCLIPPER			BX.SCY-BLMLN4A	BX.SCY-CT	0 ms
	LBE	cfv-400-blmln4b	BX.SBP-BLMLN4B	BX.SBP-CT	0 ms	LEMO input L4X.SR4CHOPPER			LEMO input L4X.TAILCLIPPER			BX.SCY-BLMLN4B	BX.SCY-CT	0 ms
PSB	BI	cfv-361-blmbi	BX.SBP-BLMBI	BX.SBP-CT	0 ms	BX.SBIN-BLMBI	BIX.W10-CT	8 ms	BX.EBOUT-BLMBI	BEX.AMC-CT	100 ms	BX.SCY-BLMBI	BX.SCY-CT	0 ms
	Ring	cfv-361-blmbra	BX.SBP-BLMBRA	BX.SBP-CT	0 ms	BX.SBIN-BLMBRA	BIX.W10-CT	8 ms	BX.EBOUT-BLMBRA	BEX.AMC-CT	100 ms	BX.SCY-BLMBRA	BX.SCY-CT	0 ms
		cfv-361-blmbrb	BX.SBP-BLMBRB	BX.SBP-CT	0 ms	BX.SBIN-BLMBRB	BIX.W10-CT	8 ms	BX.EBOUT-BLMBRB	BEX.AMC-CT	100 ms	BX.SCY-BLMBRB	BX.SCY-CT	0 ms
	Bt, BTM, BTY, BTP	cfv-361-blmbt	BX.SBP-BLMBT	BX.SBP-CT	0 ms	BX.SBIN-BLMBT	BEX.AMC-CT	0 ms	BX.EBOUT-BLMBT	BEX.AMC-CT	2 ms	BX.SCY-BLMBT	BX.SCY-CT	0 ms
PS	Ring	cfv-359-blmpra	PX.SBP-BLMPRA	PX.SBP-CT	0 ms	PX.SBIN-BLMPRA	PX.SCY-CT	9 ms	PX.EBOUT-BLMPRA	PX.ELFT-CT	2 ms	PX.SCY-BLMPRA	PX.SCY-CT	0 ms
		cfv-359-blmprb	PX.SBP-BLMPRB	PX.SBP-CT	0 ms	PX.SBIN-BLMPRB	PX.SCY-CT	9 ms	PX.EBOUT-BLMPRB	PX.ELFT-CT	2 ms	PX.SCY-BLMPRB	PX.SCY-CT	0 ms
	TT2: FTN,FTA, F16	cfv-269-blmtt2	PX.SBP-BLMTT2	PX.SBP-CT	0 ms	PX.SBIN-BLMTT2	PX.SCY-CT	9 ms	PX.EBOUT-BLMTT2	PEX.AMC-CT	2 ms	PX.SCY-BLMTT2	PX.SCY-CT	0 ms
	EA: F61, F62, F63	cfv-157-blmea	PX.SBP-BLMEA	PX.SBP-CT	0 ms	PX.SBIN-BLMEA	PX.SCY-CT	9 ms	PX.EBOUT-BLMEA	PX.ELFT-CT	2 ms	PX.SCY-BLMEA	PX.SCY-CT	0 ms
SPS	TT10	cfv-ba1-blmtt10b	SX.SBP-BLMTT10B	SIX.W20-CT	22 ms	SX.SBIN-BLMTT10B	SIX.W20-CT	19 ms	SX.EBOUT-BLMTT10B	SIX.W20-CT	21 ms	SX.SCY-BLMTT10B	SIX.F1KLO-CT	1002 ms
		cfv-269-blmtt10a	SX.SBP-BLMTT10A	SIX.W20-CT	22 ms	SX.SBIN-BLMTT10A	SIX.W20-CT	19 ms	SX.EBOUT-BLMTT10A	SIX.W20-CT	21 ms	SX.SCY-BLMTT10A	SIX.F1KLO-CT	1002 ms

BLMINJ_Wiki_Timings_configuration

Loss Measurements

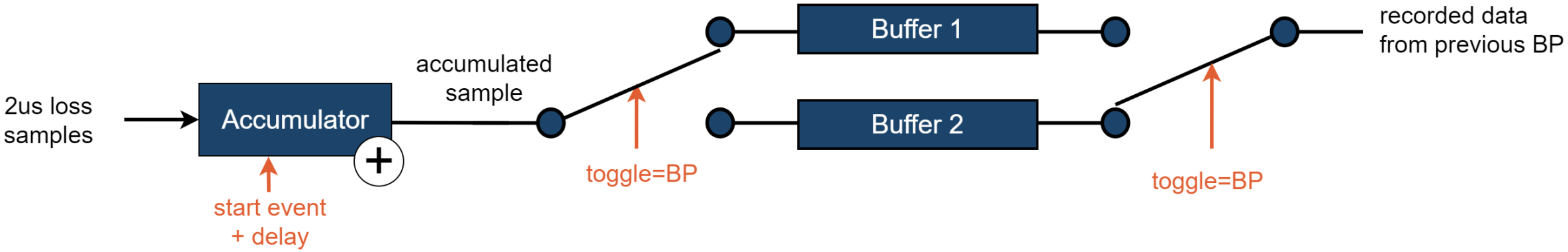
- Acquisition: 31bits loss samples transferred at 2us rate
- Processing: Buffers, Integrations and Running-sums are published at BP=1.2s rate
- No synchronization: free running acquisition and potential jitter in measures



Evolution and Capture Buffers

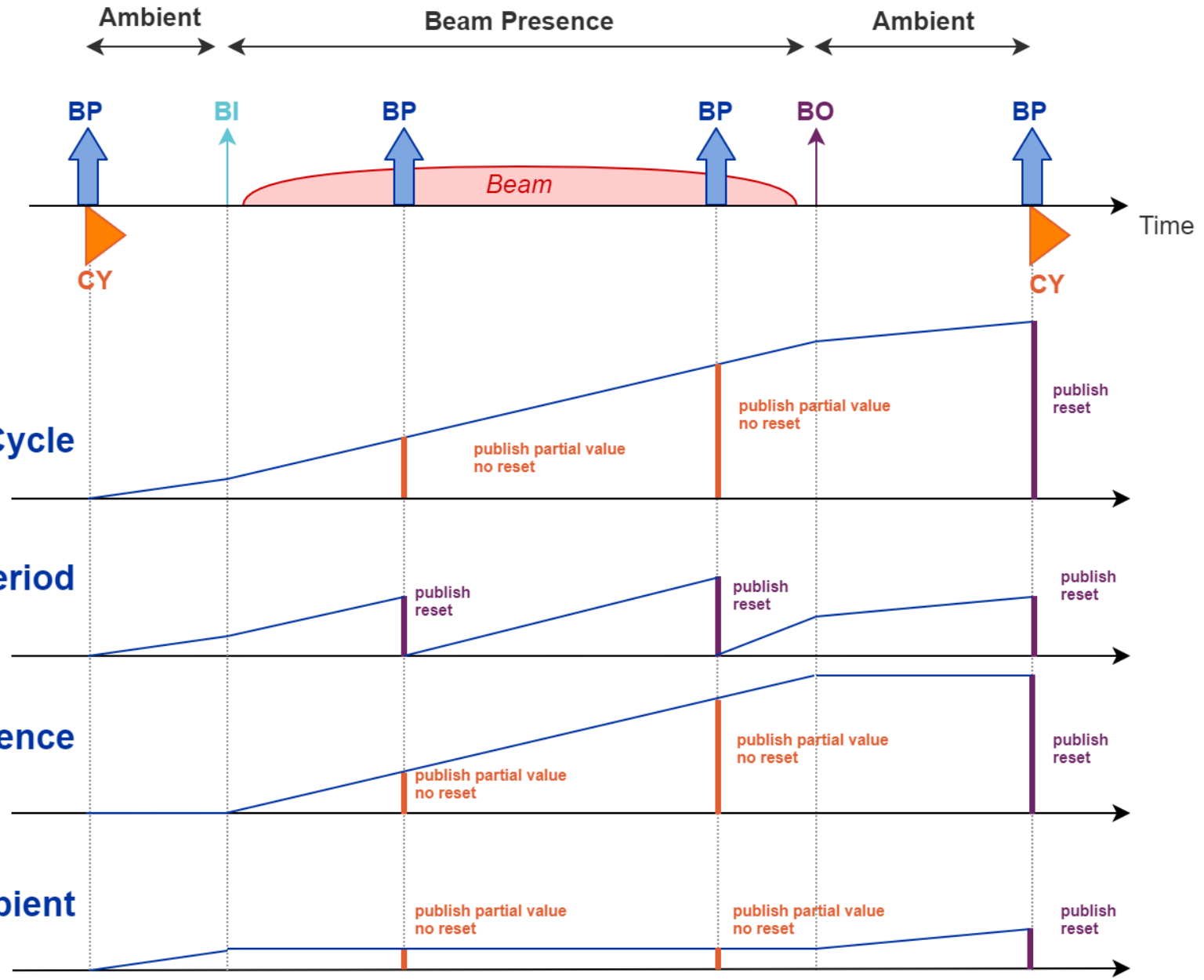
- **Double-buffer mechanism**
- **Adjustable pre-accumulator**
  - Start event
  - Delay
  - Accumulation sample rate

Parameter	Evolution		Capture
	Ring	Transfer	
Start Event	BP	BI	custom
Delay	0ns	0ns	custom
Accu.Sample Rate	1ms	2us	custom
Buffer Depth	1200 max	1200 max	512 max
TOTAL	1.2s	2.4ms	1.2ms to 1.2s



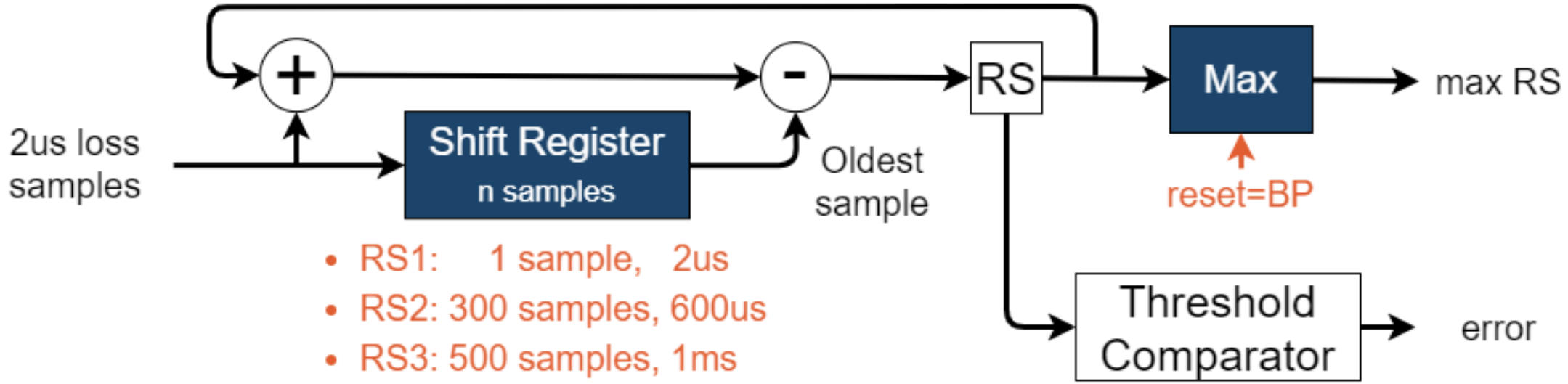
Loss Integrations

- Integrals of the 2us samples
- Start/Stop events
- Provided a single value
  - Cycle based reset
  - BP based publication
- Threshold comparator
- Define 4 types of measures



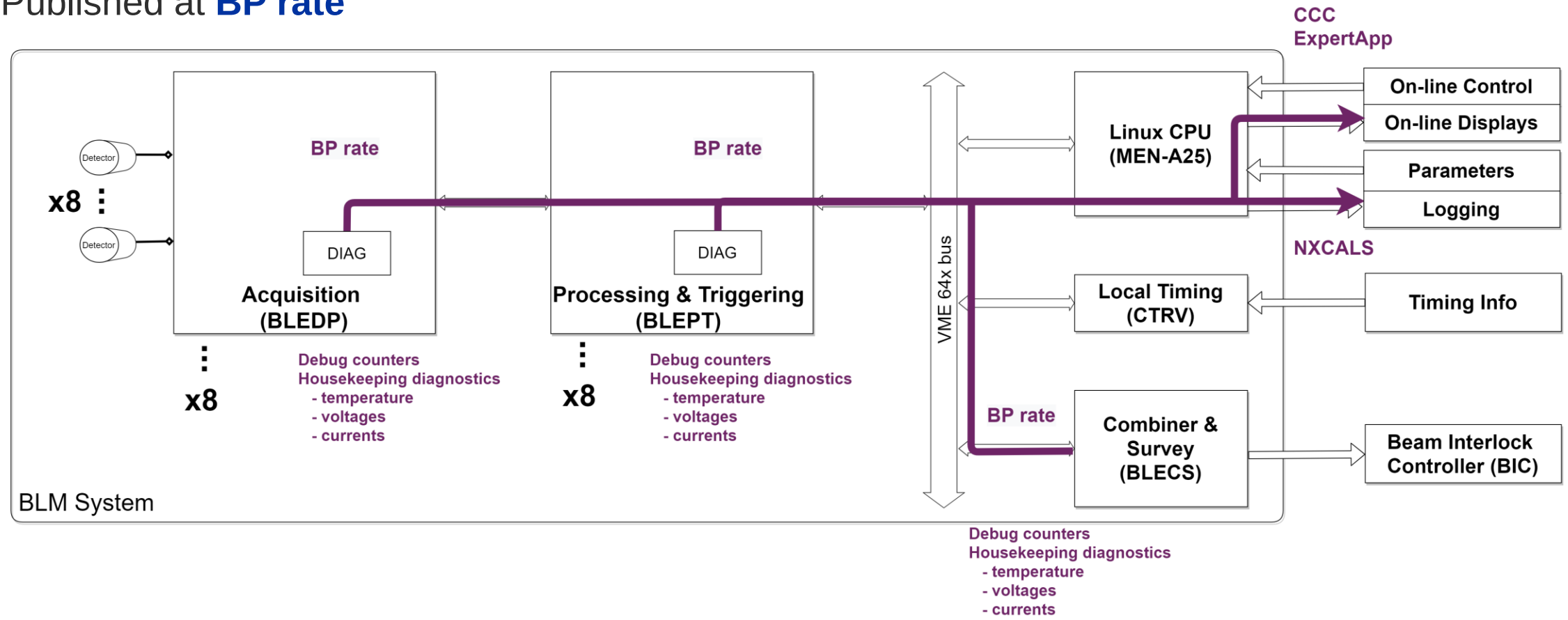
Maximum of Running Sums

- Implemented with a variable length **shift registers**
- **3 time-windows** implemented
- Store the **maximum value** over the Basic Period
- Publish a single value at **BP rate**
- **Threshold comparison**



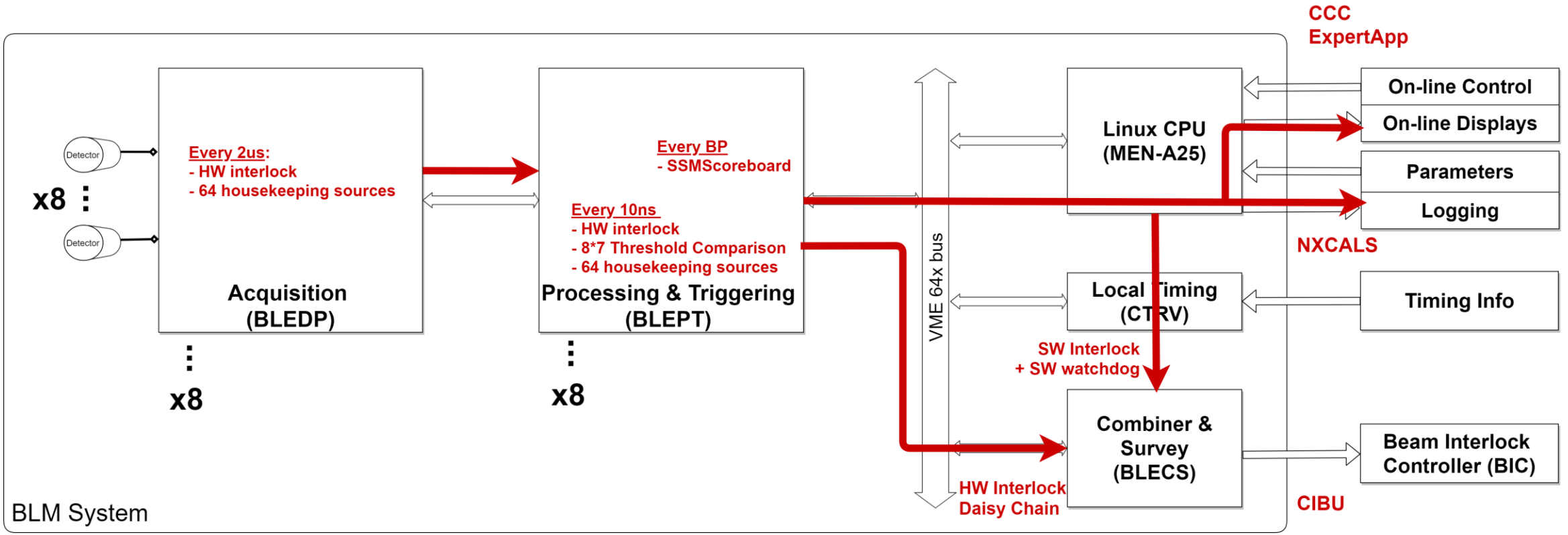
Diagnostics

- Diagnostics: electronics **housekeeping** values, **debug** counters, **error** states, etc…
- The **3 FPGAs** generate diagnostics
- Published at **BP rate**



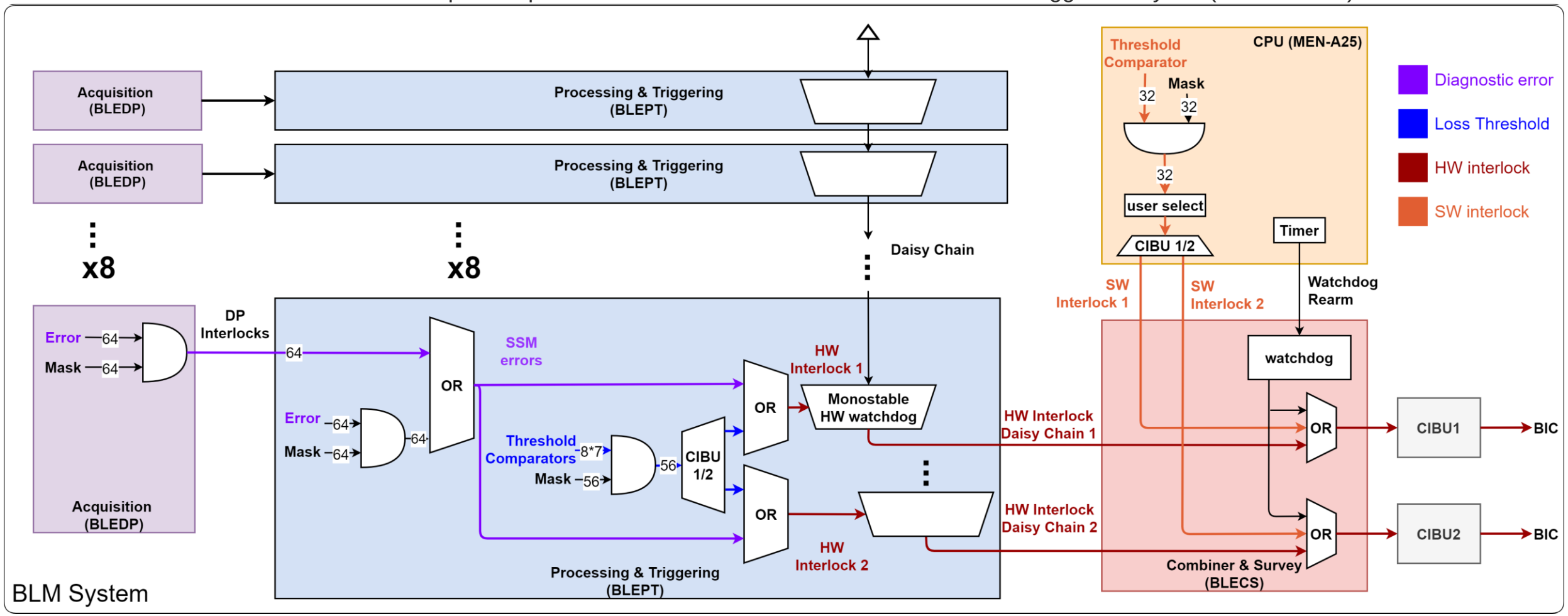
Interlocks

- Diagnostics and Losses are compared to **thresholds** to produce errors
- Acquisition, Processing and SW produce **maskable errors** (System Self Monitor)
- Generation of **HW & SW interlocks**



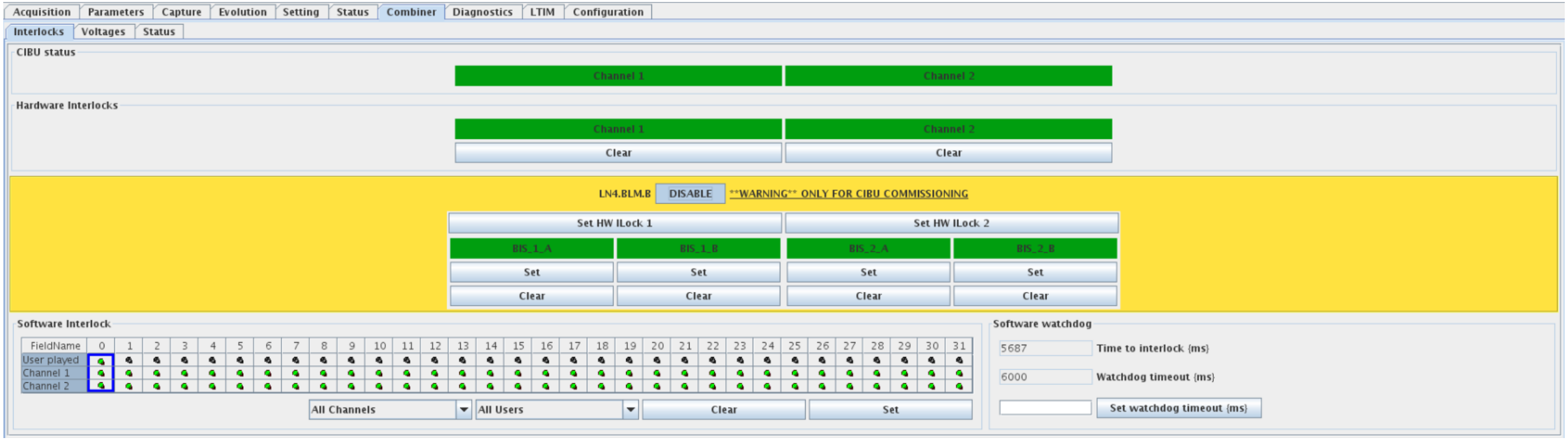
Interlocks

- **2 HW interlocks**: with 184 sources, 2 * 64 diagnostics error and 8 channels * 7 loss type threshold comparators
- **2*32 SW interlocks**: threshold comparator per user
- **Watchdogs**: daisy chained HW monostable + SW CPU timer
- **2 BIS connections:** up to 2 CIBU
- All errors are logged every BP (**Scoreboard**)



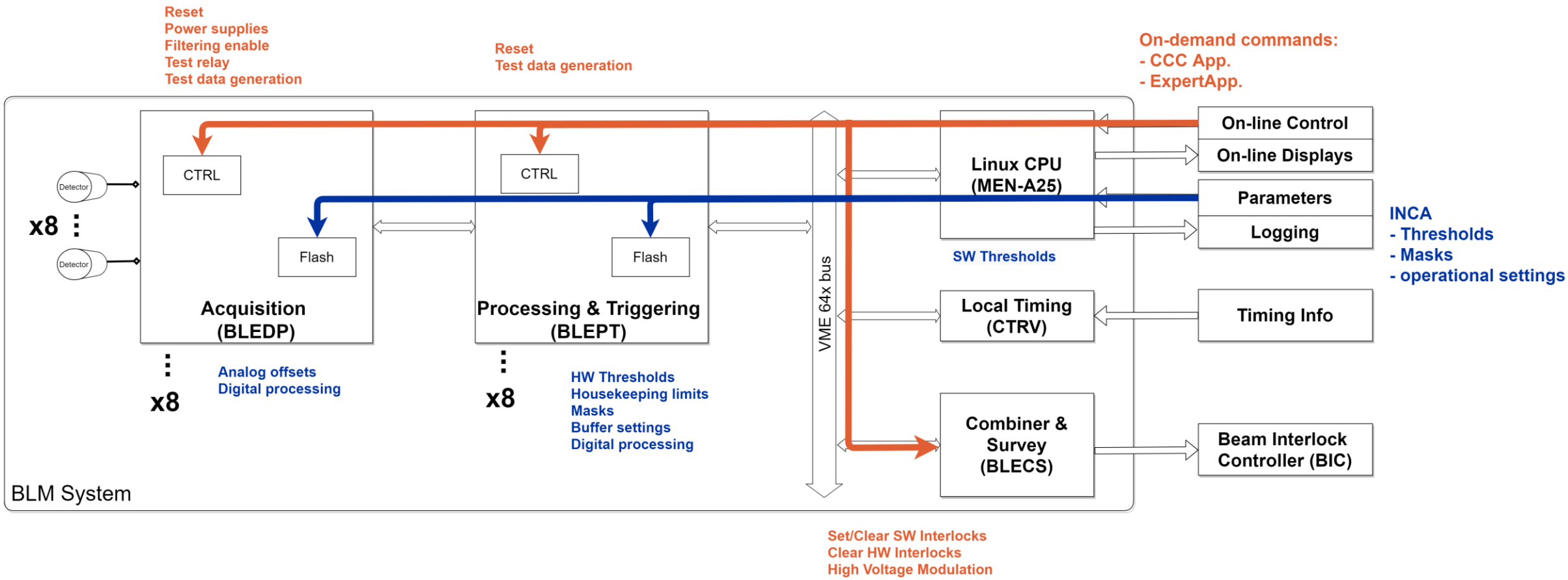
Connection to the Beam Interlock Controller

- The Combiner and Survey (**BLECS**) firmware connects to the CIBU
- Special tab in the **BLM Expert Application**
- Used for **CIBU commissioning**
- Overview of SW and HW interlock state and sources



Control & Parameters

- **Control :** from the expert application or the control room
- **Parameters :** updated at startup or on demand and **saved locally in flash memory**



Outline

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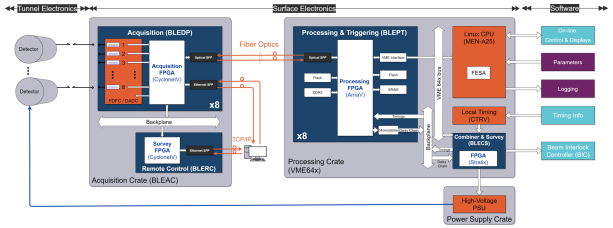

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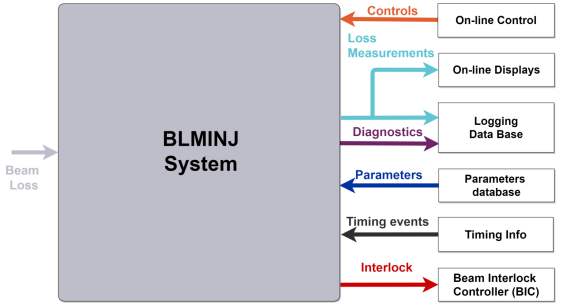
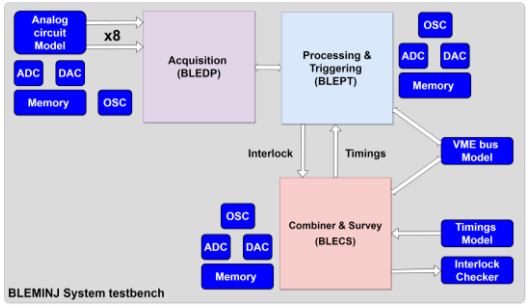
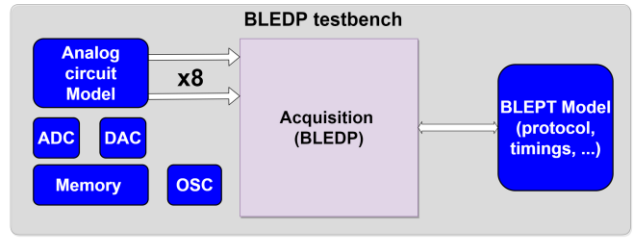


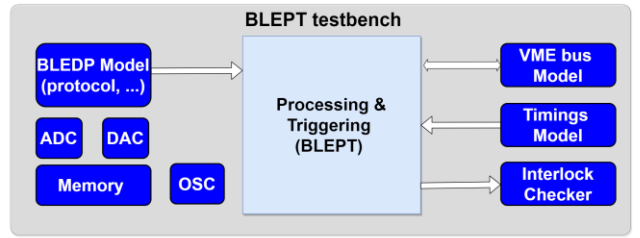
3. **Firmware Validation**

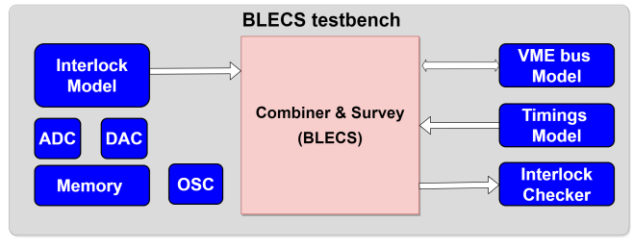


Firmware Simulation

- **Test Benches :**
  - **3 board models**: BLEDP, BLEPT and BLECS
  - **Full System** = 3 boards interconnected

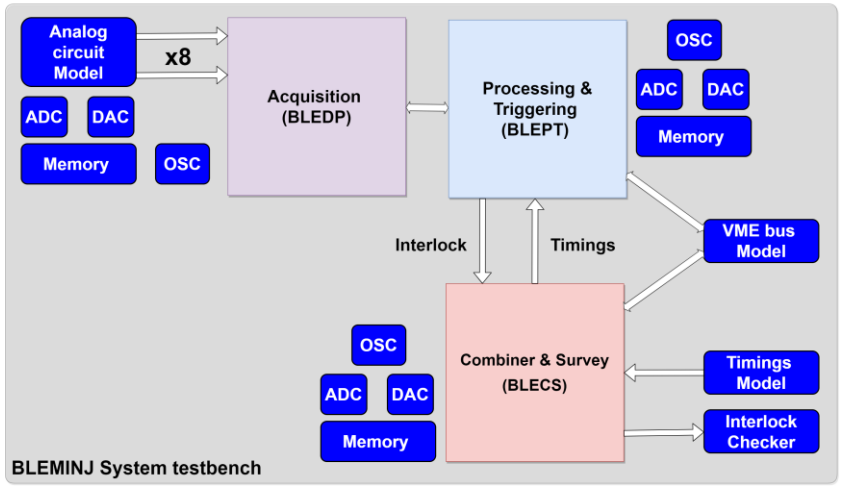






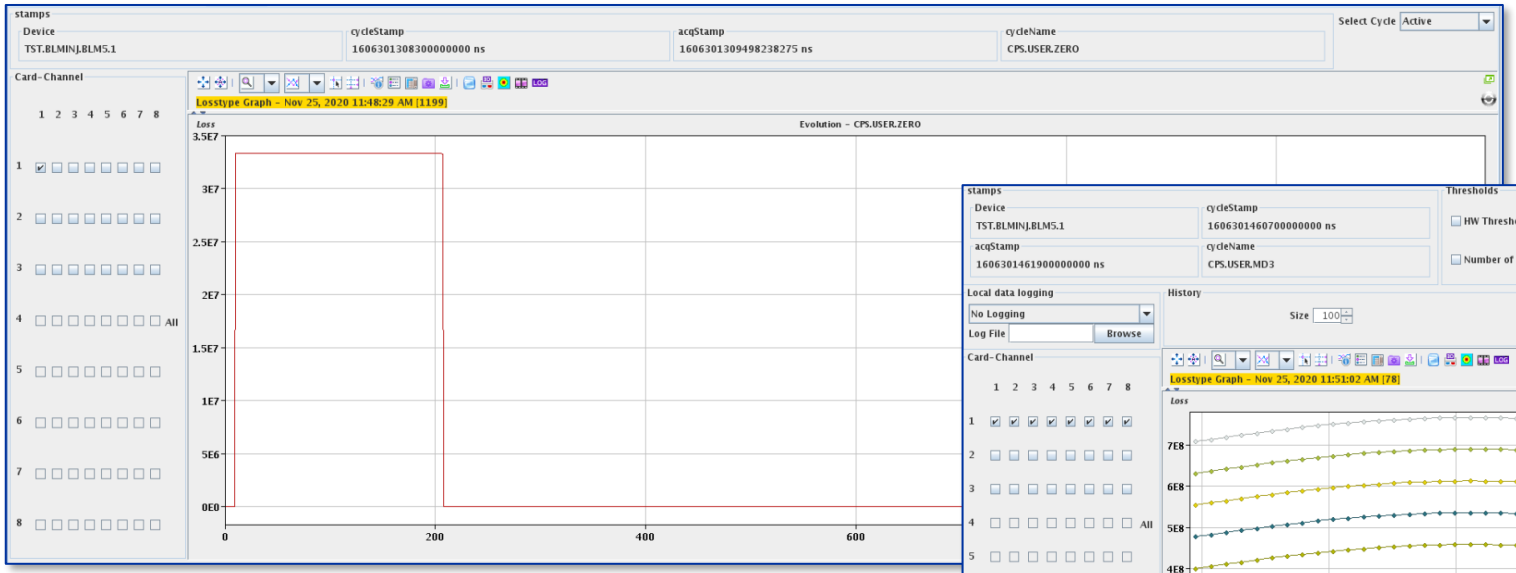
- **On-going simulations of the BLMINJ firmware:**
  - Validation objective : 100% functional coverage
  - Verification objective: 100% code coverage

- **For long-term maintenance:**
  - A technical student is working on both BLMINJ & BLMLHC
  - **Unitary verification** of all sub-modules, libraries and top-levels
  - Test of maximum of **corner cases**

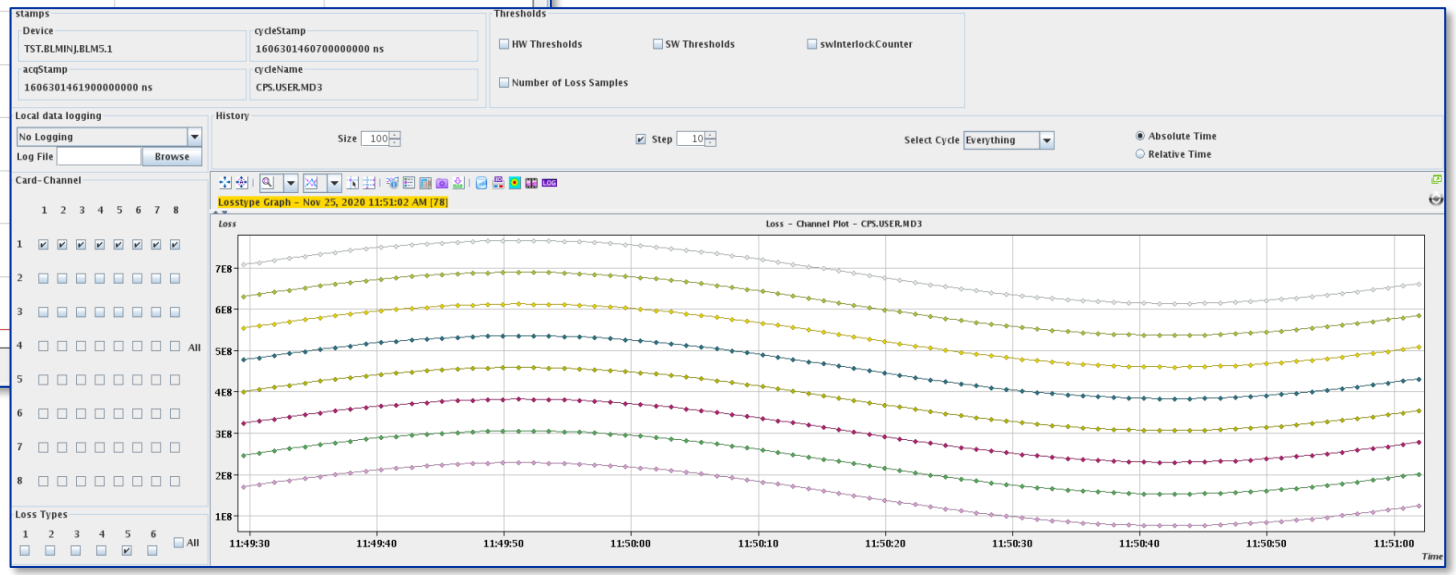


Firmware Validation on Target

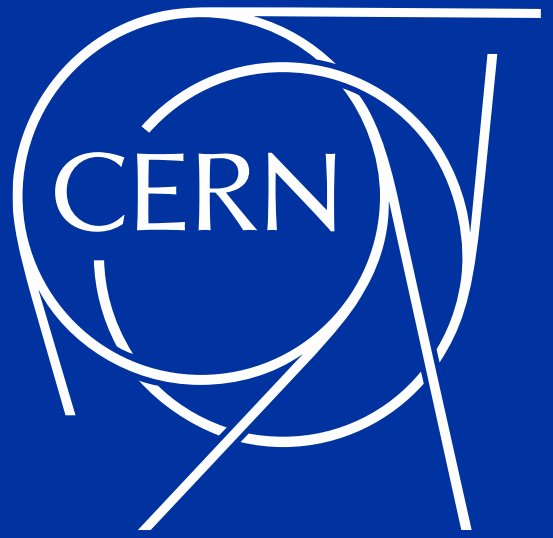
- PSB, SPS and LHC timing info available in the laboratory
- A setup with high-voltage bias and a real BLM **Ionization Chamber**
- A setup with a programmable **current source** and adjustable trigger ➔ fake beam pulse
- Use of FW **internal sine wave generator** with offset



200ms pulse generation from current source 10ms after CY



Internal sine wave generation


CERN