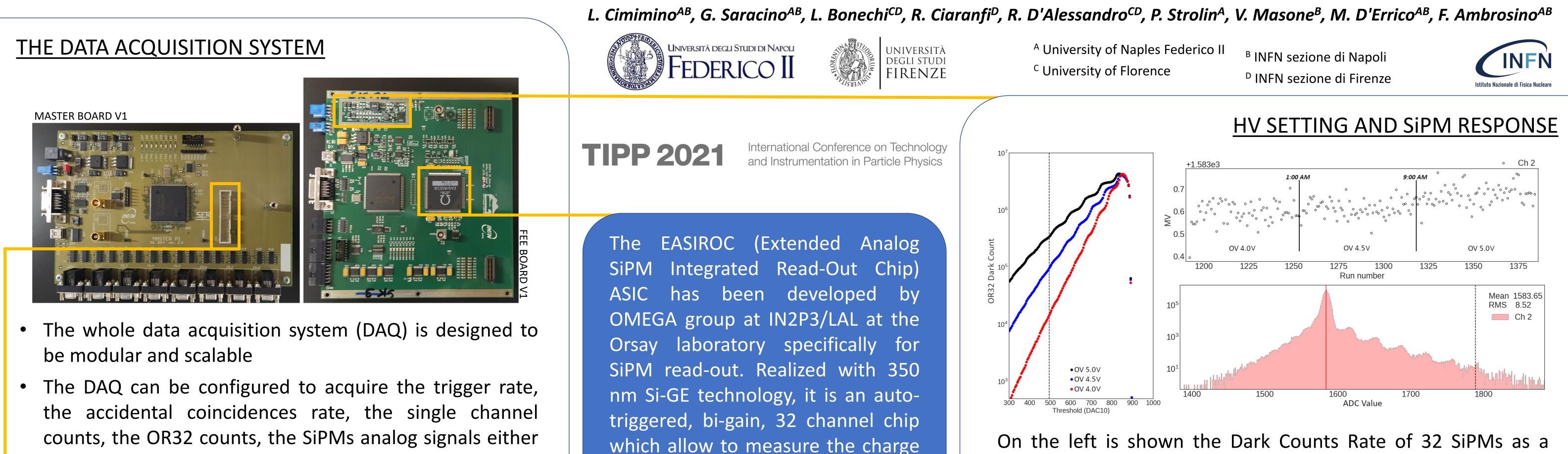
Stand-alone Low Power Consumption FEE and DAQ for Particle Tracking in Outdoor Applications



On the left is shown the Dark Counts Rate of 32 SiPMs as a function of threshold - lower DAC10 values correspond to higher threshold levels - for different overvoltages. The vertical dash line is drawn in correspondence of the 7th ph.e. at 4V overvoltage and it corresponds to the dash line in the photoelectron spectrum of the SiPM (bottom right plot) at the same overvoltage. It crosses the 5V overvoltage curve at 5th ph.e., denoting a change in the whole dynamics of the SiPMs not limited to the gain only. The increase in overvoltage produces a stretching of the spectrum towards higher ADC values, while the ADC value of the main peak remains quite constant as shown in the top right plot where the mean value of the SiPM spectrum is plotted in function of the run number in a 24 hours test.

Acquired data are digitized and then transmitted from the FEE board to the ARM single-board computer embedded in the MASTER board

in random acquisition or by satisfying a combinatorial

The DAQ software is developed in C and Python programming languages. Thanks to the connection through the GPIO interface, it is possible to program the EASIROC. An asynchronous communication protocol developed at low level, ensures that both the settings and the acquired data are transmitted between the computer and the FEE board through the MASTER board. Several GPIO lines are used to perform polling or interrupt operations, to generate clocks and to transmit data packets. An integrity check process and a Vertical Redundancy Check ensure the quality of the data collected before storing it.

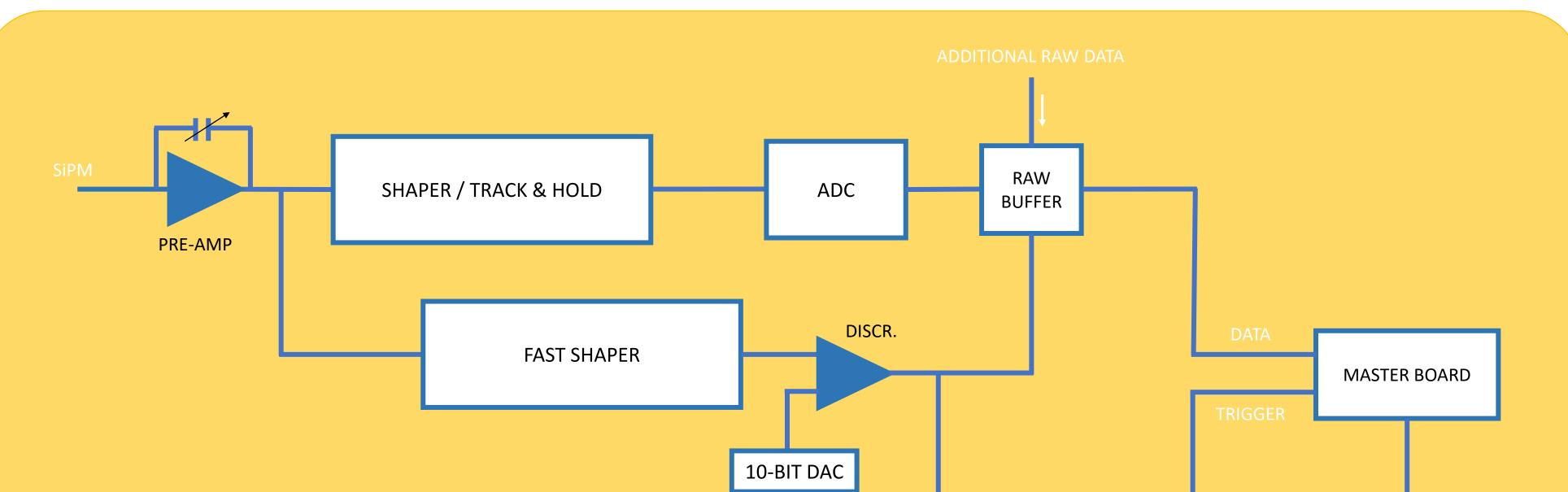
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fine gain adjustment. The power consumption is up to 155 mW per chip. The analog output from the EASIROC will be digitized by a dedicated electronics that also provide data transmission. A fast shaper followed by a discriminator provides a trigger path set by an integrated 10-bit DAC.

from one to 2500 photoelectrons.

It can provide to each SiPM a

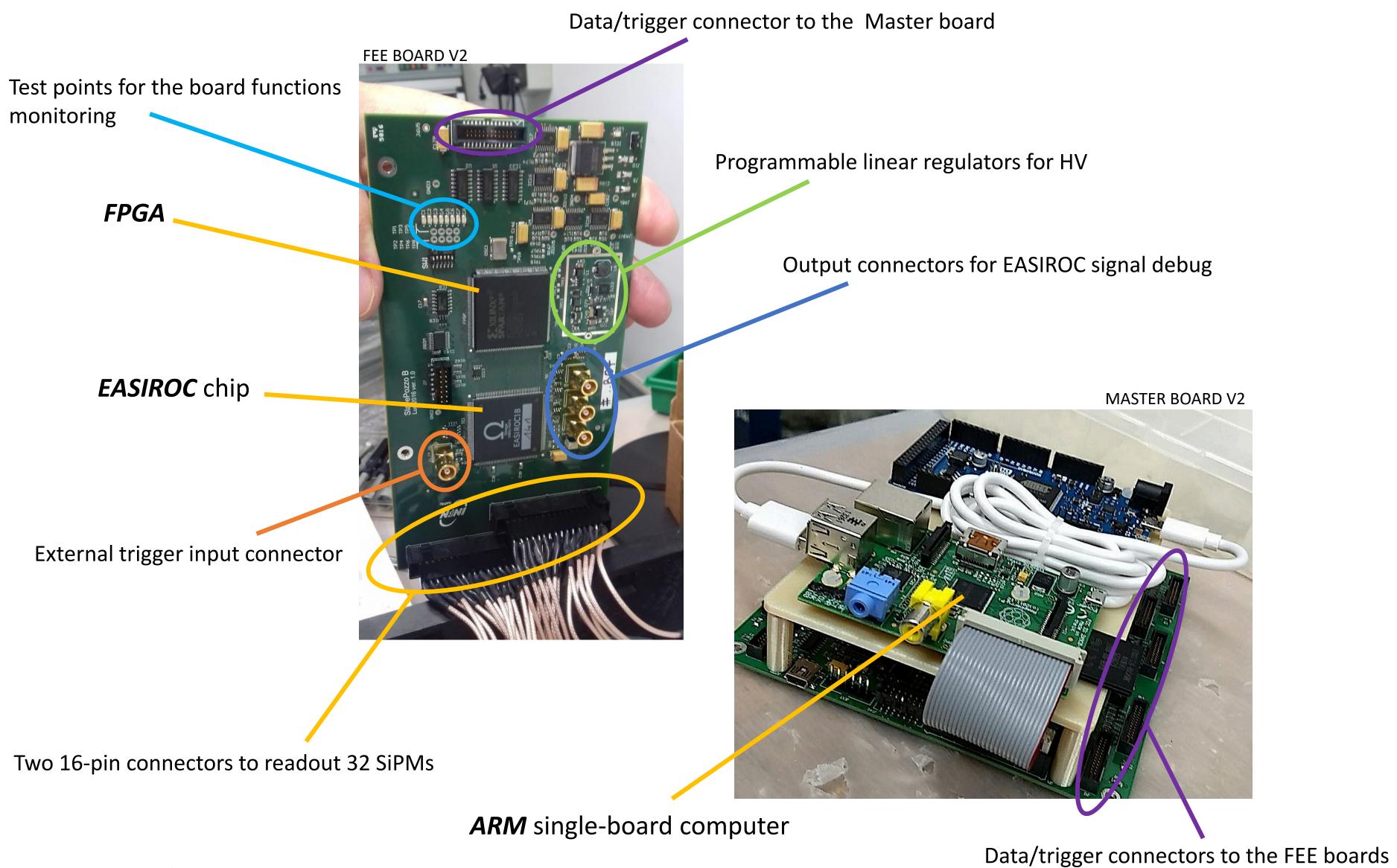
DAQ SCHEME





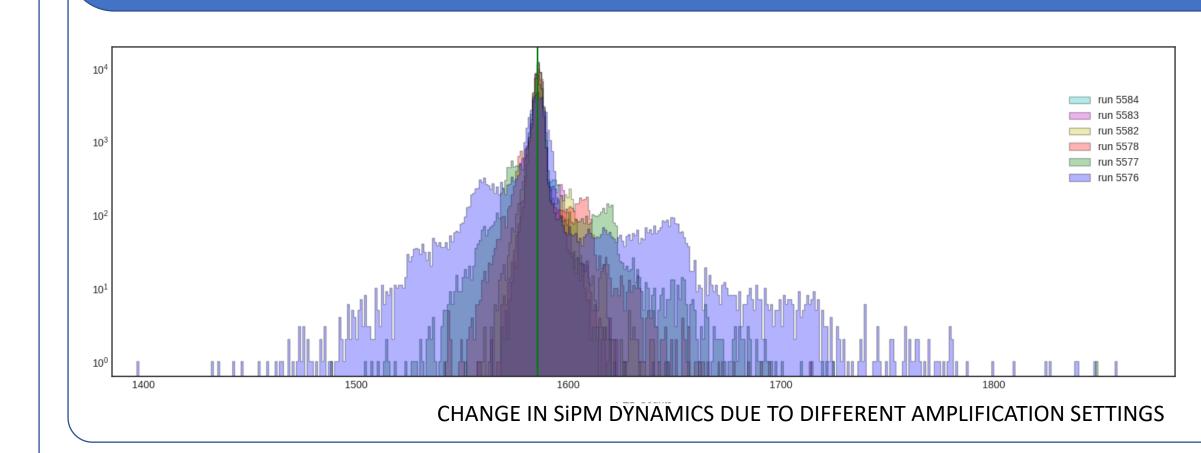
MAIN FEATURES

logic



The signals produced by SiPMs are amplified of a factor depending on a feedback capacitance setting. Two separated amplification path (High and Low Gain) are available. In each path a tunable shaper followed by a Track and Hold circuit determine the amount of charge measured. The measured values for each SiPM are converted by a 12-bit ADC.

OR32



RAW DATA FORMAT

COMPUTER

- < 2.5 W FEE board power consumption</p>
- RUN and DIAG operating mode
- Designed to embed a ARM single-board computer
- Events data are downloaded from each FEE board and stored in a NAS
- Programmable HV for SiPMs bias voltage
- Analog to Digital conversion operated by a FPGA
- Input and output connectors for characterization and debug
- Programmable trigger logic
- Delayed trigger for accidental rate measurement
- Time expansion circuit for TOF measurement • 780 bit data format
- Remotely controllable
- Autonomous Control System avoids damages, sets working point based on variations in environmental condition and controls data acquisition

[2axxx] [00xxx] [01xxx] ... [1fxxx] [Oxxxx] [Oxxxx] [000xx] [00xxx] [2axxx] [25555]

Event Number x32 digitized measured values Map of over-threshold channels Board temperature Texp value for TOF measurement VRC End of data

REFERENCES

L. Cimmino, et al., *The MURAVES telescope front-end electronics and* data acquisition, Annals of Geophysics 60 (1) (2017)

S. Callier, et al., *EASIROC, an Easy and Versatile ReadOut Device for SiPM*, Physics Procedia 37 (2012)