Contribution ID: **627** Type: **Parallel session talk**

# Buried Layer Low Gain Avalanche Diodes

*Wednesday, May 26, 2021 5:48 AM (18 minutes)*

We report on the design, simulation and test of Low Gain Avalanche Diodes (LGADs) which utilize a buried gain layer. The buried layer is formed by patterned implantation of a 50-micron thick float zone substrate wafer-bonded to a low resistivity carrier. This is then followed by epitaxial deposition of a ~3 micron-thick high resistivity amplification region. The topside is then processed with junction edge termination and guard ring structures and incorporates an AC-coupled cathode implant. This design allows for independent adjustment of gain layer depth and density, increasing design flexibility. A higher gain layer dopant density can also be achieved by controlling the process thermal budget, improving radiation hardness. A first set of demonstration devices has been fabricated, including a variety of test structures. We report on TCAD design and simulation, fabrication process flow, and preliminary measurements of prototype devices.

## TIPP2020 abstract resubmission?

No, this is an entirely new submission.

## Funding information

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**Session Classification:** Sensors: Solid-state sensors for tracking

**Track Classification:** Sensors: Sensors: Solid-state position sensors