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Radiation damage investigation of epitaxial p-type silicon using Schottky and pn-junction diodes

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Schottky Project description and goals

- **What:**
  - fabricate Schottky and n^+p diodes on p-type epitaxial (50µm thick) silicon wafers
  - doping concentrations as they are normally found in CMOS MAPS devices

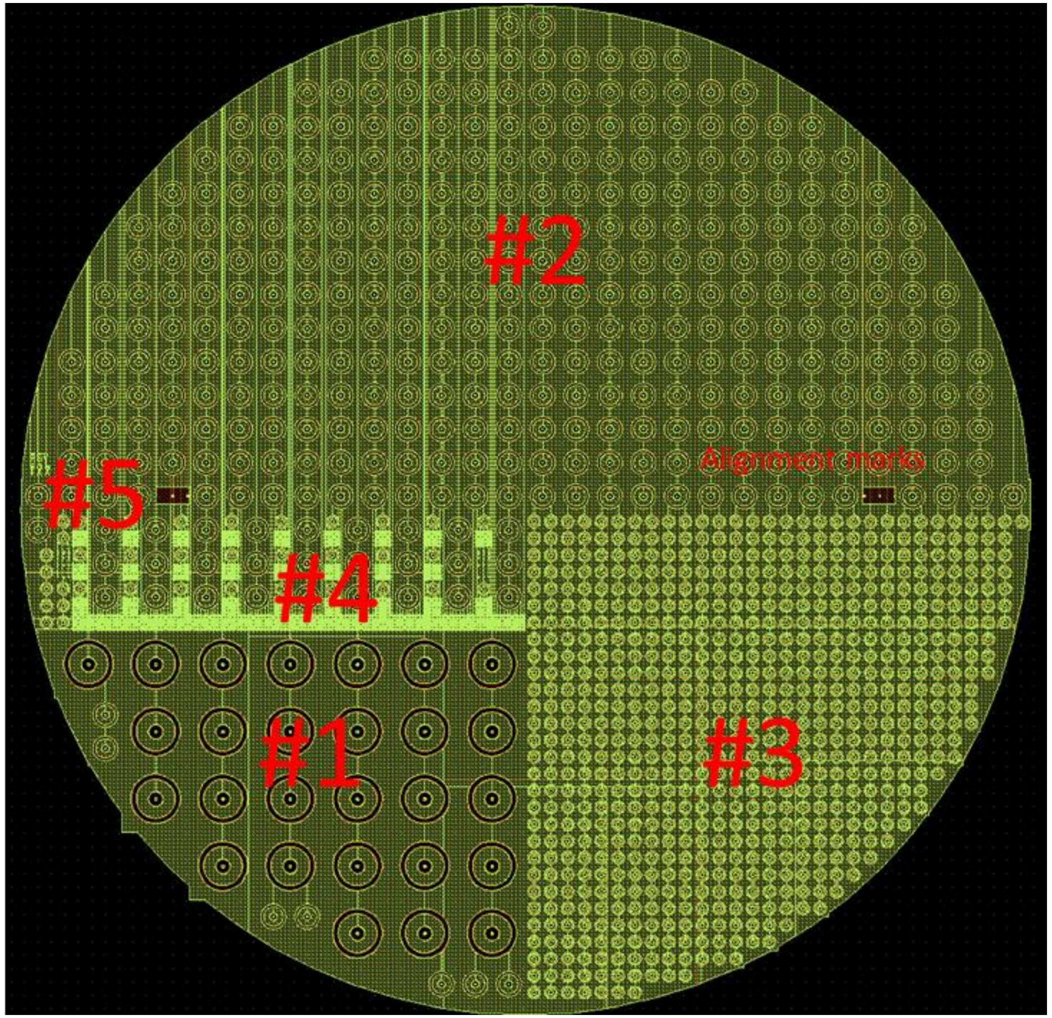
- **Why:**
  - investigate and gain a deeper understanding of radiation bulk damage in CMOS sensors.
  - develop reliable damage models that can be implemented in TCAD device simulators (Synopsys or Silvaco)

- **How:**
  - purchase of 6-inch wafers at five B-doped epitaxial levels (10^{13}, 10^{14}, 10^{15}, 10^{16} and 10^{17} cm^{-3}) 25x each, total **125 wafers**
  - fabrication process has started both at ITAC (RAL) and Carleton University Microfabrication Facility (CUMFF).
  - tests will be carried out at RAL, Birmingham, JSI, CUMFF, IHEP

Design and layout of devices

5 type of devices proposed:

- #1: 2 mm Ø cathode with 0.4 mm Ø central hole, 10 x 10 mm^2 area
- #2: 1 mm Ø cathode, 0.2 mm Ø central hole, 5 x 5 mm^2
- #3: 0.5 mm Ø cathode, no central hole, 2.5 x 2.5 mm^2
- #4: 0.1 mm Ø cathode, no central hole, 0.5 x 0.5 mm^2
- 'cell' with the previous 3 flavors (2,3,4) grouped together, to exploit wafer uniformity on small area
- #5: 6 TLM points for contact and epi resistance
- 2 masks only (metal and oxide)
- detailed description during the 35th RD50 workshop



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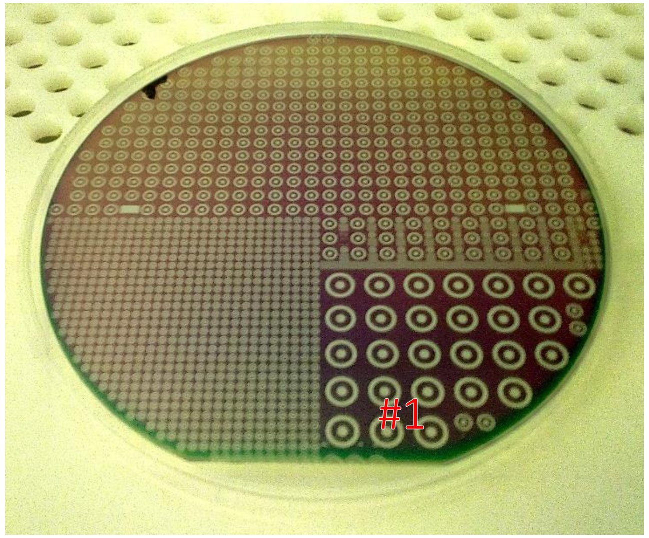
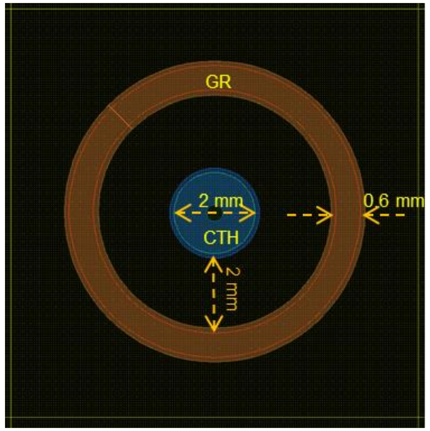
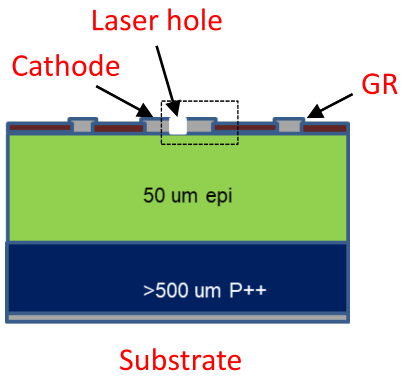






Fabrication details & comparison

RAL-ITAC

- Schottky process optimised on test wafers
- oxide deposition @150°C
- Al sputtering immediately after etching (no thin SiO2 layer)
- Al lift off in Acetone ultrasonic tank

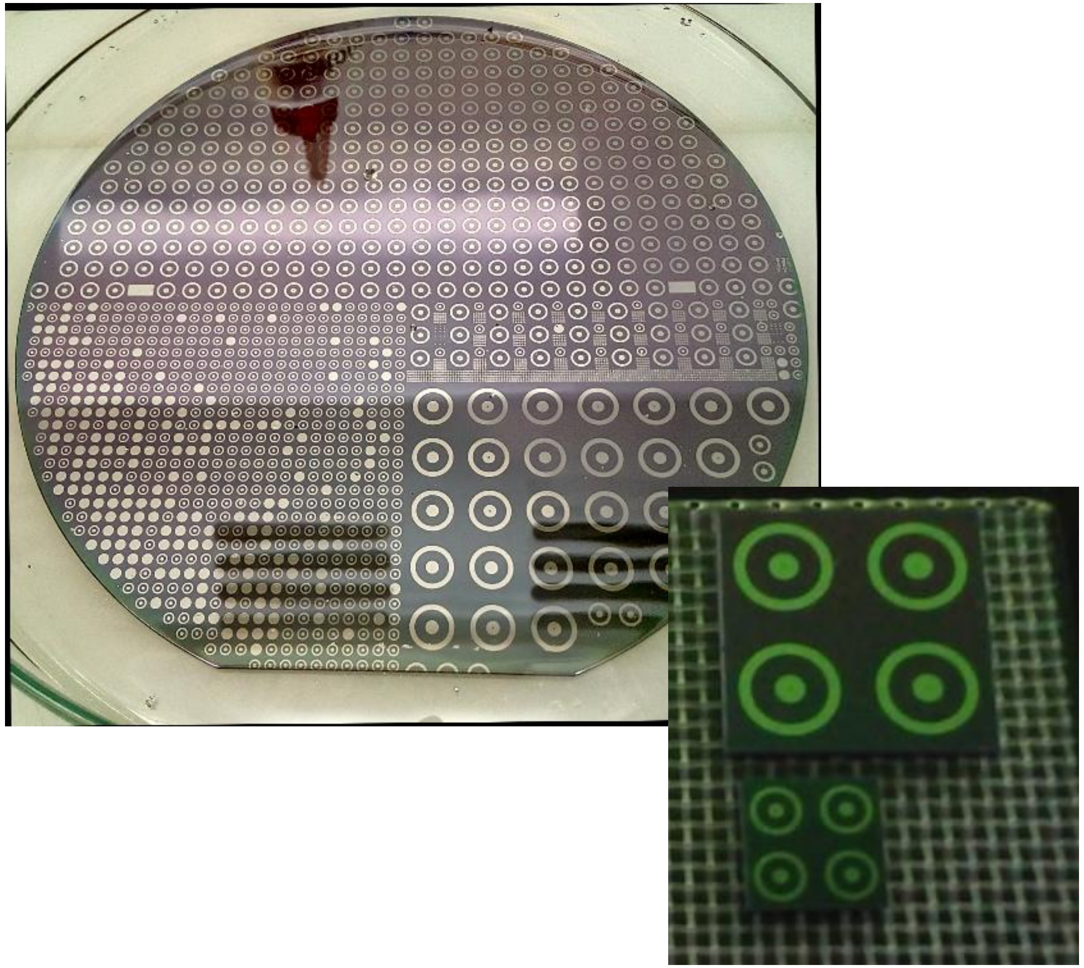
CUMFF

- pn-junction process optimised on test wafers
- 6” substrate wafers laser cut into 4”
- high temperature thermal oxidation
- Al front metal thermal deposition, back Al via e-beam evaporation
- front metal patterning + etching

full details of fabrication processes in **[E.G. Villani’s talk from the 36th RD50 Workshop]**

Project status

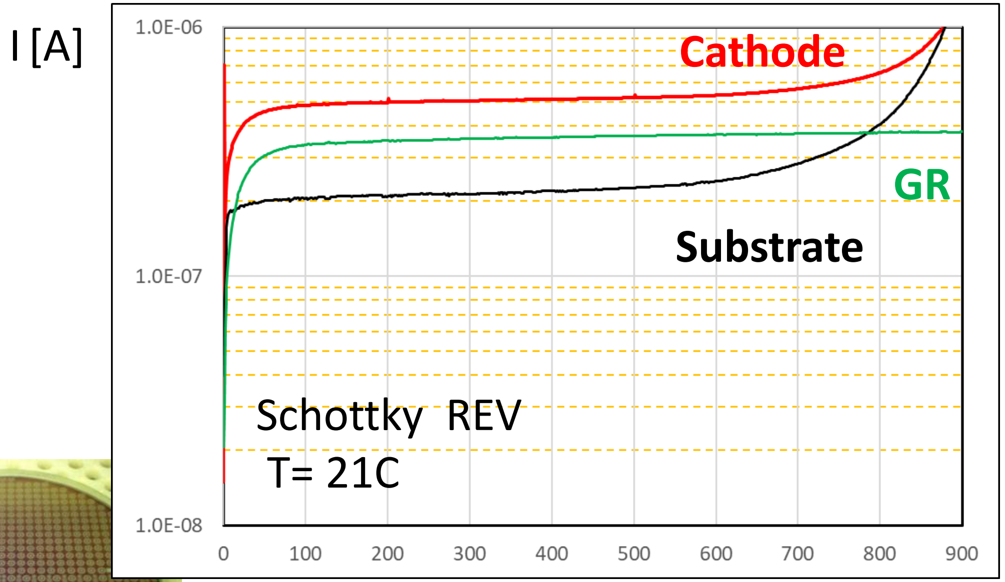
- 2x 4-inch wafers with pn-junctions fabricated at CUMFF
- 1 full Schottky wafer fabricated at RAL (+9 process started), multiple runs with wafer pieces at CUMFF
- IV & CV measurements on multiple diode flavours per wafer
- results cross-checked between institutes
- laser dicing at Scitech (RAL) for small samples used in DLTS and irradiation
- DLTS on Schottky and pn-junctions performed in Bucharest and at Semetrol (USA)

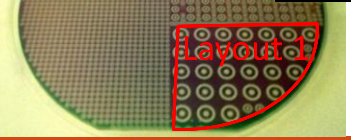


IV measurements

SCHOTTKY DIODES

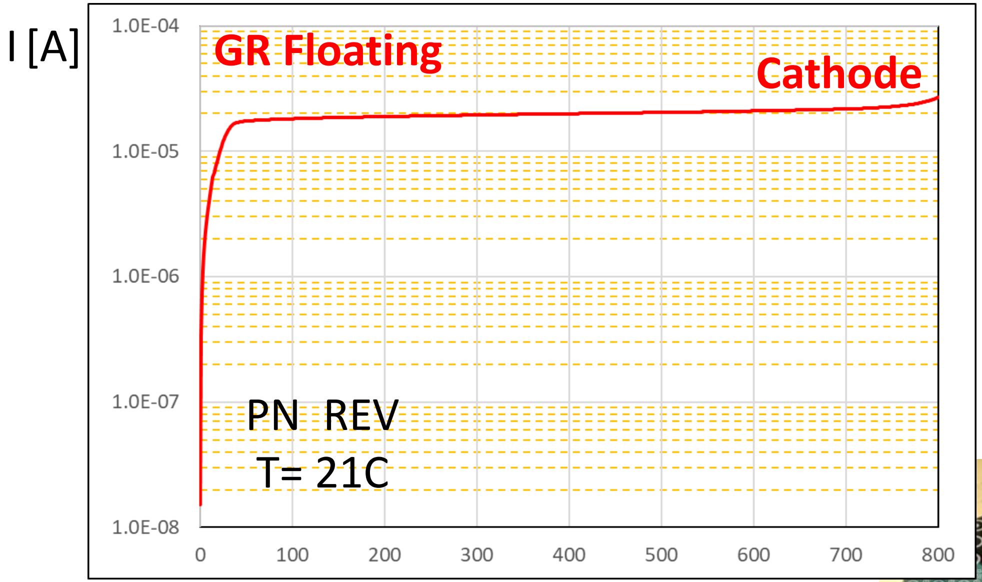
- backplane + GR at GND
- all layouts tested

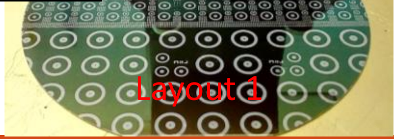




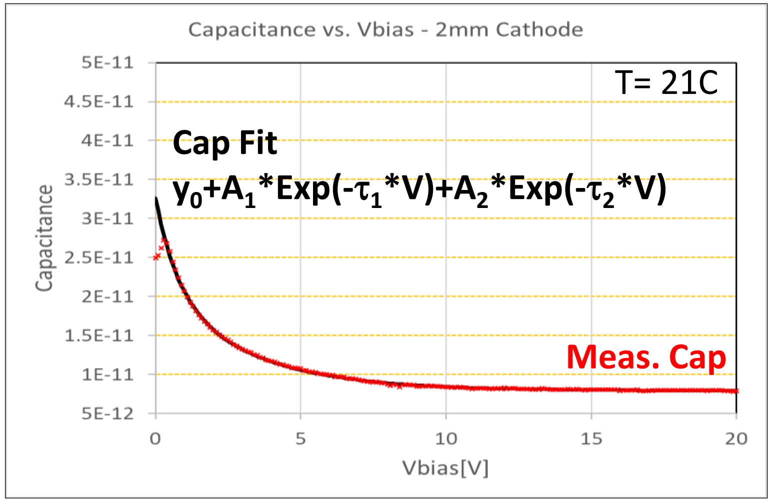
PN JUNCTIONS

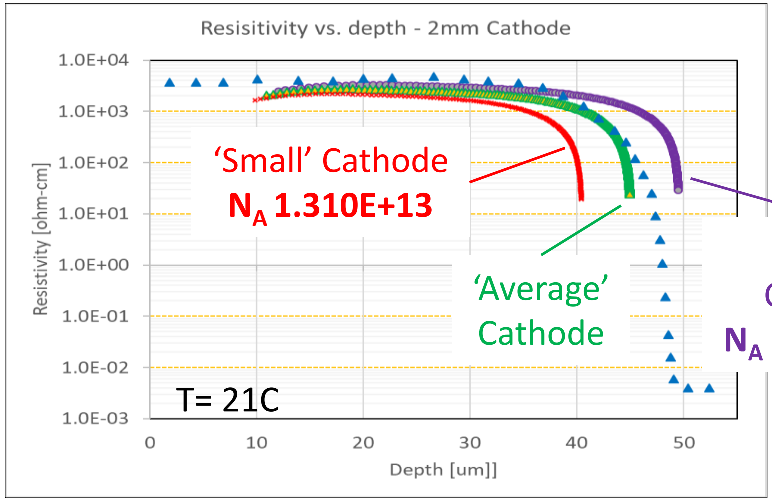
- leakage current much higher than for Schottky by two orders of magnitude





CV measurements

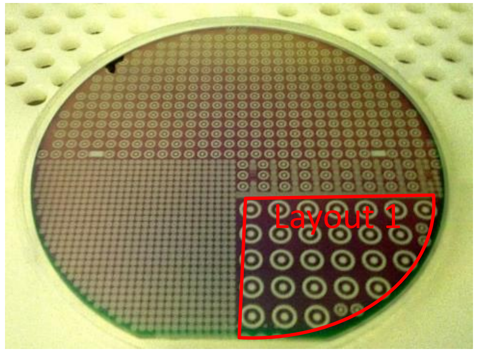


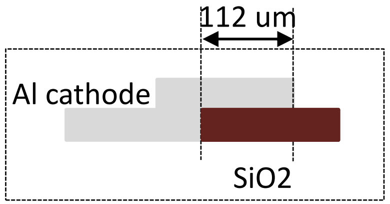


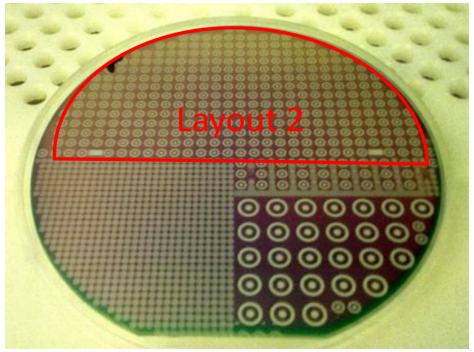
'Small' Cathode
N_A 1.310E+13

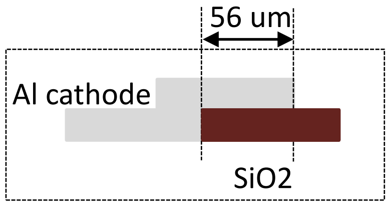
'Average' Cathode

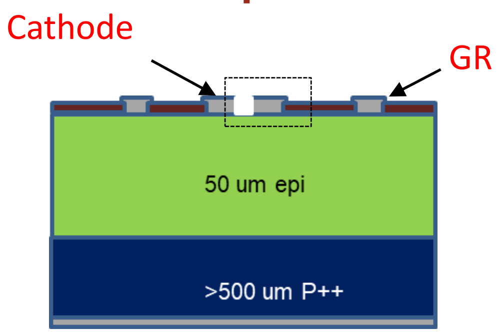
'Large' Cathode
N_A 8.731E+12



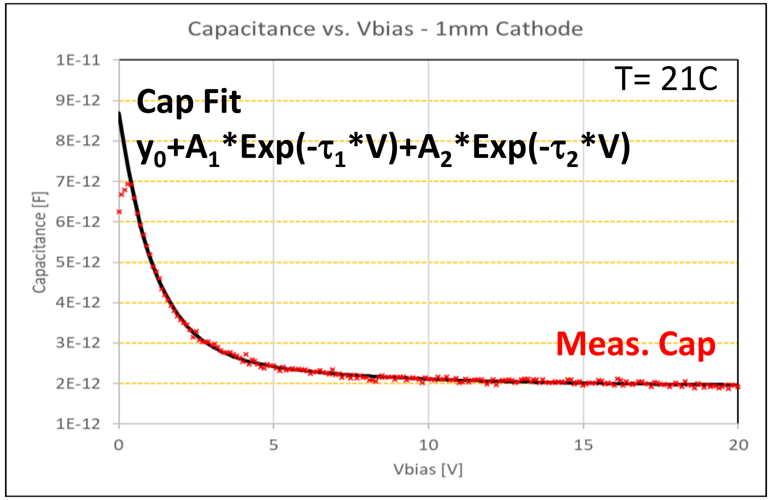


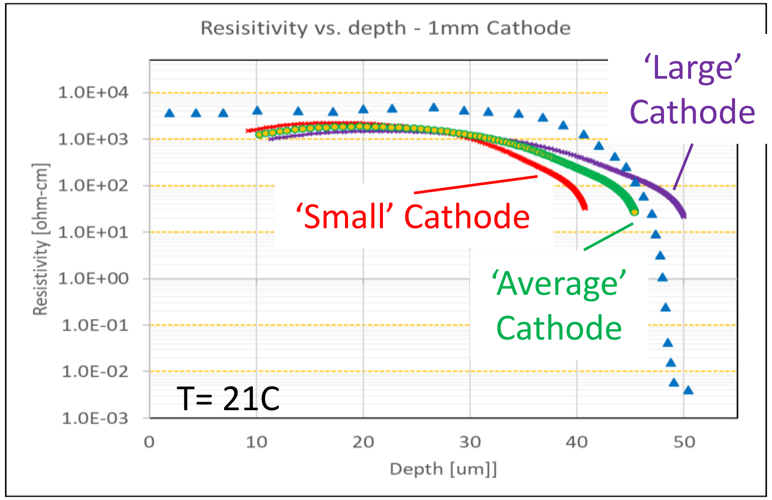






Substrate





Schottky barrier height

- Schottky barrier derived from CV measurement

$$\varphi_b = V_d + \frac{K \cdot T}{e} \cdot \left(ln\left(\frac{N_V}{N_A}\right) + 1 \right) - \Delta\varphi$$

↑ From 1/C^2

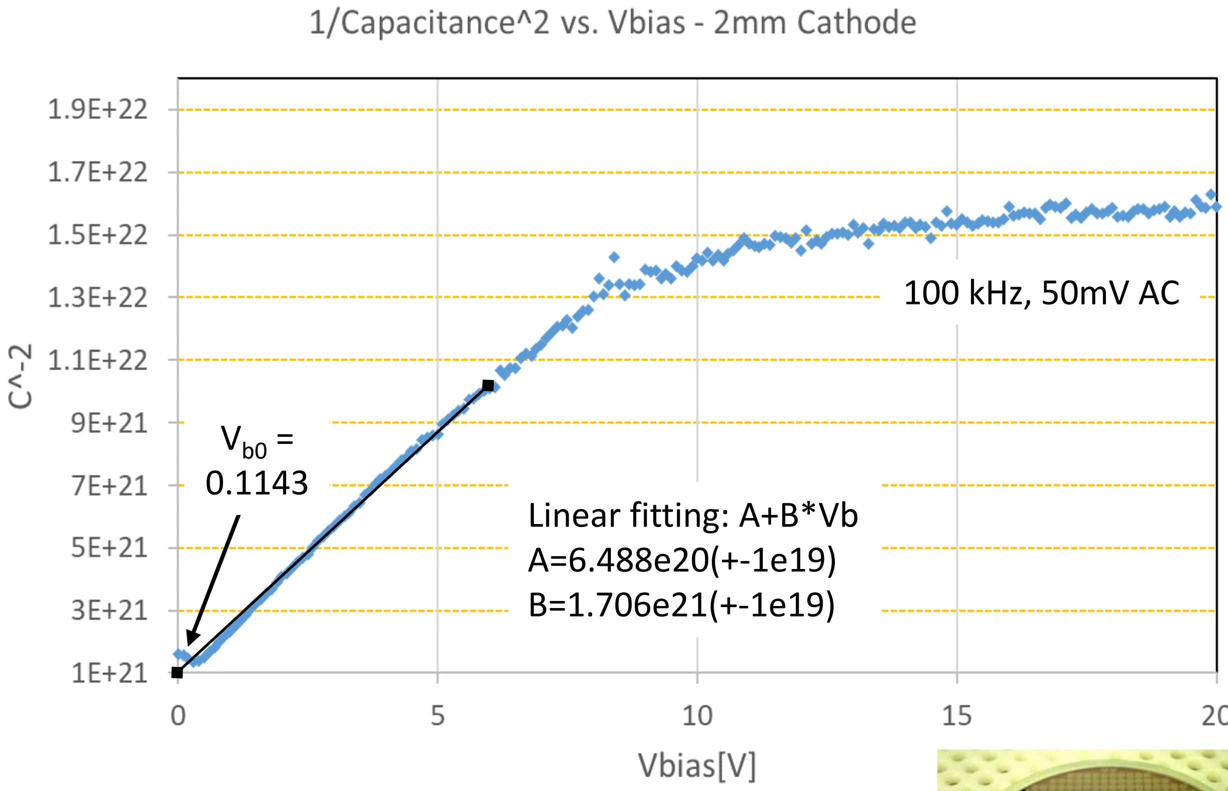
↑ From C-V

↑ Barrier lowering (neglected here)

- from 1/C^2 intercept: V_d=0.1143 V and using N_v =1.83e19

$$\varphi_{bpmin} = .4985\ eV$$
$$\varphi_{bpmax} = .5088\ eV$$

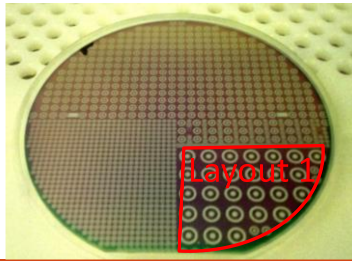
depending on the cathode size chosen and therefore the doping N_A


1/Capacitance^2 vs. Vbias - 2mm Cathode

V_{b0} = 0.1143

Linear fitting: A+B*Vb
A=6.488e20(+-1e19)
B=1.706e21(+-1e19)

100 kHz, 50mV AC



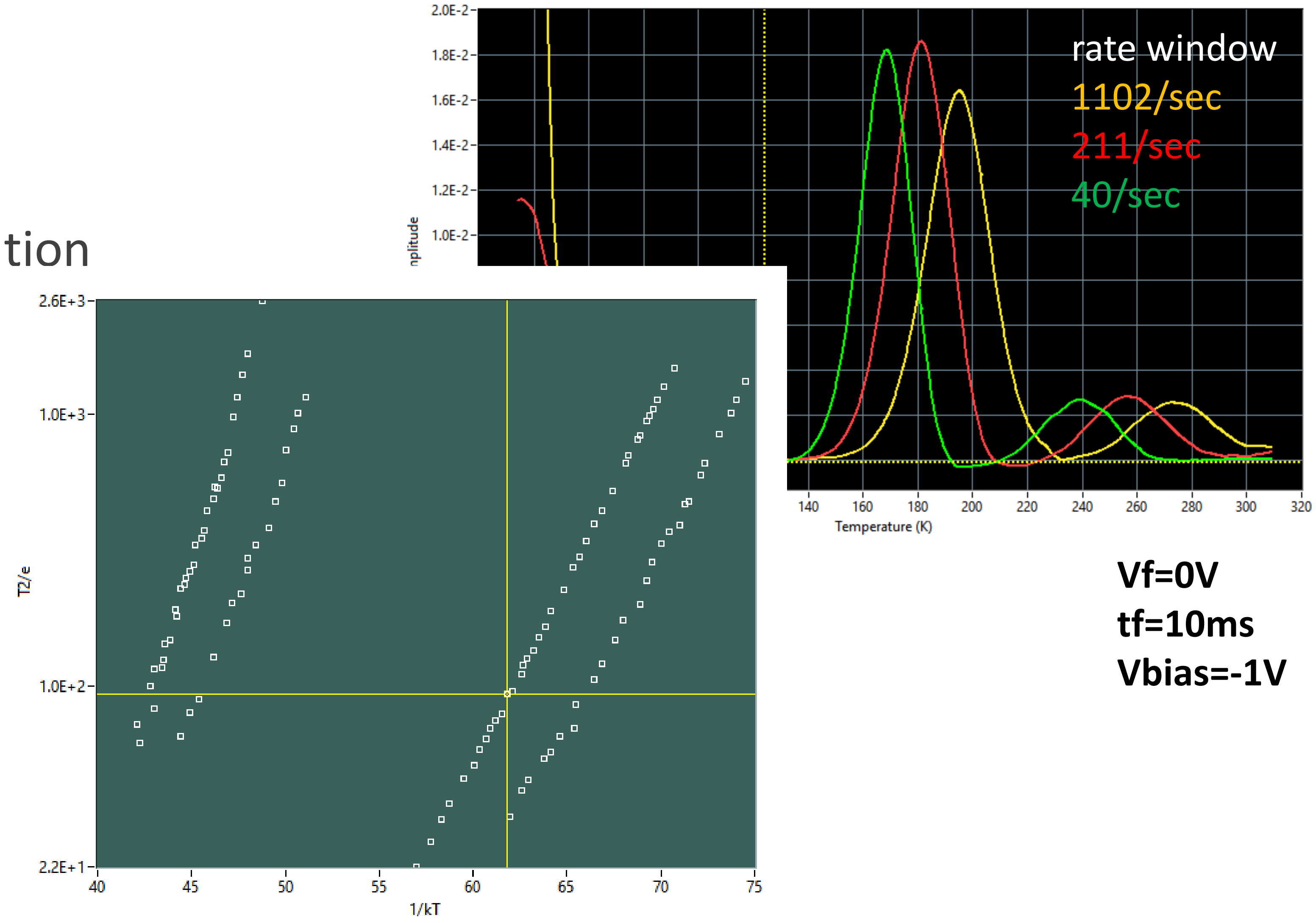
DLTS measurements: pn-junction diode @Semetrol

DLTS spectrum:

- 2 maxima
- analysis with Gaussian deconvolution
  ⇒ peaks contain 2 traps each

trap params from Arrhenius plot:

Midpoint temp (K)	E_t (eV)	Sigma (cm²)	N_t/N_s
170.6	0.293	7.6E-16	9.7E-3
182.8	0.310	7.0E-16	2.1E-2
241.8	0.430	1.0E-15	7.6E-4
258.5	0.536	3.2E-14	3.5E-3



Vf=0V
tf=10ms
Vbias=-1V

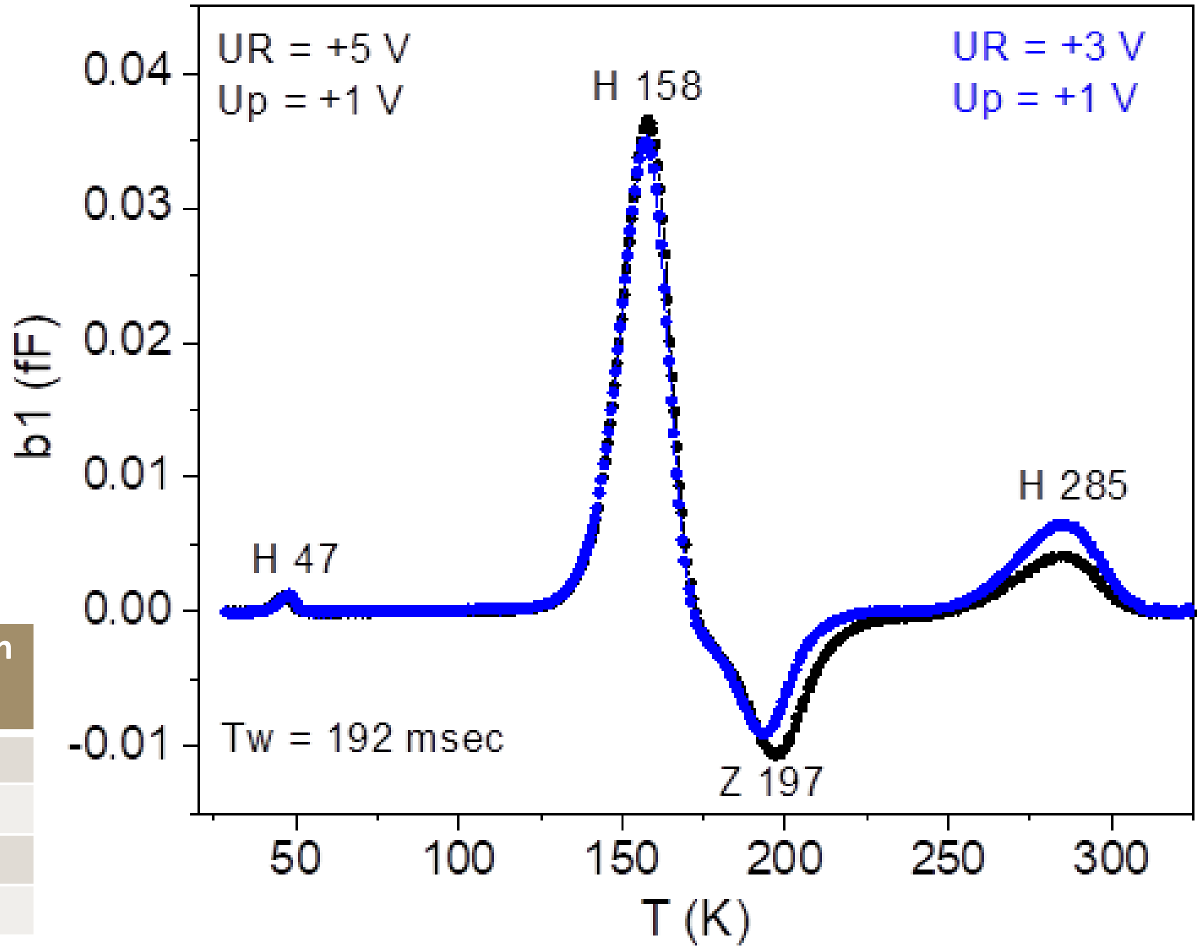
DLTS measurements: Schottky diode @Bucharest

DLTS spectrum:

- 3 maxima from hole traps
- 1 minimum, most likely from surface/interface states

trap parameters (Vbias=+5V; Vf=+1V):

Defect	Temp (K)	Ea (eV)	Sigma (cm2)	Defect concentration (cm-3)
H47	47	0.069	6.87E-17	2.49E10
H158	158	0.294	4.35E-16	9.32E11
Z197	197	0.439	1.85E-14	2.90E11
H285	285	0.611	3.76E-15	1.32E11

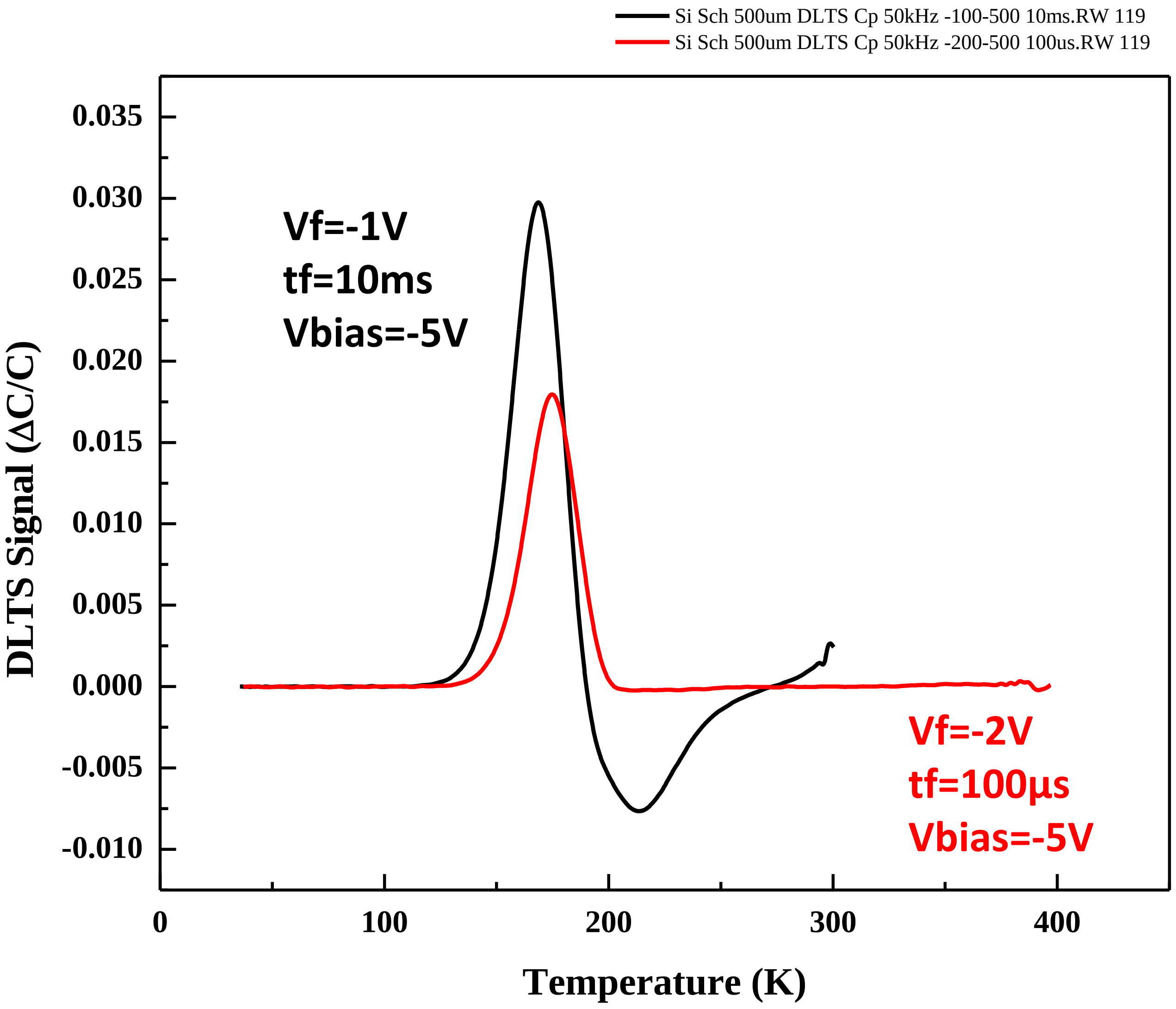


DLTS measurements: Schottky diode @Semetrol

DLTS spectrum:

- peak with 2 majority carrier traps
- ‘minority’ carrier trap
  ⇒ vanishes for reduced + shorter filling pulse
  ⇒ surface/interface states likely
- large majority carrier trap for larger filling pulses at room temperature

Midpoint temp (K)	E_t (eV)	Sigma (cm^2)	N_t/N_s
170	0.312	5.5E-15	7.8E-3
180	0.294	3.3E-16	2.2E-2

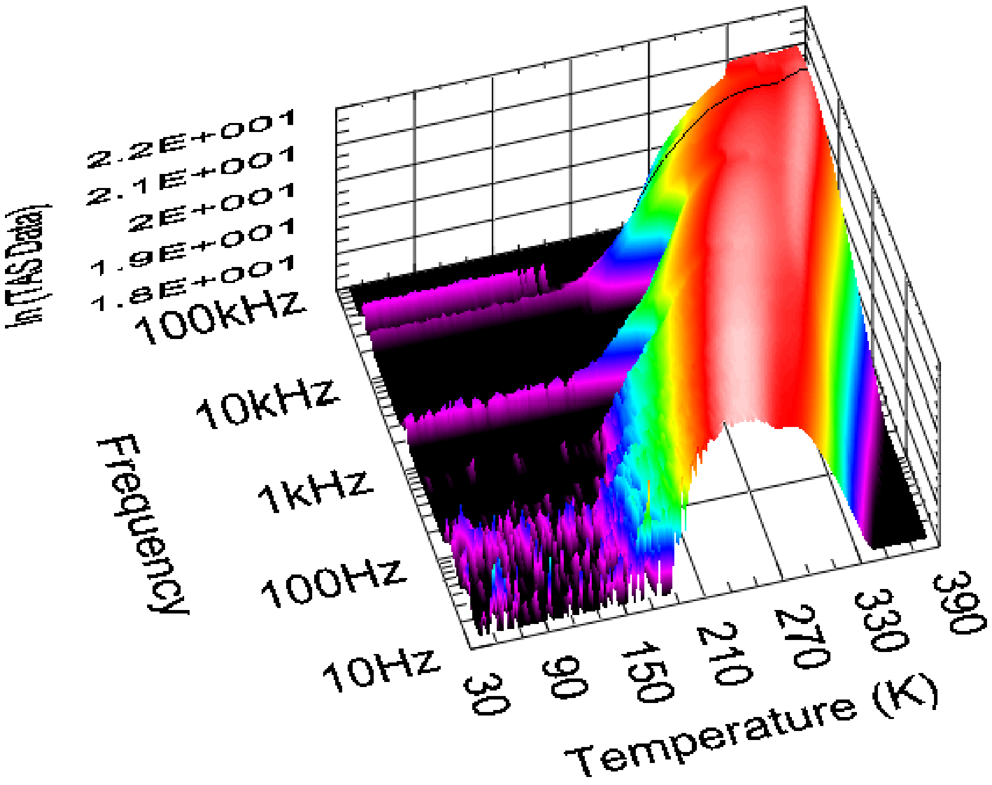


Thermal Admittance Spectroscopy (TAS)

- samples characterized with other spectroscopic techniques @Semetrol (DDLTS, IDLTS, IVT, PICTS, TAS)

TAS:

- measure capacitance C and conductance G as function of frequency and temperature
- defect contribution to C/G depending on test signal frequency and temperature
- steps in C or peak in G for thresholds
- steady-state measurement
- applicable for low-doped or high-resistivity materials, complements DLTS

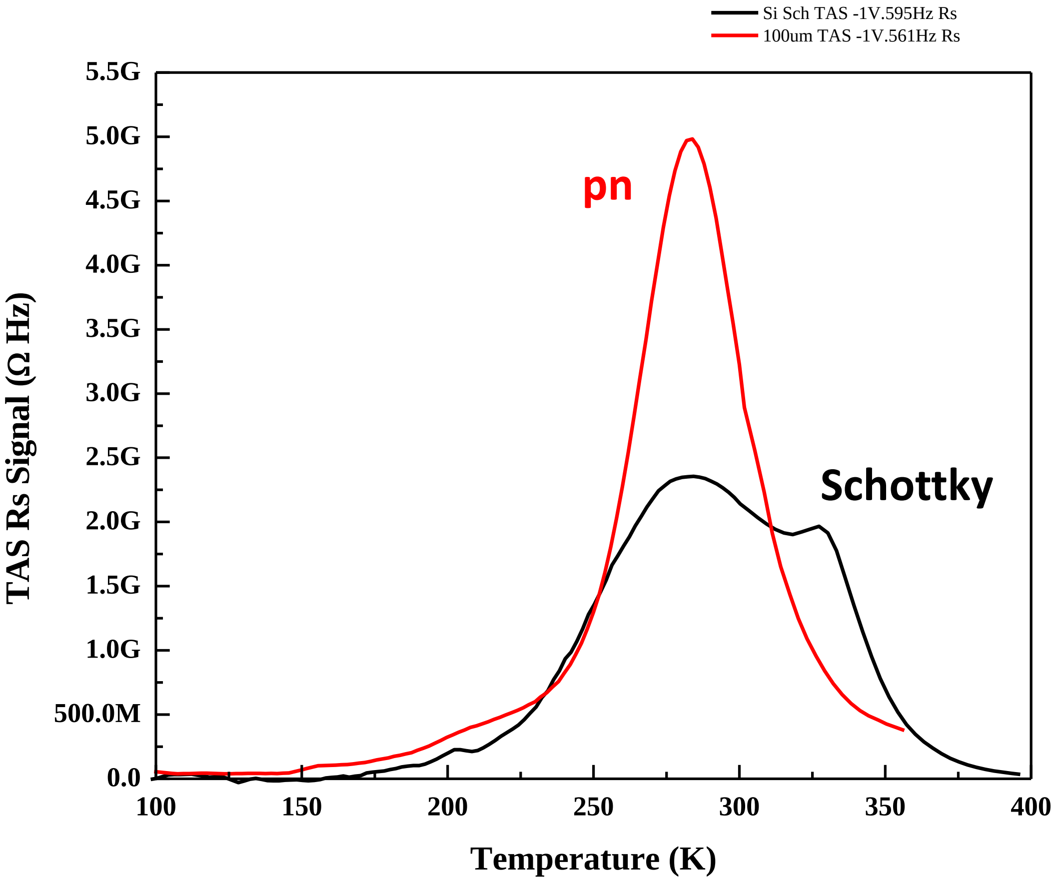


Thermal Admittance Spectroscopy (TAS)

TAS analysis:

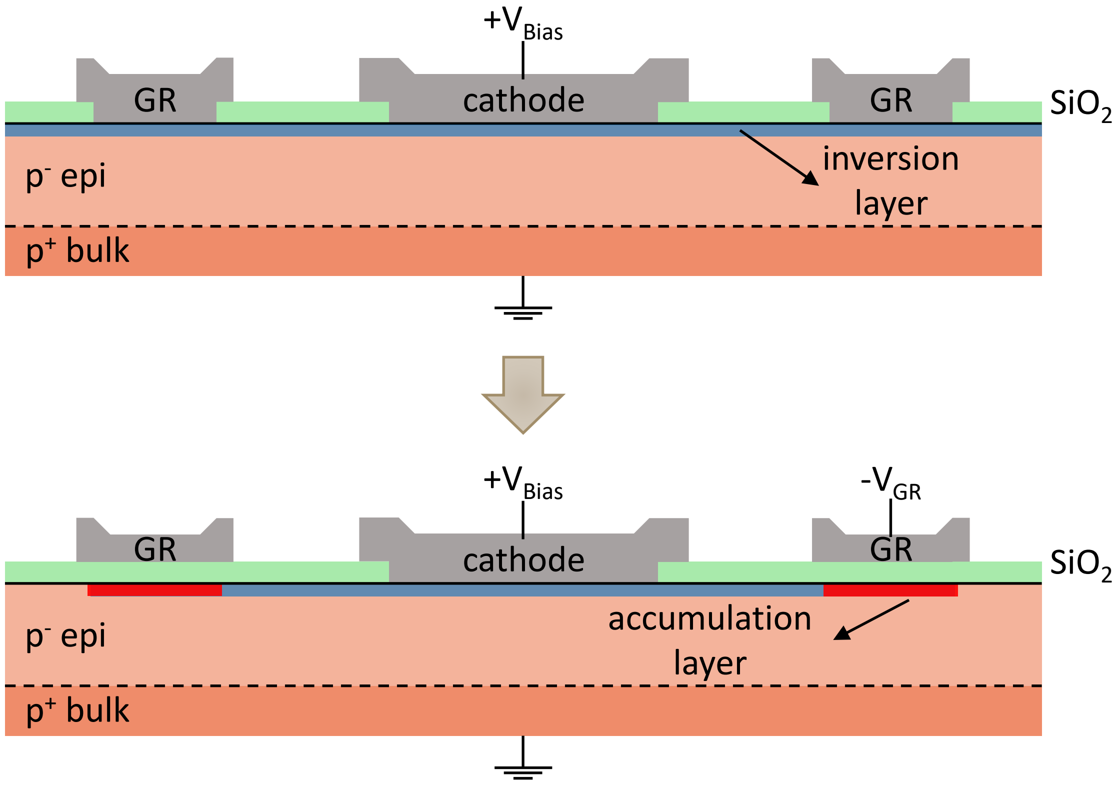
- higher trap energy in Schottky for similar peak
- second Schottky trap near mid-gap
- energy shift at different test voltages
  - ➢field dependence of trap energy
  - ➢might explain difference between Schottky and pn-junction (higher E-fields in pn diode)

Sample	V_{bias}	E_t (eV)	σ (cm²)
PN	-1V	0.384	1.1E-16
Schottky	-1V	0.498	1.6E-14
Schottky	-2V	0.467	3.0E-15
Schottky	-1V	0.664	3.5E-13
Schottky	-2V	0.614	3.7E-14



Reducing leakage current: MOS gate guard ring structure

- some diode runs on 1e13 cm^{-3} wafer had high leakage currents
- tests showed that cause was formation of electron inversion layer
- expected typical behaviour after radiation damage in oxide
  - outlook to actual behaviour after irradiation
- mitigate by modifying the masks to isolate GR on oxide
- apply low negative V to gated GR
  - accumulation layer formation in interface
  - limit inversion layer



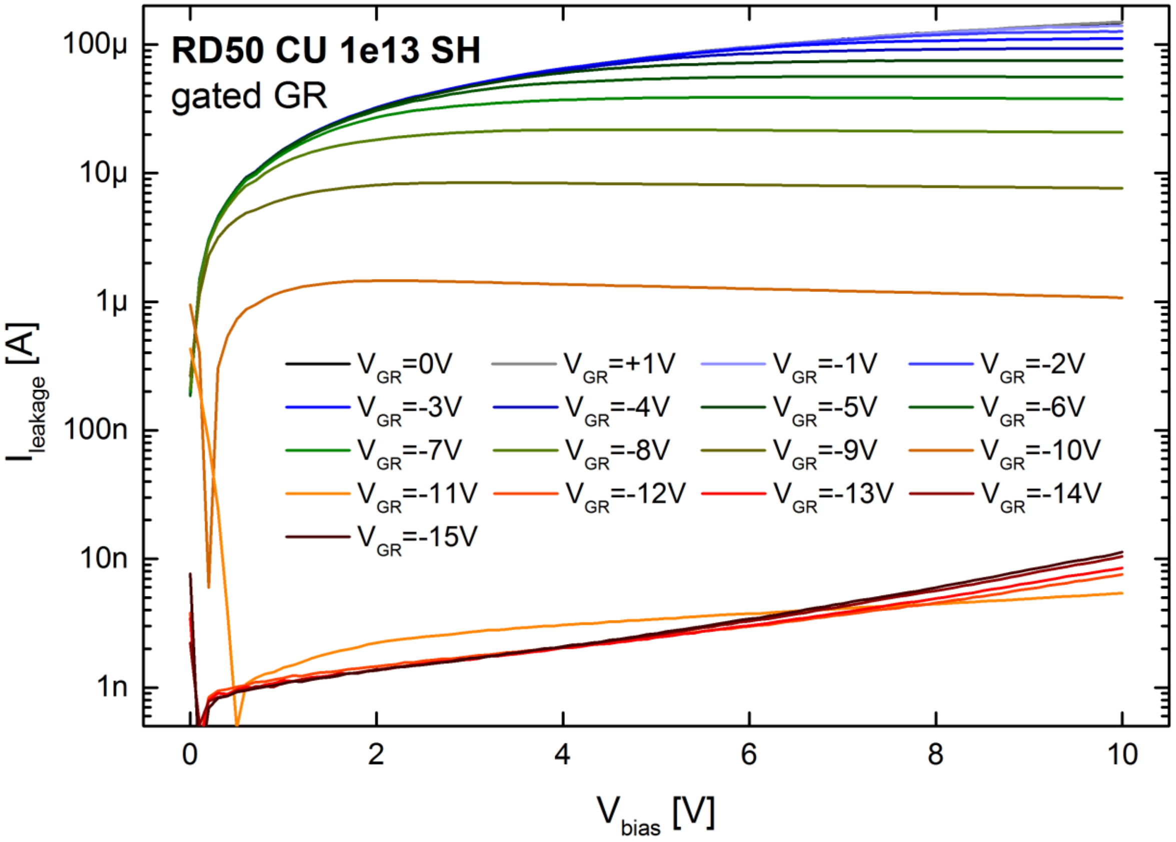
solve this issue **now**

⇒ improve performance of irradiated devices **later**

Reducing leakage current: MOS gate guard ring structure

- gated GR yielded expected results
- high leakage fully mitigated for V_{GR} <-10V
  - depending on oxide thickness
- devices even showed 'memory effect'
  - stable-ish charge traps in interface
  - further improvements during repeated scans

➢ looking forward to device irradiation



Summary & outlook

- testing has proceeded successfully after shutdown periods last year
- general electrical characterisation from IV/CV measurements, very detailed trap characterisation from DLTS and TAS
- fabrication efforts at RAL and CUMFF has ramped up
  - adaptability and flexibility of processing

Outlook:

- TCAD simulations of devices
- proton irradiations at Birmingham (in 2021), neutron irradiations at Ljubljana
- charge collection measurements