The MIMOSIS pixel sensor

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on behalf of IPHC-IKF-GSI collaboration

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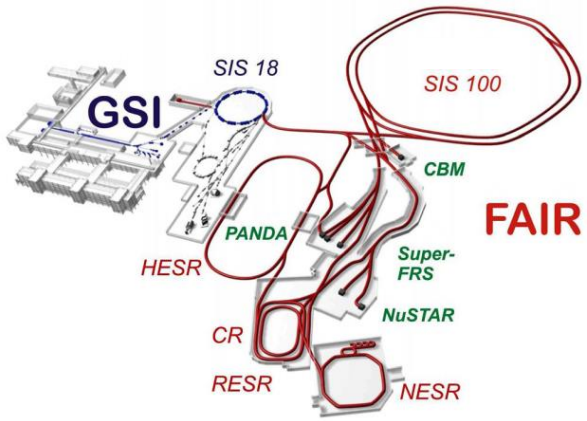
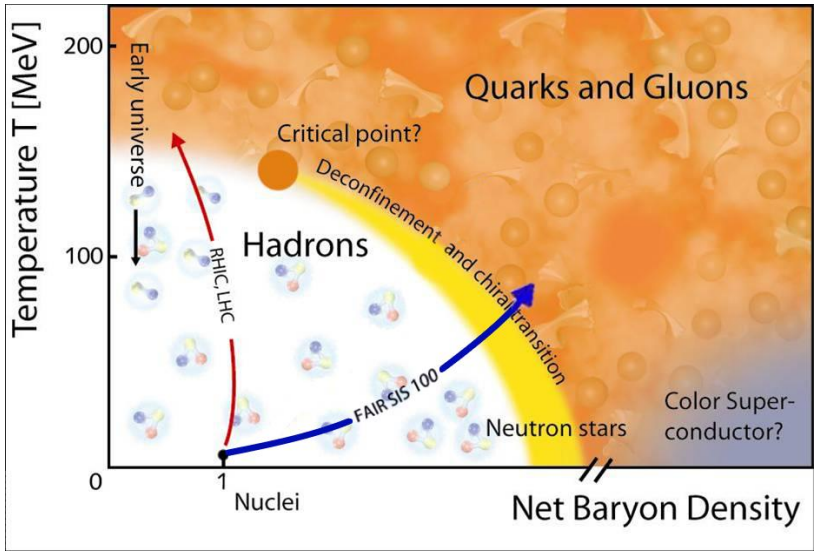
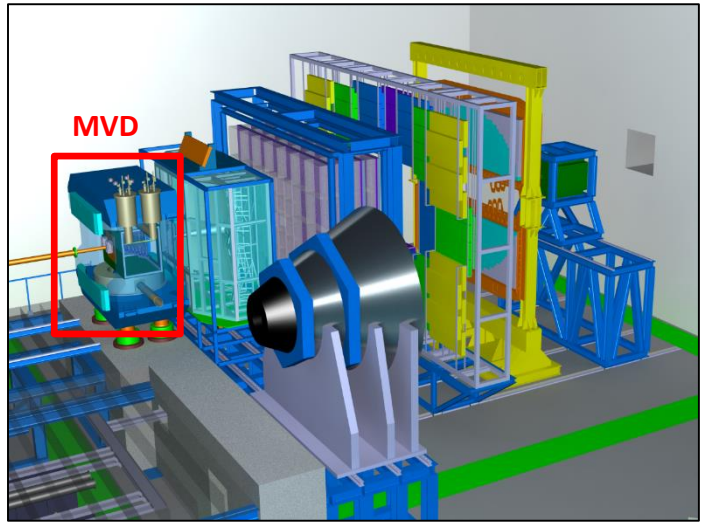
(05P19RFFC1)

The Compressed Baryonic Matter experiment @ FAIR

- Explore phase diagram at region of highest net-baryon density
- Fix target
- Beam start is schedule for end 2024



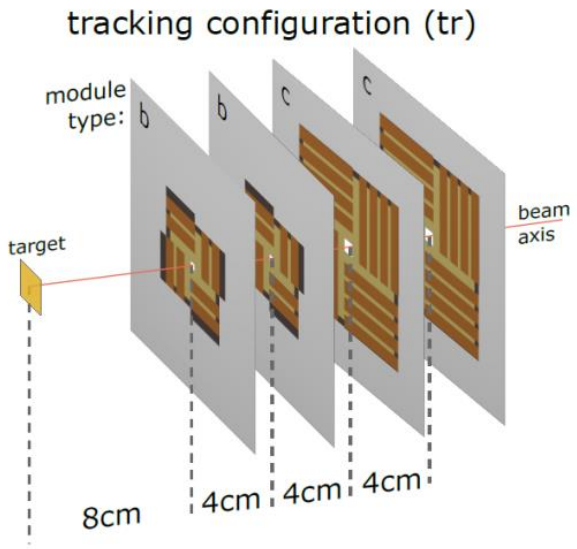


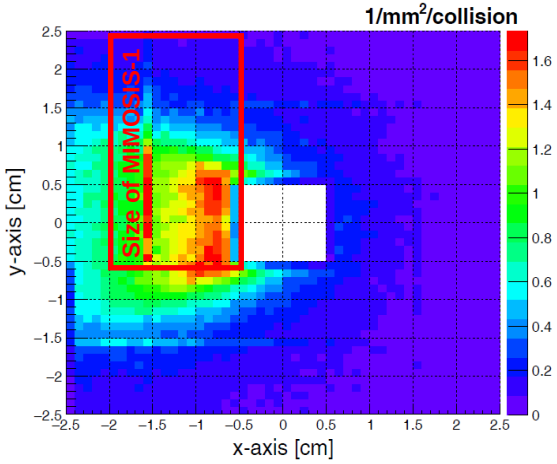


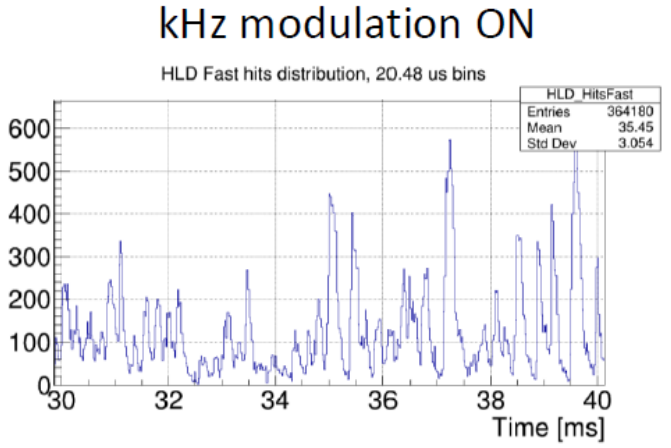
April 2021

Micro Vertex Detector

- Aim for high collision rate capability
  - 100 kHz Au+Au @ 11 AGeV
  - 10 GHz p+Au @ 30 AGeV
- Aim to contribute to tracking
  - 4 planar detector stations
- Aim for good sec. vertex resolution
  - Operate in target vacuum
  - First station 5 cm from target (in vertexing configuration)
  - ~ 5 µm resolution
  - Thin stations
    - ~ 0.3 % X_0 (first station)
    - ~ 0.5 % X_0 (other stations)
- Sensor must handle occupancy gradients in space
- Sensor must handle beam fluctuations in time







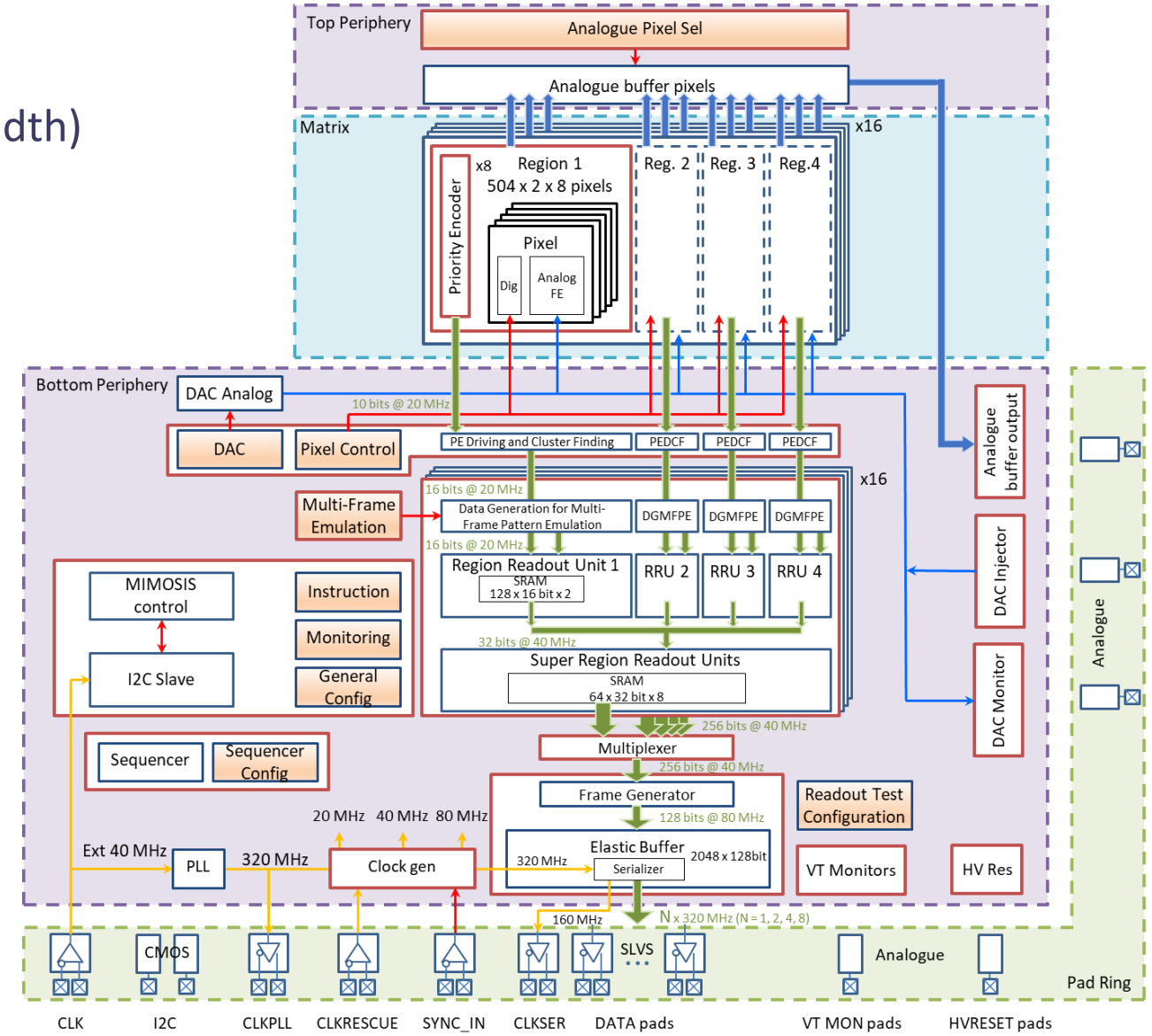
MIMOSIS Requirements

	Requirement
Spatial resolution	~5 µm
Time resolution Triggerless without dead-time	~5 µs
Sensor thickness	~50 µm
Radiation length	~ 0.3 % X_0 (first station) ~ 0.5 % X_0 (other stations)
Power dissipation	<100 - 200 mW/cm²
Operation temperature	- 40°C to +30°C
Temperature gradient on sensor	5 K
Radiation* (non-ionizing)	~ $7x10^{13}$ n_{eq}/cm²
Radiation* (ionizing)	~ 5 Mrad
Radiation gradient on chip	100%
Heavy Ions-tolerance	10 Hz/mm²
Rate (average/50 µs peak)	200/800 kHz/mm²

* No safety factor

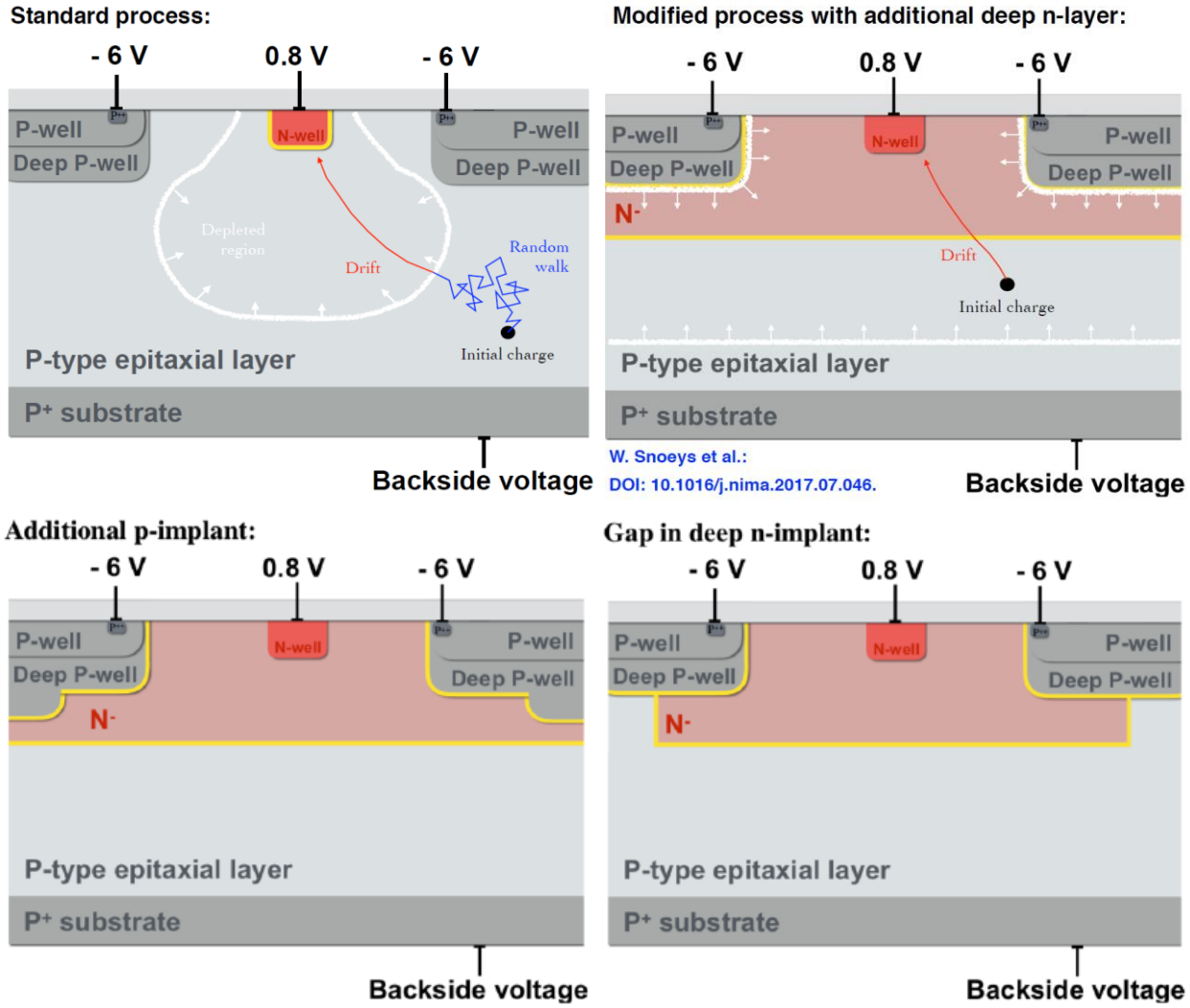
MIMOSIS diagram

- Matrix dimension: 1024 col. X 504 row
- Pixel dimension: 26.88 µm (height) x 30.24 µm (width)
- Integration time: 5 µs
- Tower Semiconductor 180 nm
- 4 sub-arrays for threshold adjustment
- 3 steps prototyping:
  - MIMOSIS0 small scale prototype (2017)
  - MIMOSIS1 first full scale prototype (2020)
  - MIMOSIS2 final prototype (2021)
  - MIMOSIS3 pre-production run (>2022)



Charge collection

- Tower Semiconductor 180 nm
  - 4 process variants and various epi layer thickness
  - Optimize charge collection
    - efficiency after irradiation
  - Based on the experience accumulated with ALPIDE and MALTA/MONOPIX
- Goals:
  - Increase depletion region with a small collection diode
  - Avoid charge traps due to low lateral electric field on the edges
- Additional degree of freedom for MIMOSIS:
  - AC coupled pixels to increase collection diode voltage

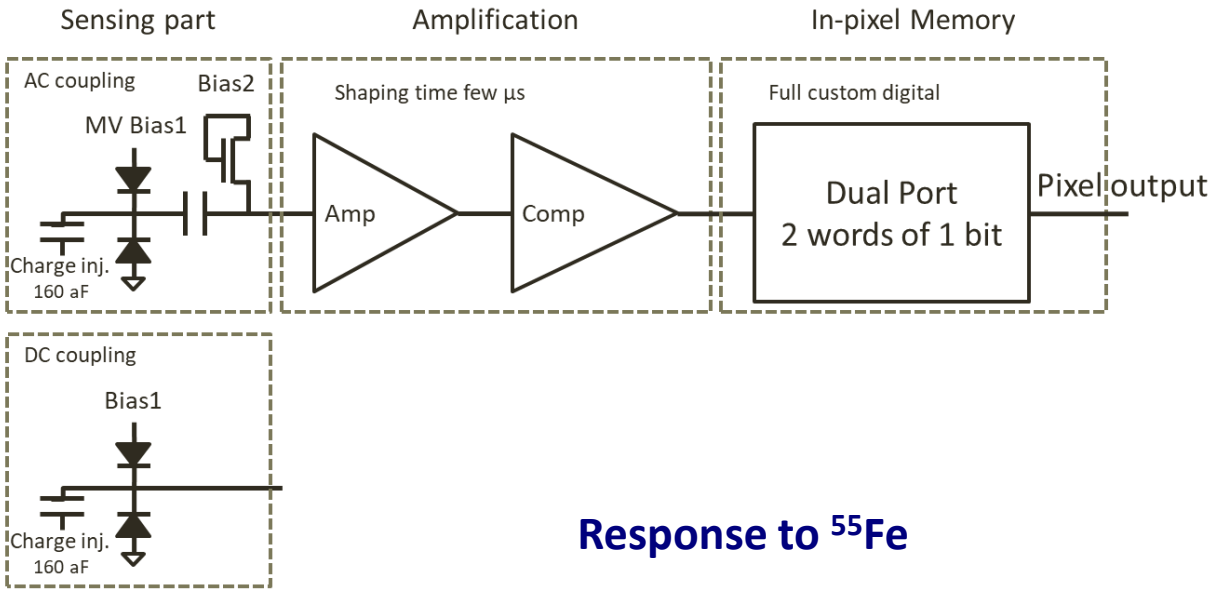


Study of the depletion depth in a frontside biased CMOS pixel sensors
J. Heymes https://doi.org/10.1088/1748-0221/14/01/P01018

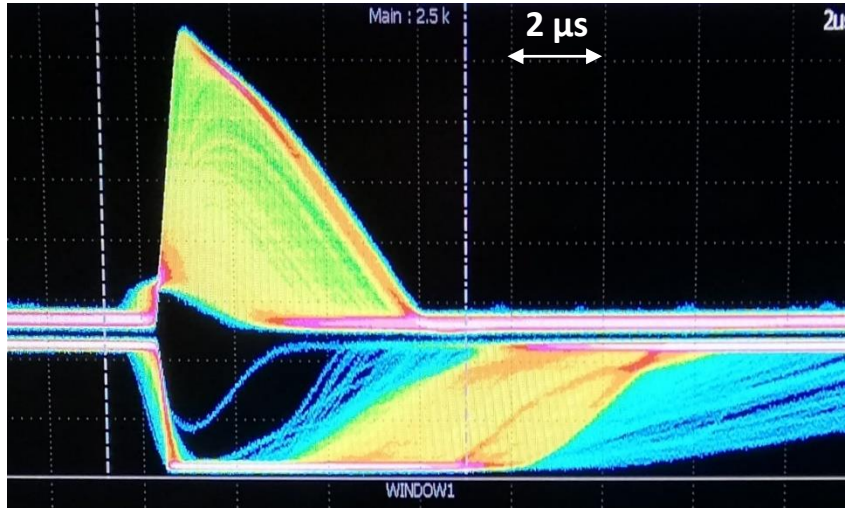
Monolithic CMOS sensors with a small collection electrode
Seminar by M. Munker at Royal Holloway University of London (2019)

Pixel

- 2 versions of sensing part evaluated:
  - DC or AC coupled
    - Polarization of the collecting diode to ~10-20 V in AC
    - Variants are in MIMOSIS0 and MIMOSIS1 prototype
- Amplification:
  - Similar to ALPIDE
  - Non linear and with clipping technique
- In-pixel Memory:
  - Dual ports for triggerless framing (5 µs)
    - One to write the hit (current frame)
    - One to read the hit (previous frame)
  - Avoid multiple counting
    - For impact which spread over several capture windows
  - High density full custom block
- Amplifier and sensing part tested in MIMOSIS0



Response to ^{55}Fe



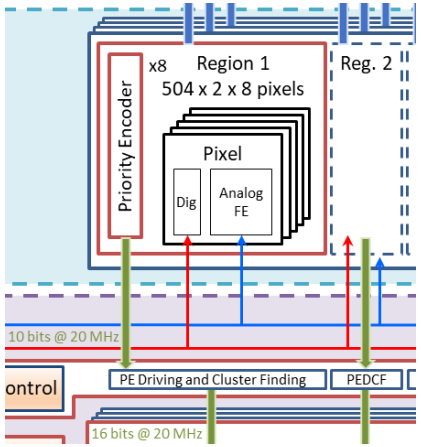
Amplifier output

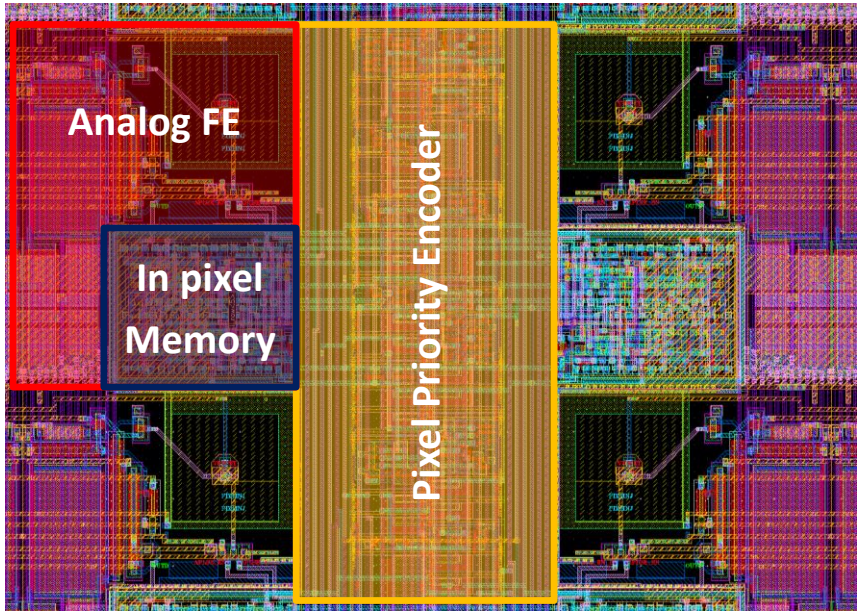
Comparator output

M. Deveaux NIM A 958 (2020) 162653

Matrix readout

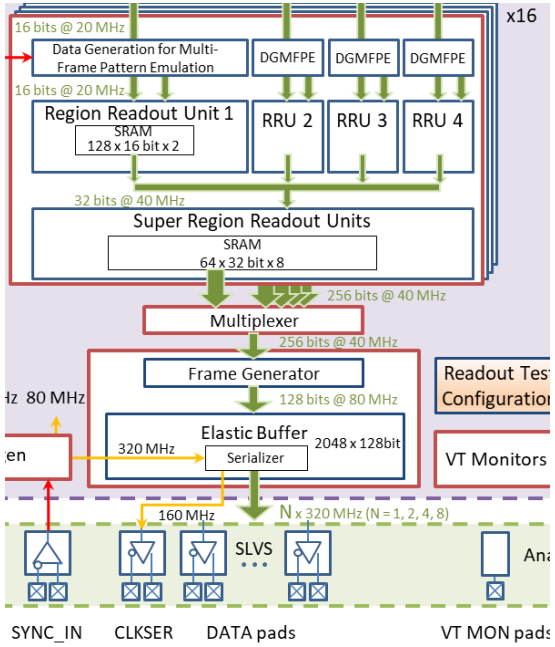
- Priority Encoders Functions:
  - Give the address of the hit pixel with the highest priority
  - Aim the pixel reset signal to the selected pixel
- 2 levels of priority encoders to read a Region:
  - Pixel level
    - inside the pixel array to read 2 columns of 504 pixels
  - Region level
    - at the bottom of the pixel array to read 8 Pixel level Priority encoders
- Characteristics:
  - Reading is done at 20 MHz (100 pixels/frame/region)
    - ~3 MHz/mm² ➔ 1 MHz/mm² (hit multiplicity of 3) > 800 kHz/mm²

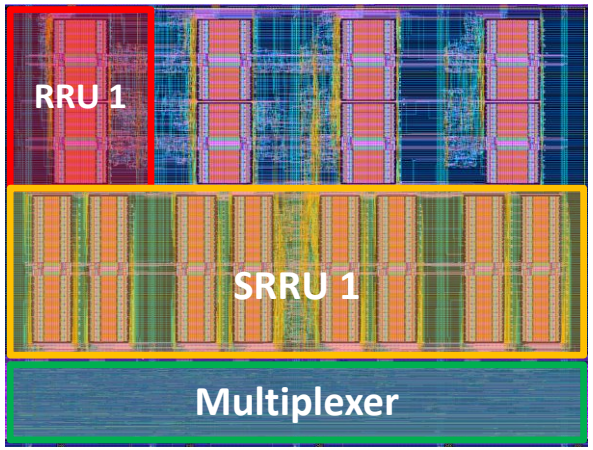


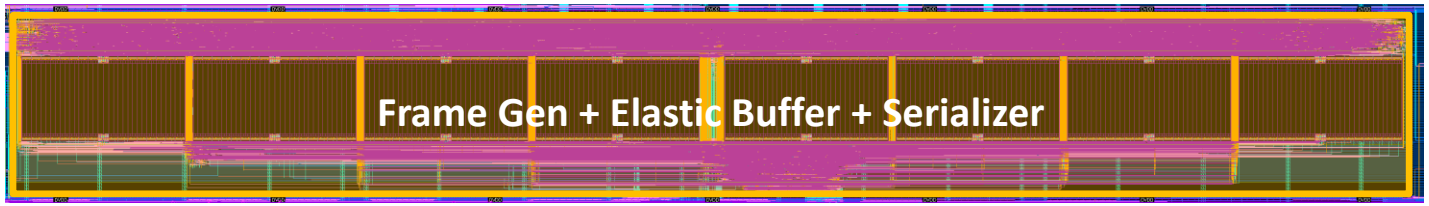


Bottom periphery readout

- Function:
  - Averaging the data fluctuations over the pixel array (gradient in space)
  - Averaging the data fluctuations in time (beam fluctuations)
  - Works like a funnel for the data
    - 20.48 Gb/s (16 bits x 64 regions @ 20 MHz spread over ~3 cm)
    - 2.56 Gb/s (8 serial links @ 320 Mb/s spread over ~3 mm)
- 3 levels of dual port memories
  - 64 Regions and 16 Super-Region (for space averaging)
    - Write frame N in parallel @ low speed
    - Read frame N-1 in serial @ high speed
    - No data loss between matrix readout and Super-Region
  - 1 elastic buffer (for time averaging)
    - Works like a circular buffer
    - Write speed 10.24 Gb/s > Read speed 2.56 Gb/s (for 8 links)
    - Configurable number of serial links (8,4,2 or 1)
    - Can store 3 x nominal beam during 50 µs

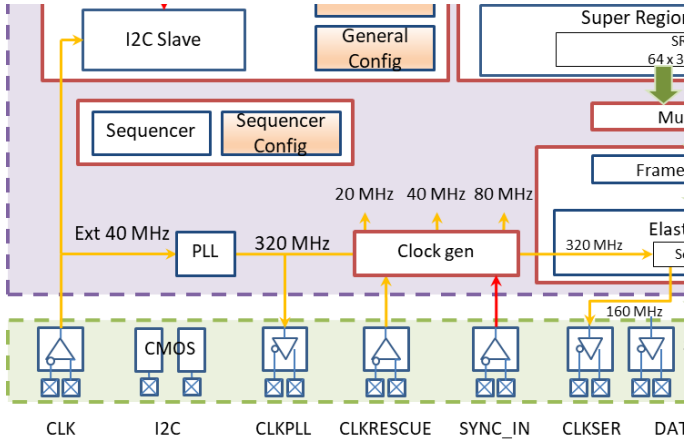






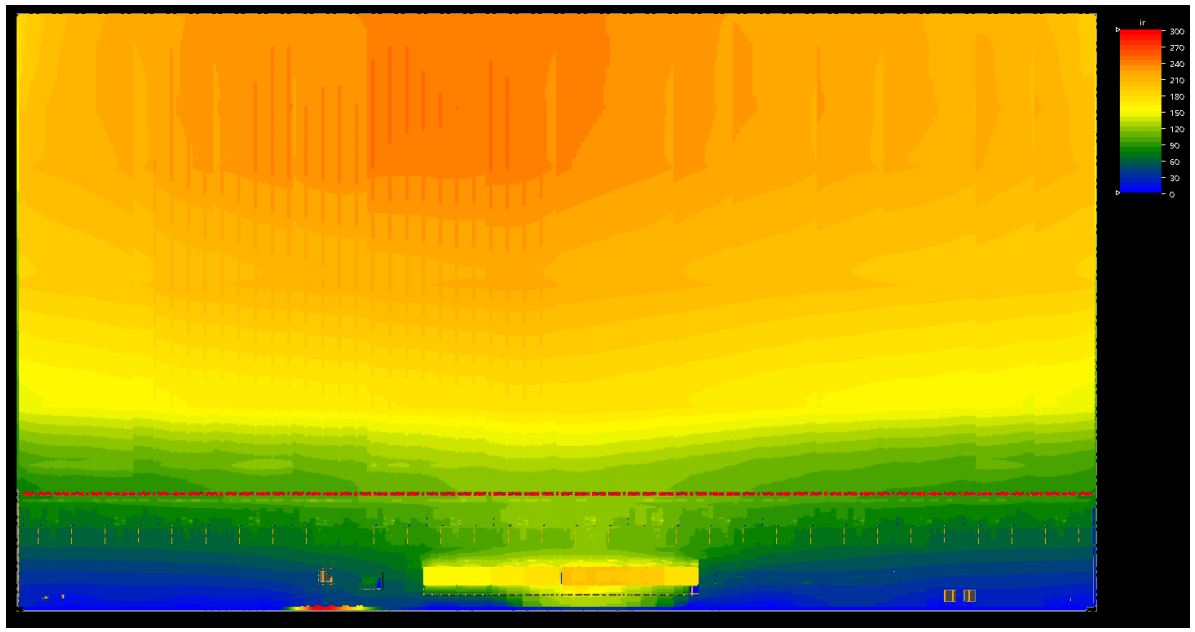
Multi-chips synchronization

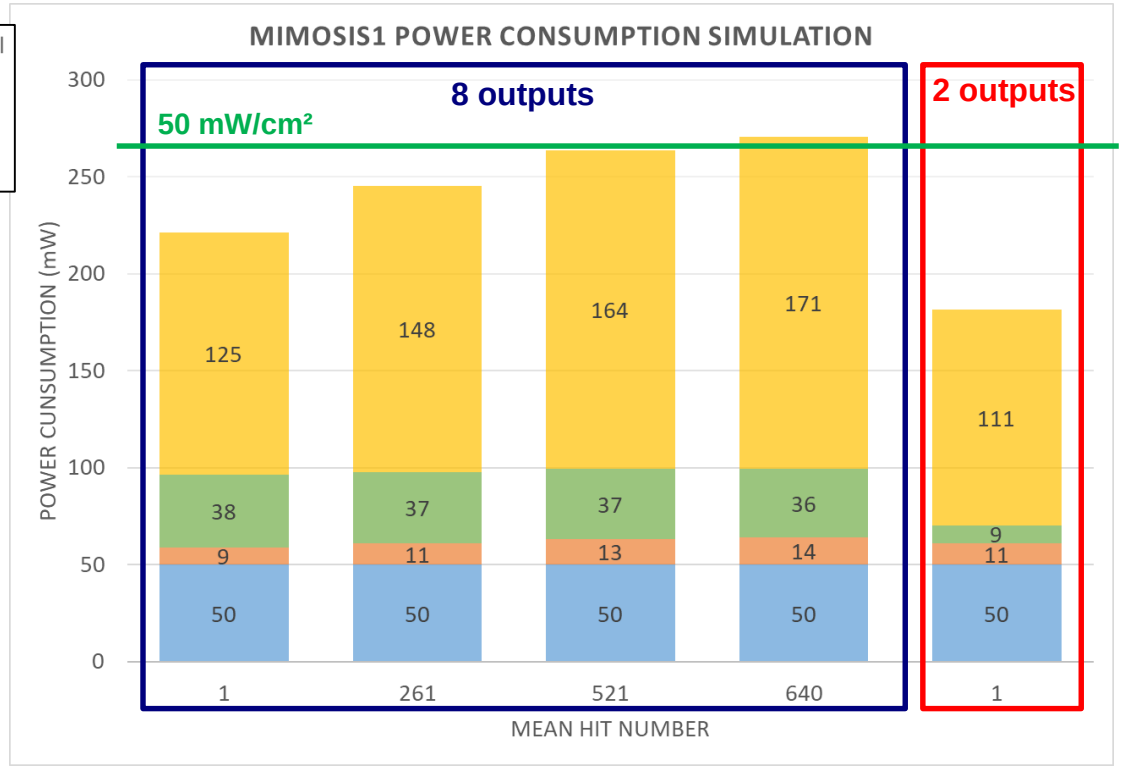
- No trigger available
  - Need a mechanism to synchronize several chips for common base time
- All the clocks derive from the 320 MHz clock from the PLL
  - Synchronisation pad (SYNC_IN) acts like a reset for the clock generator
- Principle
  - Synchronisation signal is latched 2 times
    - With external 40 MHz clock
    - With 320 MHz clock from the PLL
  - Timing constraints for the synchronisation signal over several chips is relax to the 40 MHz clock

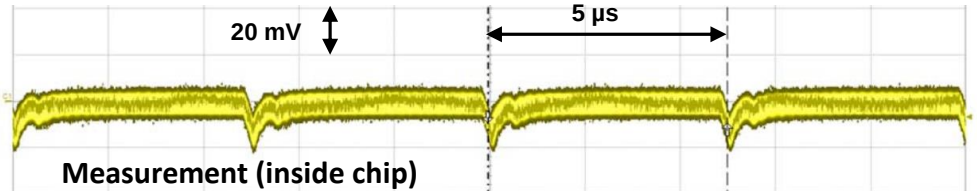


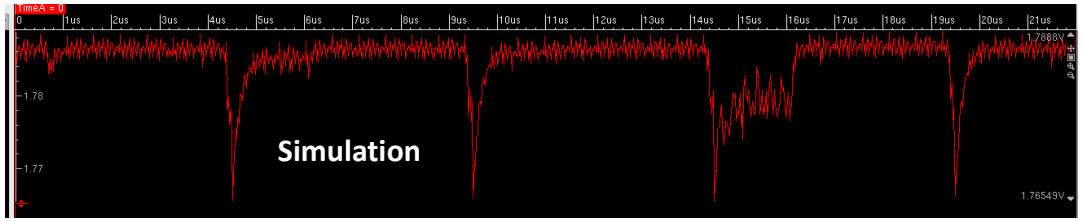
Power consumption

- Well below the requirements:
  - ~50 mW/cm² (for whole chip surface)
  - To be confirmed by measurement
- Dominated by:
  - The number of hits for the bottom periphery
  - The number of outputs in the padring
- Voltage drop will be mitigate in next submission









Testability and SEE mitigation

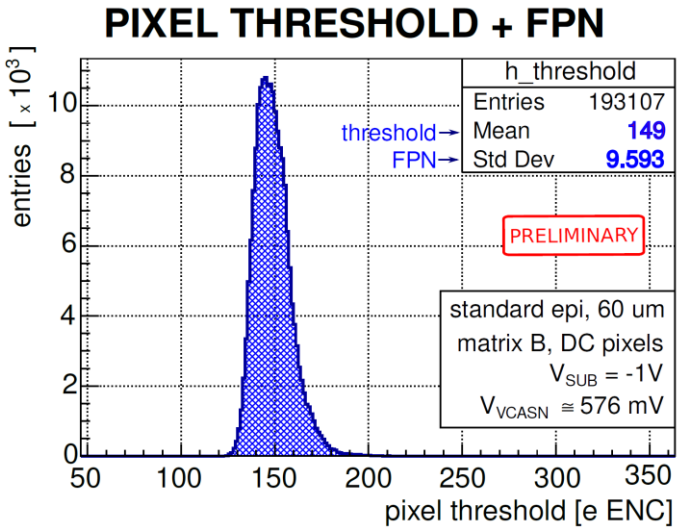
- Several levels of testability
  - Pixel level
    - Analogue and digital pulsing over the whole matrix
    - Output of the amplifier and comparator of the first row is accessible
  - Region level
    - Generates data over several frames for each region
  - Serializer level
    - Serialize a 128 bits words over the 8 serializer

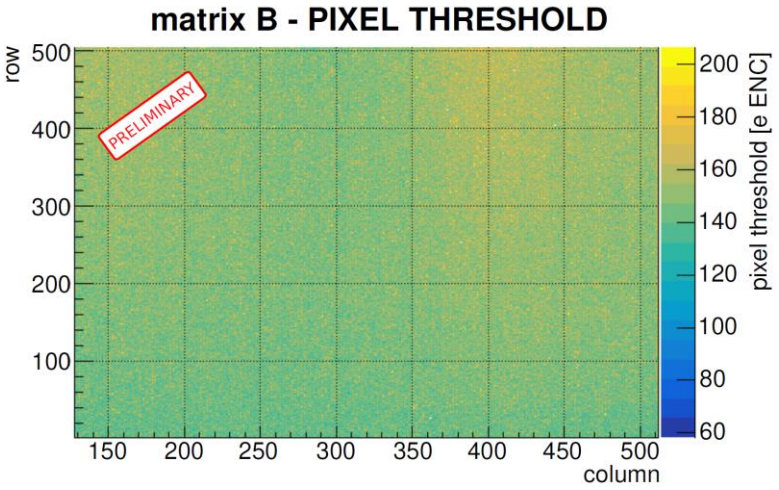
- Single Event Effect mitigation*
  - All FSM are triplicated
  - All configuration registers use a self corrected hamming register
  - Partial triplication of clock and reset trees
    - Full trees in next submission
  - Only a CRC check for data corruption
  - Classic latchup protection

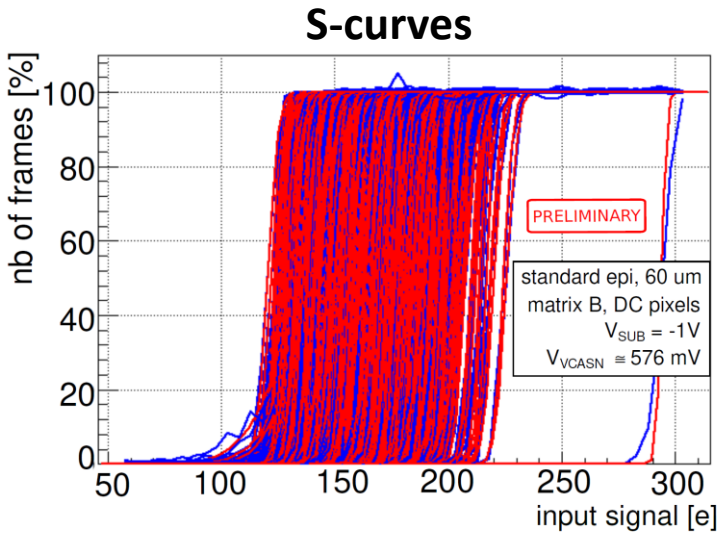
*Y.ZHao PoS(TWEPP2019)131

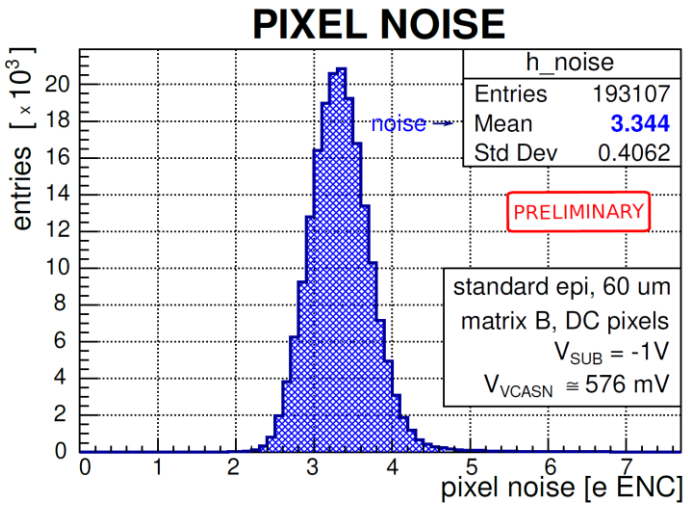
Preliminary Results DC pixel

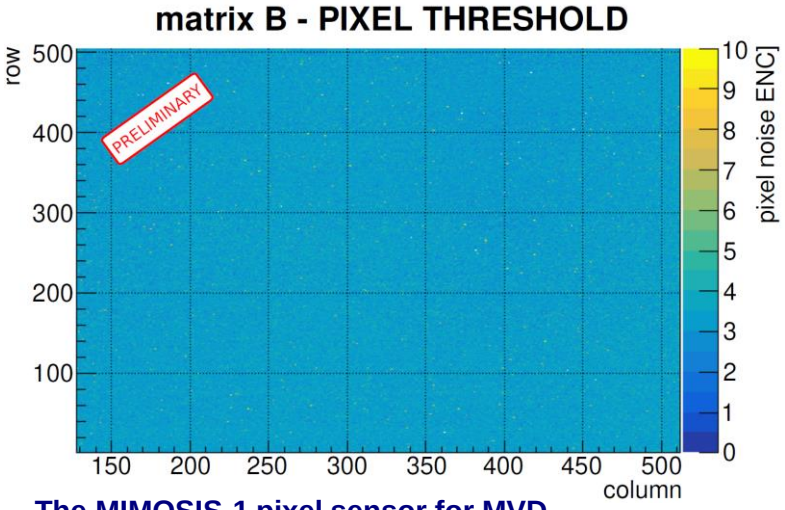
- Matrix B (DC pixels 24 regions)
  - Vsub=-1 V
  - Threshold scan obtain through charge injection
  - Preliminary conversion factor (mV/e-)
    - 25 % of precision
  - Exemplary Results:
    - Pixel noise: ~3.4 e- ENC
    - Threshold: ~150 e- ENC
    - FPN: ~10 e- ENC





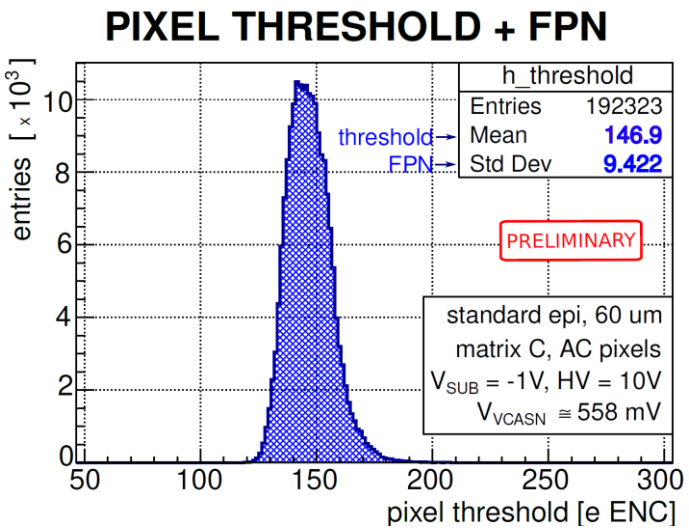


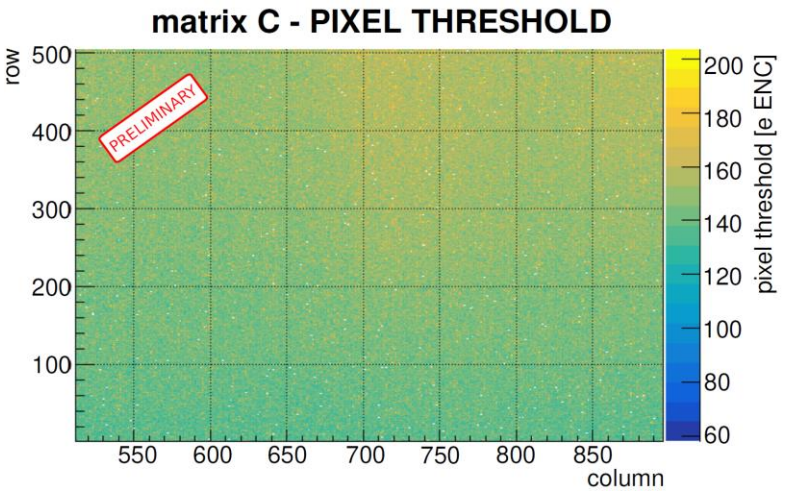


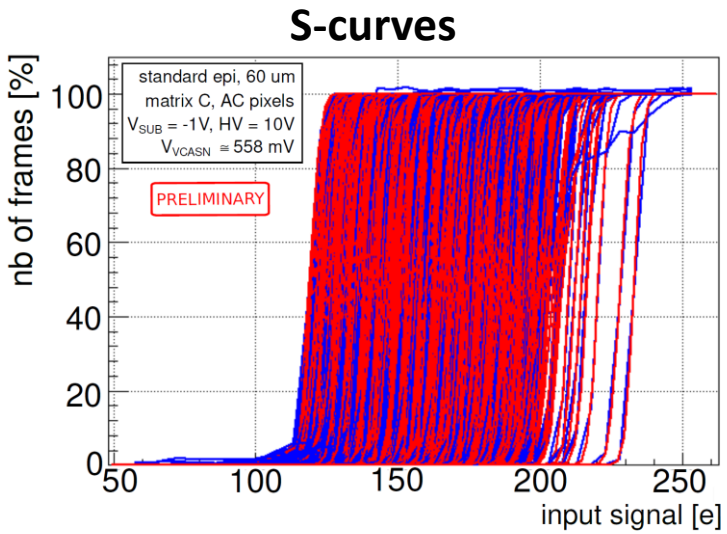


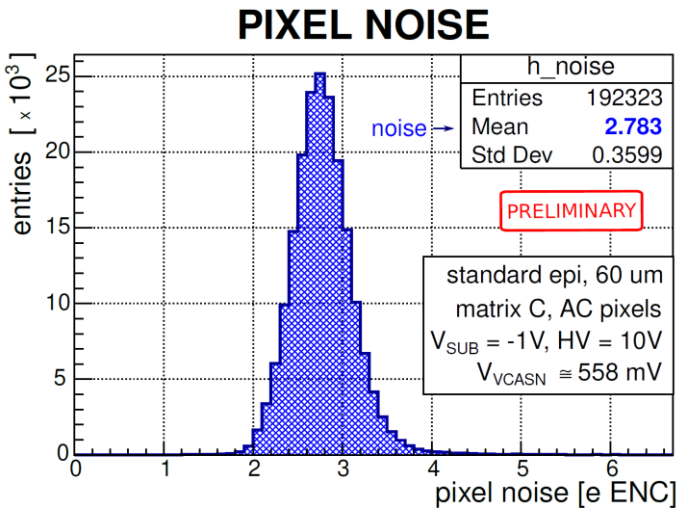
Preliminary Results AC pixels

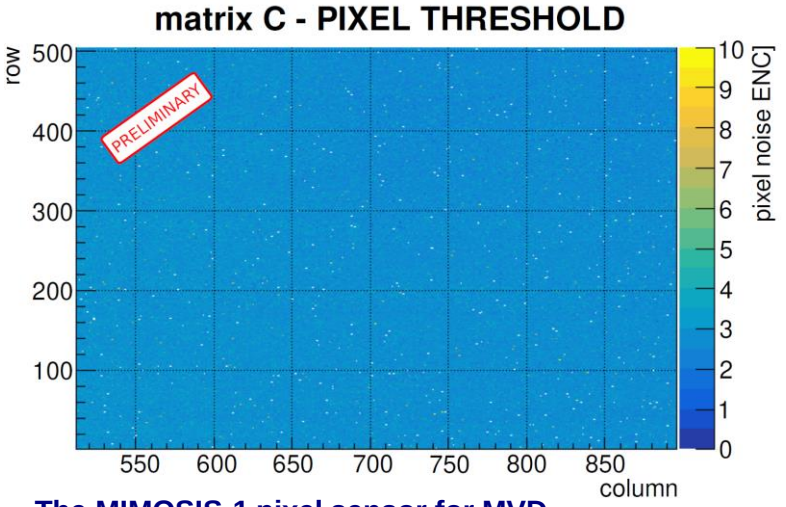
- Matrix C (AC pixels 24 regions)
  - Vsub=-1 V, Diode pol.=10 V
  - Threshold scan obtain through charge injection
  - Preliminary conversion factor (mV/e-)
    - 25 % of precision
  - Exemplary Results:
    - Pixel noise: ~2.8 e- ENC
    - Threshold: ~150 e- ENC
    - FPN: ~10 e- ENC











The MIMOSIS-1 pixel sensor for MVD
Roma Bugiel 37th CBM collaboration Meeting

Conclusion

- MIMOSIS1 is the first full scale prototype for the MVD
  - High peak rate to handle occupancy gradients and beam fluctuations
  - Triggerless without dead time
  - Ultra low power MAPS
  - Single Event Effect hardened for Heavy Ions (fix target)
  - Early results seem promising
- Next steps:
  - Pursue heavy testing program
    - Process flavours, pixels variants, irradiation
    - Lab tests, SEE/latchup tests
    - Beam tests planned in the coming months
      - Measurement of detection efficiency, spatial resolution, fake hit rate
      - Will help the pixel selection for MIMOSIS2
  - Submission of MIMOSIS2 after this summer
    - Add missing features, fix few bugs
    - Focus on promising pixels and processes

Thank You