CMS Phase-2 Inner Tracker Upgrade

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(on behalf of the CMS Experiment)

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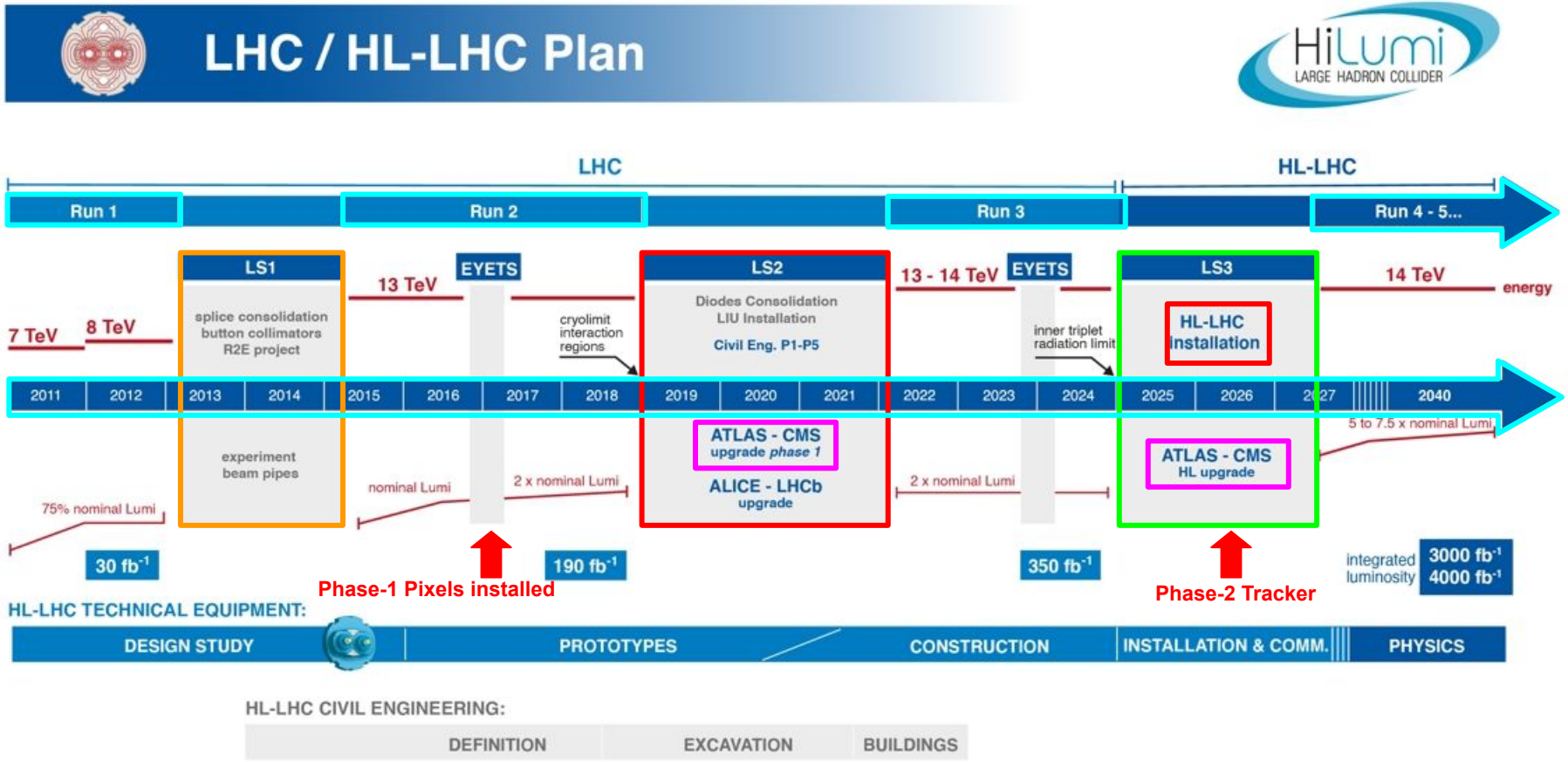
HL-LHC Schedule

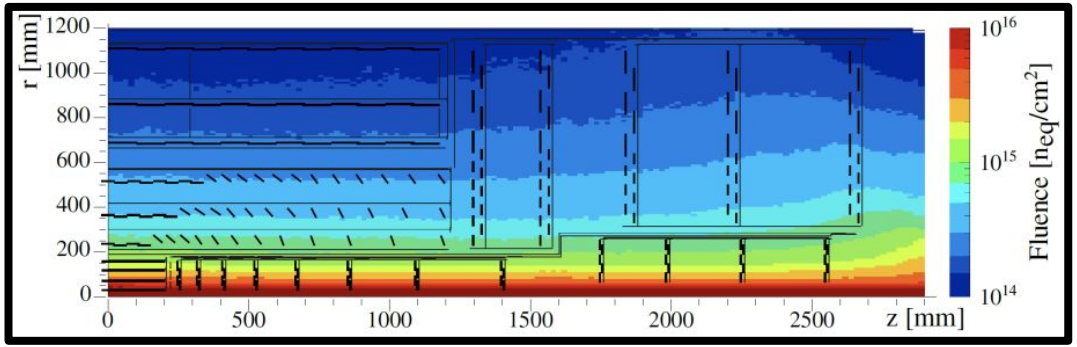


Motivation

Experimental Conditions	LHC → HL-LHC
Pileup	25 → 200
Hit rate	0.58 → 3.2 GHz/cm^2
Latency	3.2 → 12.8 μs
L1 Trigger rate	100 → 750 kHz
Radiation	300 → 3000 fb^{-1}

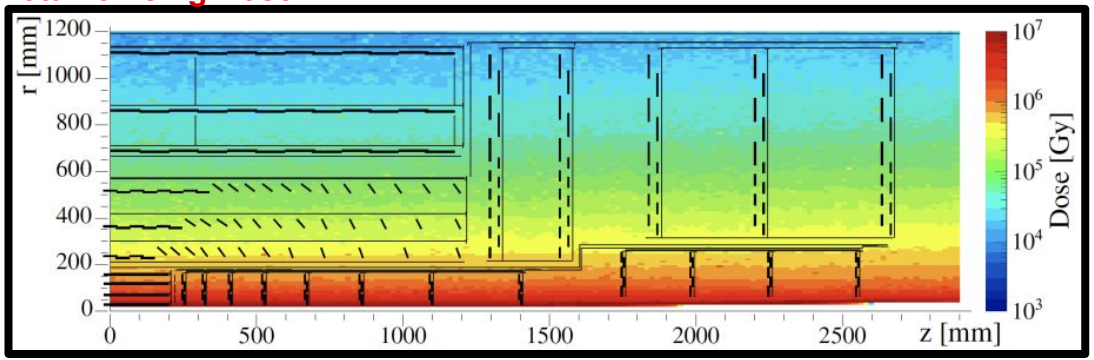
Requirements	Outcome
Increased granularity	Smaller pixels, Low occupancy
Increased coverage (|η|≤ 4)	Improved physics performance
Reduced material budget	improving tracking performance
Lower detection threshold	good resolution, two track separation
Simple installation and removal	Quick maintenance, no beam pipe removal

Fluence



Innermost layer: 2.3x10^{16} n$_{eq}$/cm^2, Outer & Service cylinder: 10^{15} n$_{eq}$/cm^2

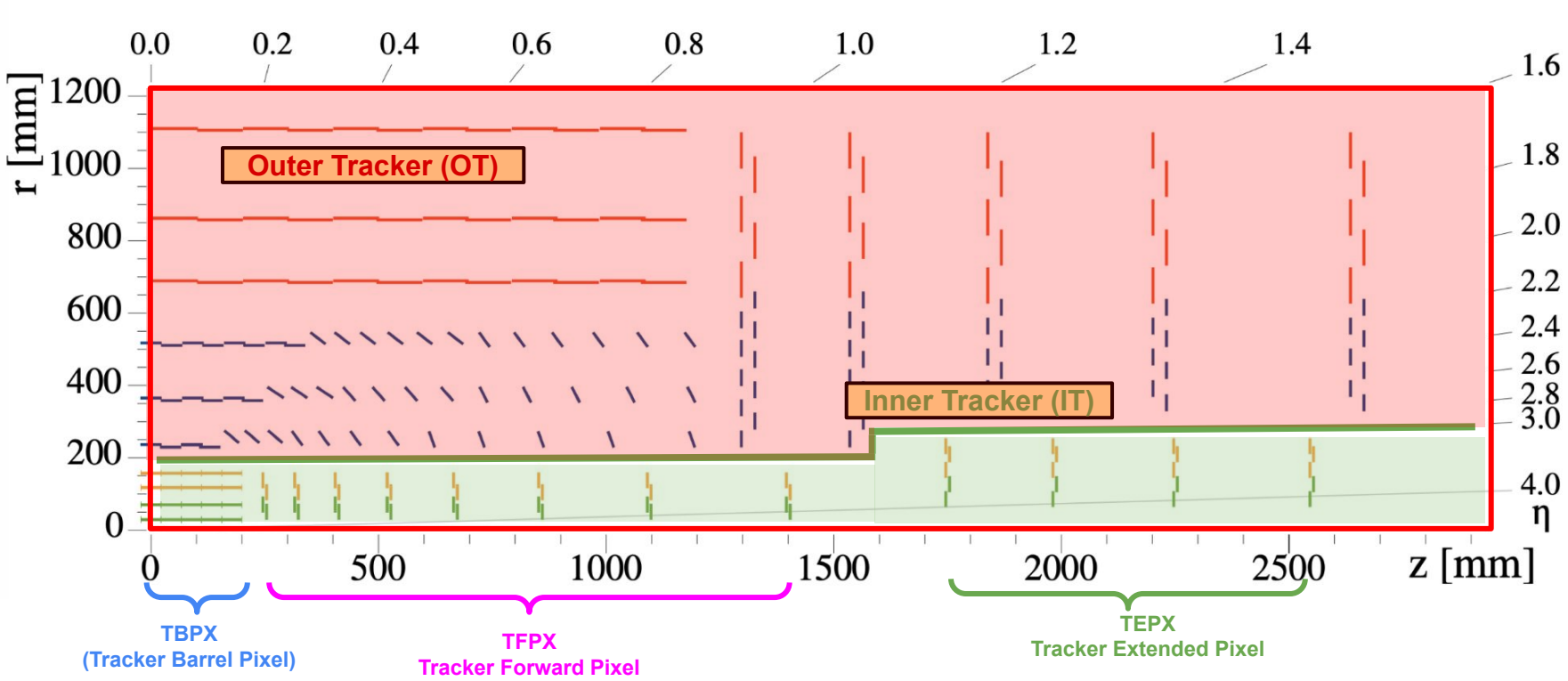
Total Ionising Dose



Innermost layer: 1.2 Grad, Outer & Service cylinder: 100 Mrad

1 Gy =100 rads

Phase 2 Tracker

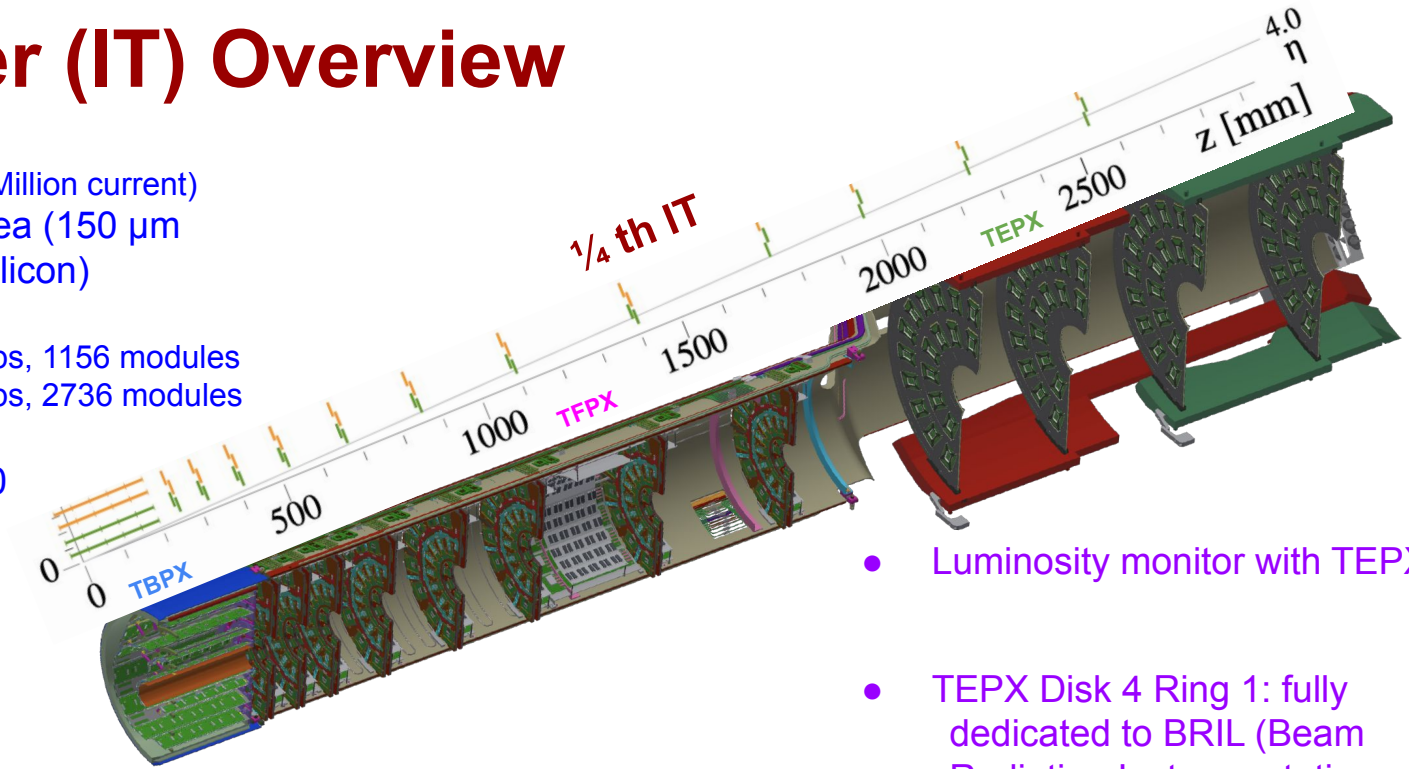


About 220m^2 of silicon detector:

- **Inner Tracker**: pixel modules (1x2 pixel-chip and 2x2 pixel-chip)
- **Outer Tracker**: pixel-strip and strip-strip modules

Inner Tracker (IT) Overview

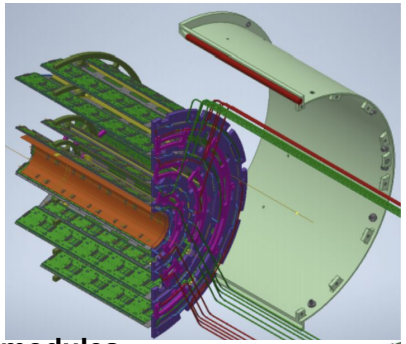
- 3892 modules
  - 2 Billion pixels (124 Million current)
- 4.9 m^2 silicon sensor area (150 µm thickness) (~1.7 kg of silicon)
- Hybrid modules with
  - 2 (1 × 2) readout chips, 1156 modules
  - 4 (2 × 2) readout chips, 2736 modules
- Occupancy < 0.1%
- Coverage up to |η| = 4.0



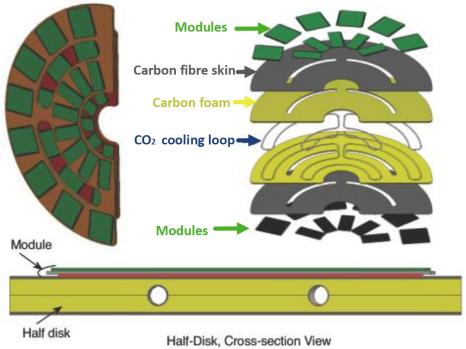
- Luminosity monitor with TEPX
- TEPX Disk 4 Ring 1: fully dedicated to BRIL (Beam Radiation Instrumentation and Luminosity)
- Simple mechanics:
  - Can be removed for maintenance
  - Barrel splits in half at z ~ 0
  - Disks with flat geometry (unlike turbine)
- Features a two-phase CO2 cooling system (nominal temp of the coolant -35°C)
  - 50-60 kW power budget

Mechanical support and Cooling

- Light Carbon Fiber support structures and cooling pipes shared among modules
- Low mass CO2 evaporative cooling removes heat, module to operate sensors below -20°C



TFPX Support - exploded view



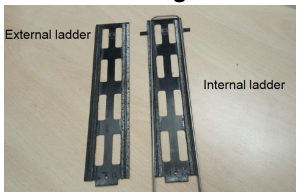
- **A ½ disk is composed of two Dees:**
  - Odd dee: ring 1+ring 3
  - Even dee: ring 2+ring 4
- **Modules of arranged on both sides of a dee- "sandwich" structure**

Prototype TFPX Dee

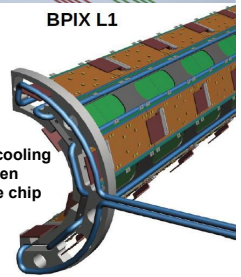
TBPX

Both faces of TBPX ladders loaded with modules

Modules arranged on ladder

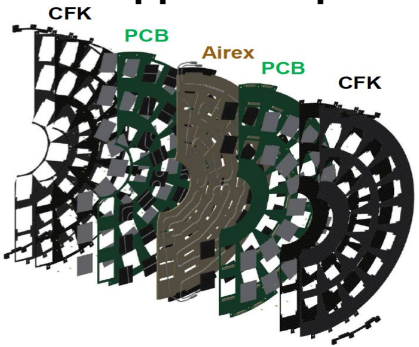


BPIX L1



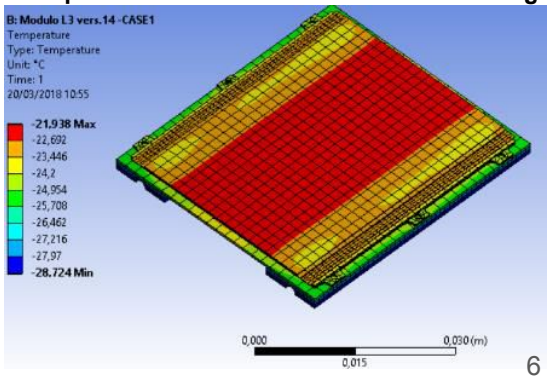
TBPX L1 cooling pipes driven Below the chip hotspots

TEPX Support - exploded view

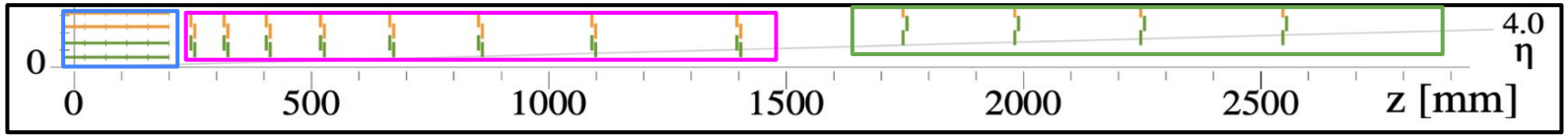


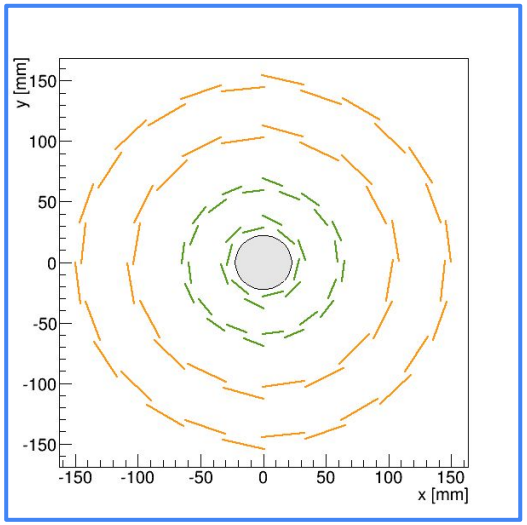
- **A disk is composed of one Dee with modules on both sides:**
  - Odd side: ring 1 + 3 + 5
  - Even side: ring 2 + 4
- **Dee composed of symmetric sandwich:**
  - Central layer CO2 pipe and Airex foam
  - Module support plates:
  - Thermal: Thermal Pyrolytic Graphite
    - El. Isolation: Aluminium Nitride
    - Dee-PCB with electrical services
  - CFK panel and modules

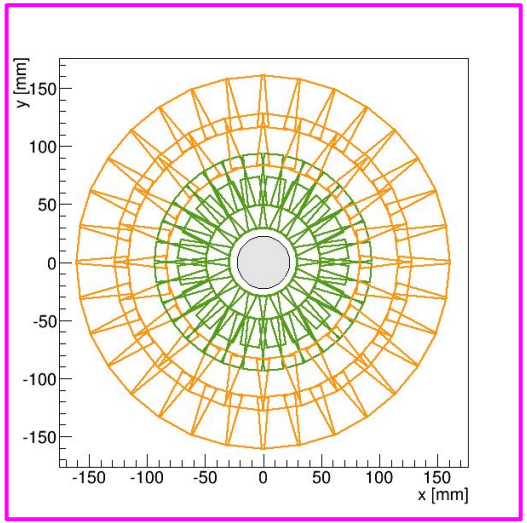
Example of TBPX L3 module thermal modelling

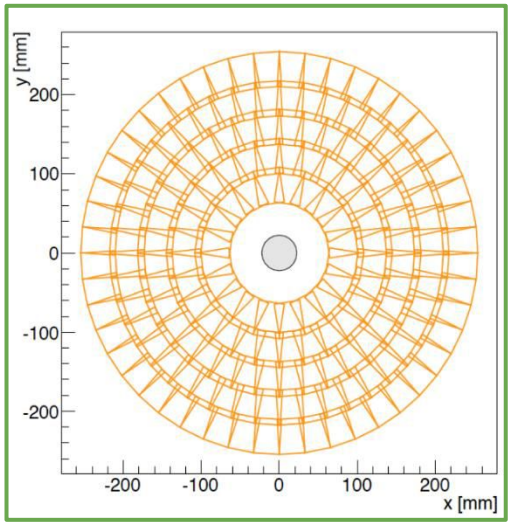


Barrel and Disk Layout









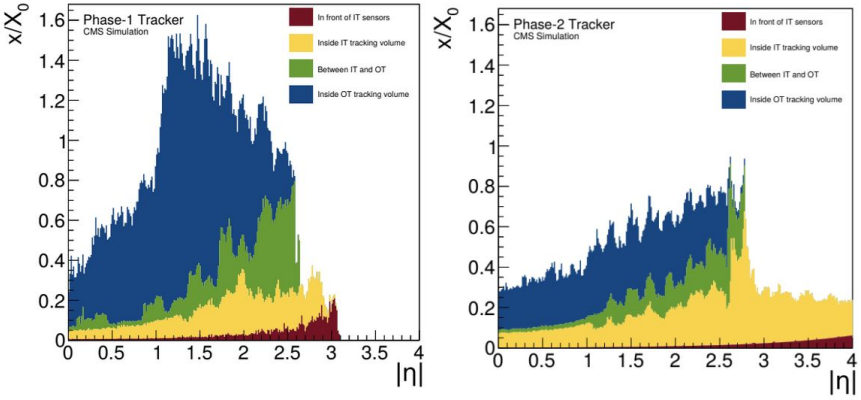
TBPX:
- 4 layers
- 4/5 modules per ladder

TFPX:
- 8 disks per side
- 4 rings per disk

TEPX:
- 4 disks/end
- 5 rings/disk

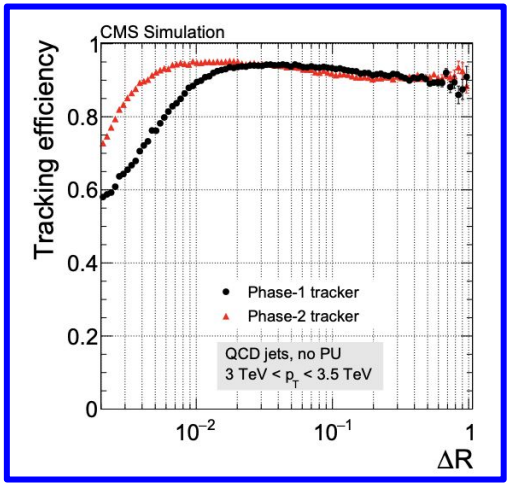
Expected Performance

Reduced Material budget

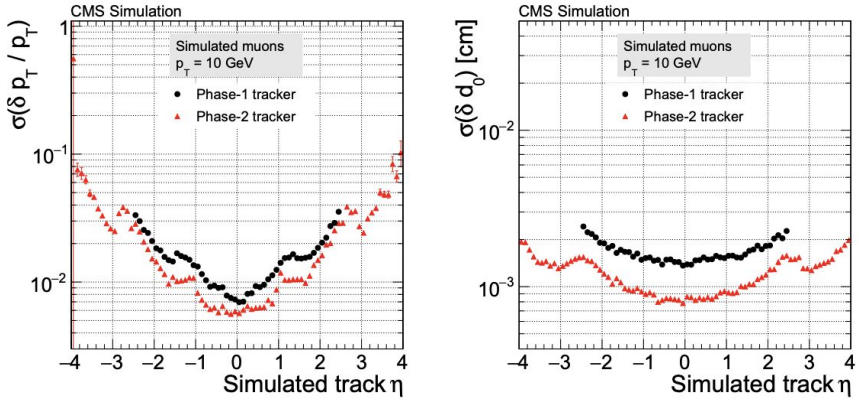


- Comparable mass to CMS Phase 1 Inner Tracker
- Robust tracking in high pile-up environment
- Improved pT and impact parameter resolution

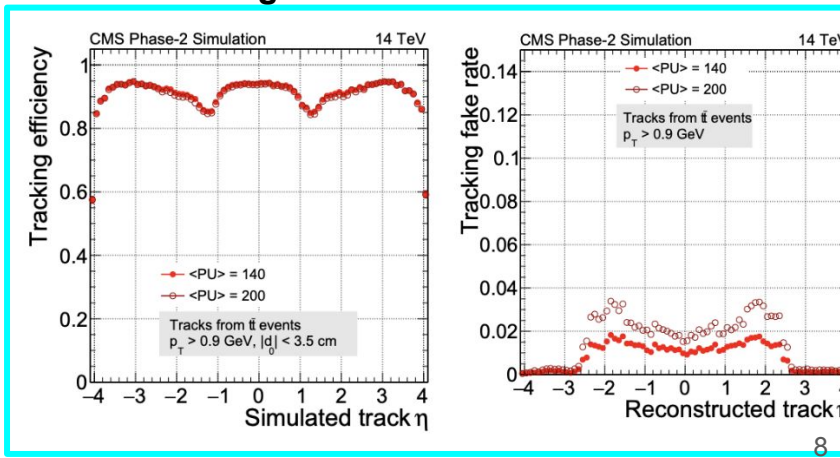
Improved efficiency



Improved Resolution

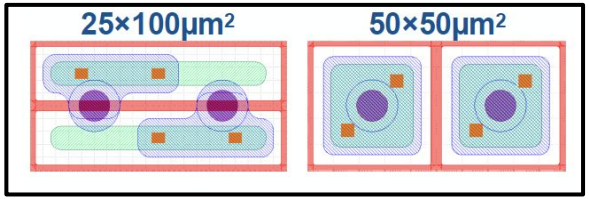


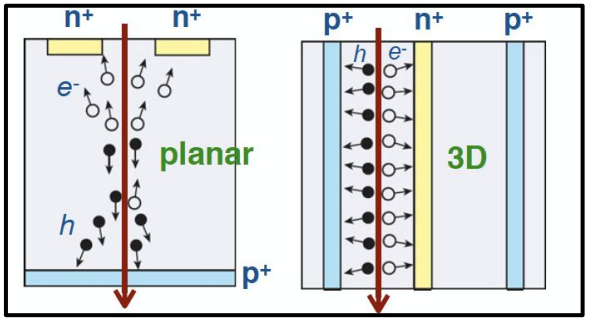
Robust Tracking Performance

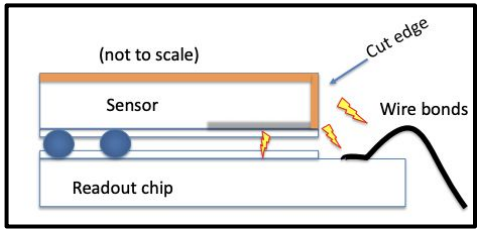


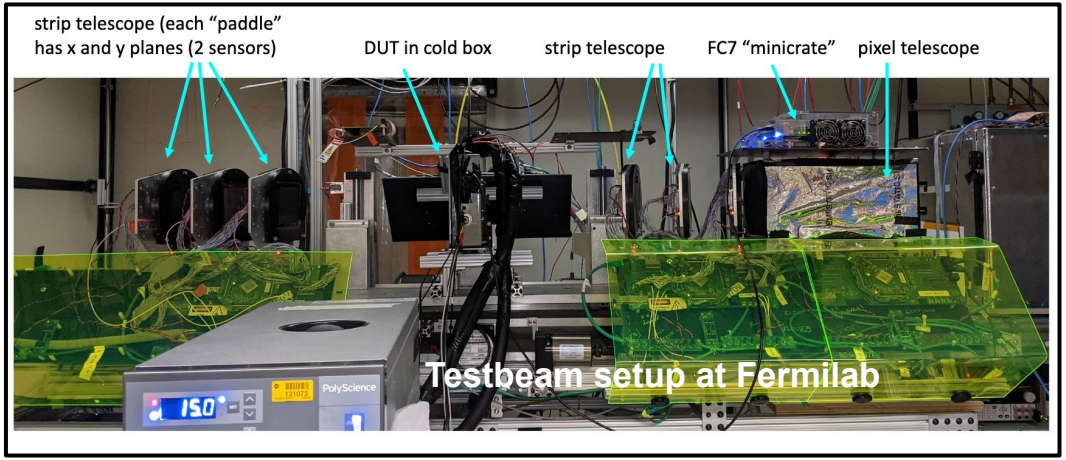
Sensors (silicon, pixels)

- Thin sensors for radiation tolerance (150 μm)
- Signal / threshold > 3 at $\Phi_{eq} \approx 8x10^{15}$ cm^{-2}
- Reduce pixel size (factor of six) to mitigate track density
  - 25x100 or 50x50 μm^2
- Thin planar n-in-p sensors:
  - 150 μm in thickness
  - stable charge collection with radiation
  - need higher bias (up to 0.8-1kV) and spark protection between ROC and sensor
- 3D sensors
  - innermost TBPX and TFPX
  - potentially more rad-hard
  - complex fabrication and larger cell capacitance
- Planar and 3D sensors investigation and characterisation ongoing in test beam

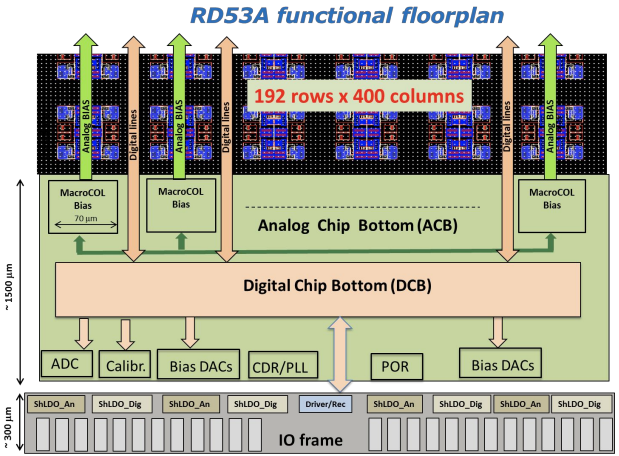




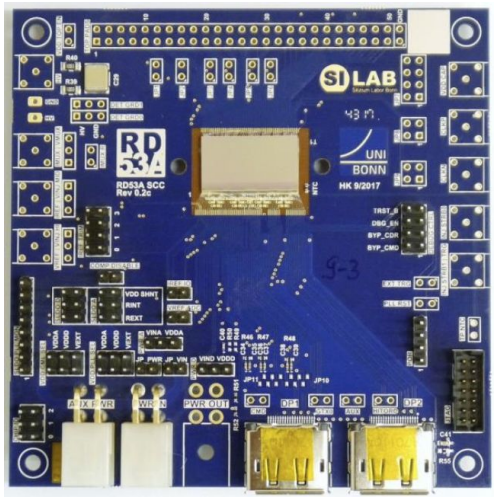




Readout Chip



- Developed by RD53 Collaboration
- For ATLAS & CMS inner tracker
- 65 nm CMOS technology
- Designed to be radiation hard up to 500 Mrad



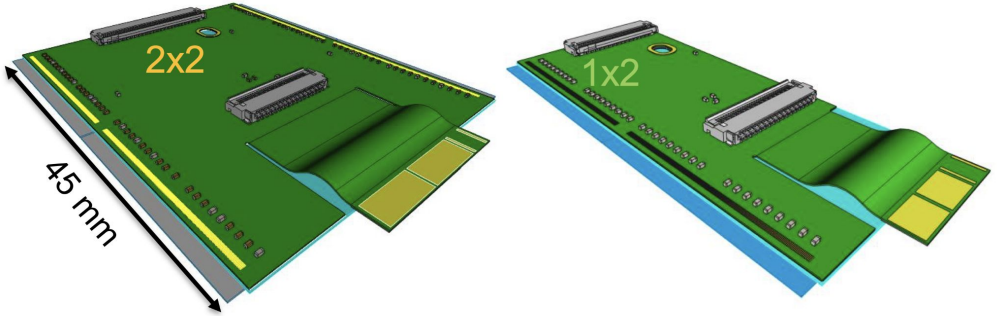
RD53 chip features:

- 50 x 50 µm^2 (25 x 100 µm^2) cell size
- 3 Analog Front-Ends
- Low threshold (~ 1000 e)
- High hit and trigger rate
  - 160 Mbps control & up to 4 x 1.28 Gbps output links
- Support for serial powering scheme
- Chip size (CMS): 16.8 x 21.6 mm^2 (336 x 432 cells).

- RD53A: first prototype (~1/2 size of final chip)
- Technology and design concepts demonstrated, lot of R&D performed
- Radiation hardness tested (up to 500 Mrad)
- Three different analog front end designs tested
- synchronous, differential, linear
- Linear analogue FE was chosen for the CMS chip
- Used in prototype modules at the test beam studies
- RD53B -CROC prototype submission in early 2021
- SEU and irradiation campaign to be repeated due to some bug fixes

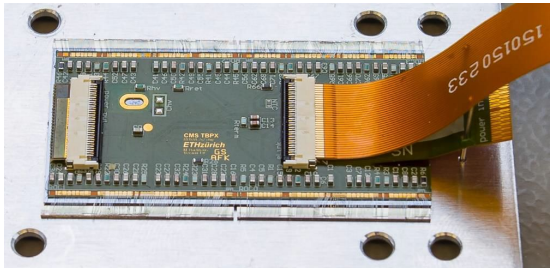
Modules

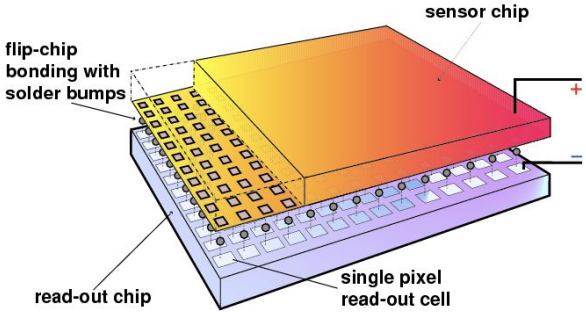
Simple design concept, ROC is the only active electronics on module



Geometry constraints

- TBPX
  - Both faces of barrel ladders loaded with modules
  - no service routing on back-side
  - supply and return directly from module to module
- TFPX and TEPX
  - service routing on “inactive” surface





HDI (High Density Interconnection)

- Flexible PCB containing only passive components (high precision resistors and decoupling capacitors)
- 2 to 4 ROCs per module
- HDI contains return path for supply current
- Careful design for current paths and low material budget
- HV capable up to 1000 V

Modules

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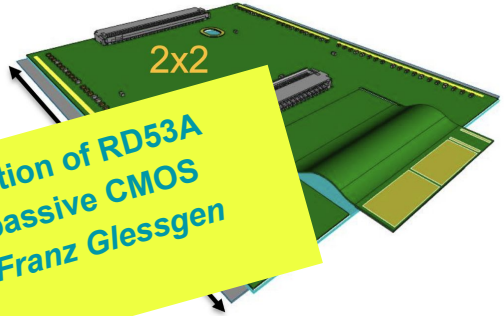

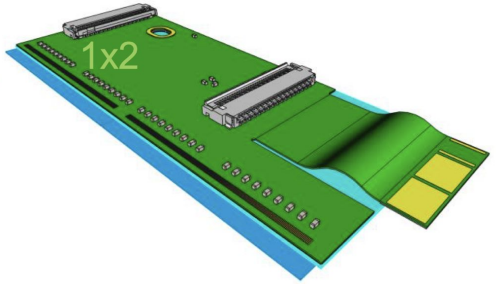

Poster - Characterization of RD53A pixel modules with passive CMOS sensors, Speaker - Franz Glessgen (ETH Zurich (CH))

Geometry constraints

- TBPX
  - Both faces of barrel ladders [illegible]ded with modules
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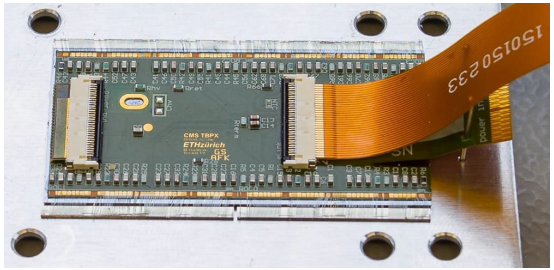

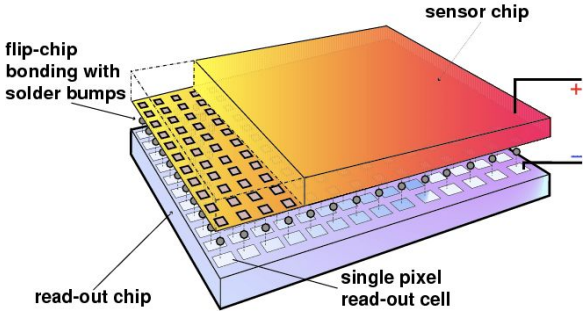

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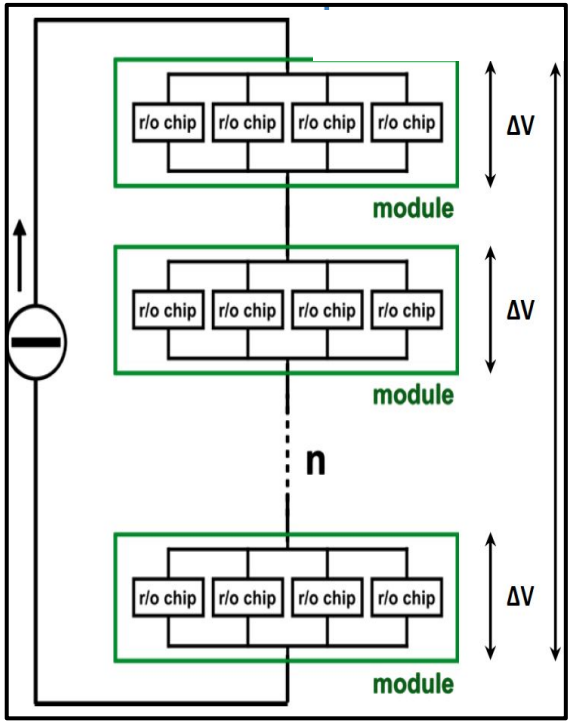
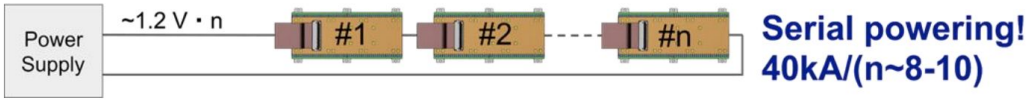
Power Architecture

Challenge

- Higher granularity, long latency → increased power consumption
- CMOS process for RD53
  - Small Features
  - low supply voltages, high input currents
- 100 m long supply lines → higher voltage drop
  - No parallel powering → increase of cable mass
- **Modules will be powered in serial chains**
  - **First time in HEP**
  - ROCs share constant input current
  - generate the necessary operational voltage





All the elements in a chain see the same current (by construction) while the voltage is equally shared if all elements represent the very same and constant load

Power requirements

- Serial power: 55 kW
- HV power: 2.5 kW
- Optoelectronics: 2.3 kW
- Pre-heaters: 3.7 kW
- Total: 63.5 kW

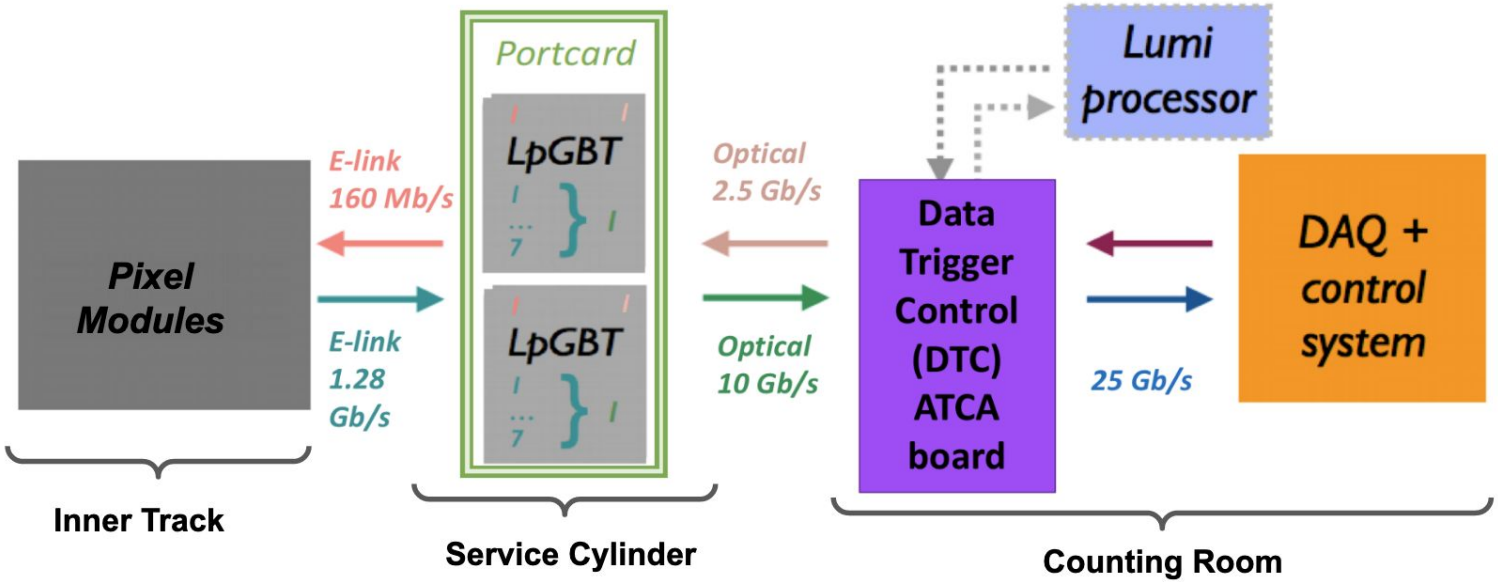
Power Distribution

- Up to 12 modules connected in one serial chain
- Low voltage power is distributed to inner tracker modules according to a serial powering scheme (~500 chains)
- High voltage bias is distributed in parallel to modules in each serial chain
- Optoelectronic services (LpGBT and VTRx):
  - Detached from the modules
  - Hosted on dedicated boards: portcards (~ 700)
  - Positioned around IT support cylinder (TBPX) and on “Dee” structures (TFPX, TEPX)
  - Powered making use of on-board DC/DC converters
- Pre-heaters (~ 350) needed by cooling system

Readout Scheme

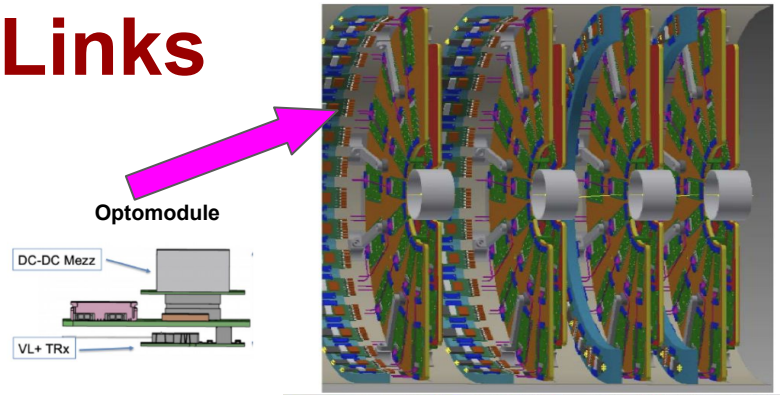
- High Bandwidth Readout chain
- Up to 6 electrical up-links @1.28 Gb/s per module to LpGBT
  - Efficient data formatting to reduce data rates (factor ~2)
- One electrical down-link @160 Mb/s per module from LpGBT
  - Clock, trigger, commands, configuration data to modules

- 28 DTC (Data, Trigger, Control) boards required for CMS IT
- Dedicated boards & crate(s) for TEPX LUMI/BKGD measurement

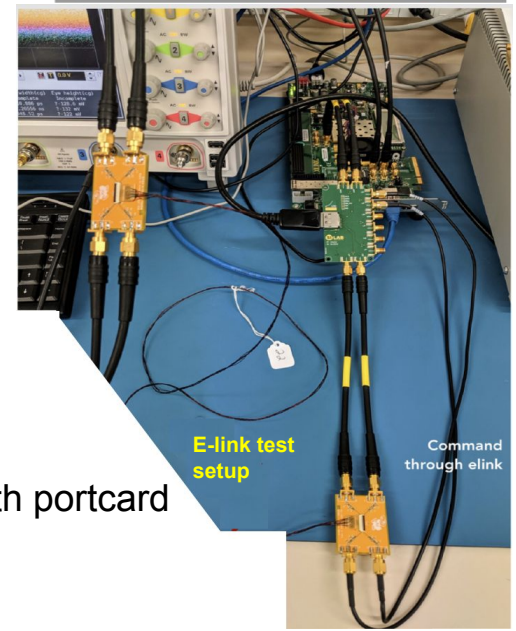


Optomodules and Low Mass Links

- Pixel modules connect via electrical links to optoelectronic service card (**optomodule aka portcard**)
  - Positioned around IT support cylinder (TBPX) and on “Dee” structures (TFPX, TEPX)
  - 2x LpGBTs and 2x VTRx+ links, powered via cascaded DC-DC converters
  - Up to 6 e-links at 1.28Gb/s per LpGBT (AC-coupled)
  - Limited to $5x10^{16}$ neq/cm^2 fluence, 100 Mrad
  - ~750 portcards to readout/control the IT



- ~7k readout + 4k control **differential electrical links** (e-links)
  - AC- coupled e-links due to serial powered modules
  - Various e-link options investigated with simulations and tests:
  - Flex and twisted pair: 0.1 – 1.6m
  - Objective: Minimize mass for acceptable cable losses
  - Studying: Pre-emphasis, Cross coupling, Eye-diagrams, first operation with portcard and twisted pair elinks occured 2019



Summary

- The upgraded CMS Tracker is an extremely challenging and ambitious project to take data with a higher pile-up and radiation environment at the HL-LHC

- The IT has been designed to:
  - Cope with higher radiation level and pile-up (higher granularity, larger bandwidth)
  - Extend forward coverage (|n|= 4), decreased material budget

- The IT has extended layout including luminosity measurement

- Entering Prototype phase

- Electronics:
  - Radiation hard ROC
  - Demonstrator RD53A chip working, used for sensor R&D
  - Preparing for the final CMS pixel chip submission
  - New DTC board, opto-boards and e-links development

- Sensor R&D:
  - Intense R&D program, rapidly progressing since availability of RD53A chips
  - Investigating thin planar sensors and 3D sensors for inner layer/ring, pixel aspect ratio

- Modules:
  - Very first prototypes produced, several test beam program on going (e.g. Fermilab, DESY)
  - Novel methods: Serial powering, CO^2 cooling, light structures, easy installation