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The LHCb Upstream Tracker data flow architecture

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The current LHCb Tracker Turicensis is being upgraded to gain spatial resolution, accommodate higher occupancy and use a trigger-less data flow. The enhanced detector is called the Upstream Tracker (UT). A core part of the UT electronics is the SALT ASIC: a device tailored to the task with several transmission modes to optimize the number of differential pairs. This optimizes copper traces inside the detector acceptance. The different data transmission modes, together with the different granularity and expected data rates, will produce a variety of situations that the data flow architecture has to cope with. This contribution focuses on the UT's unique electronics and data processing architecture, how the readout adapts to the multiple scenarios that such tracking system imposes. It discusses the tradeoffs that had to be made so that the output data format is as homogeneous as possible across the different areas and how it tries to maintain a reasonable VHDL hardware implementation.

TIPP2020 abstract resubmission?

No, this is an entirely new submission.

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