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Readout system and testbeam results of the RD50 MPW2 HV-CMOS pixel chip

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The RD50-CMOS group aims to design and study High Voltage CMOS (HV-CMOS) chips for use in a high radiation environment. Currently, measurements are performed on RD50-MPW2 chip, the second prototype developed by this group.
The active matrix of the prototype consists of 8x8 pixels with analog frontend. Details of the analog frontend and simulations have been already published earlier. Standard tests on passive test-structures have been performed as well and will be briefly mentioned.
This talk focusses on the Caribou based readout system of the active matrix. Each pixel of the active matrix can be readout one after the other. Details on slow-control, configuration settings and a setup for use in testbeams are given. Relevant aspects of hardware, firmware and software are introduced, always focusing on the operation of the chip in combination with a tracking telescope to measure efficiency and residuals.

TIPP2020 abstract resubmission?

No, this is an entirely new submission.

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