

System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC

Wednesday 26 May 2021 07:30 (18 minutes)

For the High-Luminosity Large Hadron Collider era, the trigger and data acquisition system of the Compact Muon Solenoid experiment will be entirely replaced. Novel design choices have been explored, including ATCA prototyping platforms with SoC controllers and newly available interconnect technologies with serial optical links with data rates up to 28 Gb/s. Trigger data analysis will be performed through sophisticated algorithms, including widespread use of Machine Learning, in large FPGAs, such as the Xilinx Ultrascale family. The system will process over 50 Tb/s of detector data with an event rate of 750 kHz. The system design and prototyping are described and examples of trigger algorithms reviewed

TIPP2020 abstract resubmission?

Funding information

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Session Classification: Readout: Trigger and DAQ

Track Classification: Readout and Data Processing: Readout: Trigger and DAQ