CALICE SiW ECAL

Development and first beam test results of detection elements using Chip-on-Board Technology

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On behalf of the CALICE Collaboration

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Layer Structure of SiW ECAL

Design: Total space for ASICs and PCB 1.8mm (was 1.2mm since ~2007)
In recent years the CALICE SiW ECAL has developed and used several PCB variants

- ASICs in BGA Package
- Incremental modifications
- From v10 -> v12
  - Main “Working horses” since 2014

FEV10-12

FEV11_COB

ASICs wirebonded in cavities
  - COB = Chip-On-Board
  - Thinner than FEV with BGA

FEV13

Also based on BGA packaging
  - Different routing than FEV10-12
FEV11_COB – Some Technical Details

Bonding scheme

- 177 Bonding wires
- Bonding by CERN Bondlab
- Regular exchange allowed to iron out early shortcomings

Side view

- 9+2 layers board (details of stacking, see back-up)
- Overall height ~1.2mm
- ASICs buried in cavities to ensure overall flatness
  - Need to make sure that bonding wires don’t pass board surface

- ~177 Bonding wires
- Bonding by CERN Bondlab
- Regular exchange allowed to iron out early shortcomings
Impressions FEV_COB

- Produced by EOS Company in South-Korea (supervised by SKKU)
- Height 1.2mm
- Planarity within specs for 80% of the boards
  - Less than 0.5mm bending after production
  - Planarity important for wafers gluing
  - Boards well rectangular
- First beam test in Summer 2019 (after many years of development)
COB as part of compact readout system

Current detector interface card (SL Board) connected to COB

Complete readout system

- “Dead space free” granular calorimeters put tight demands on compactness
- Current developments in CALICE meet these requirements
- Can be applied/adapted wherever compactness is mandatory
- Components will/did already go through scrutiny phase in beam tests
  - More details on compact readout system, see poster by J. Maalmi on Thursday
• Devices under test:
  – 5 FEV13 fully equipped with 4 Si wafers each. All of
    650um except one slab with 320um. Interface card SMBv5
    with the old Detector Interface Card.
  – 2 COB boards with one wafer each (500um) SL-Board
  – 2 FEV12 boards with one wafer each (500um) and the
    new SL-Board.
  – All boards equipped with SKIROC2a ASIC

• First week: 5 FEV13 (BGA) and 1 COB and
  1 FEV12 (BGA).

• Second week: full setup with 9 slabs
• FEV13s are in Power pulsed mode,
• COB and FEV12 still in continuous mode.
• Data taking w/ and w/o tungsten
  – Here all results w/o tungsten
First MIPs in COB

- Very first beam MIPs seen with a COB (after very short debugging)
  - Details on commissioning see backup

- 2 boards synchronization
- Clean signal w/o any extra component
- Coincidences between two COB Boards

- The setup and in particular the COB had an excellent start at the beam test
Adding capacitances to the COB

BGA-type PCB feature decoupling capacitances

In first place COB do not feature decoupling capacitances

• FEV12/11/13 At least two cap (120 and 150uF) per chip

COB with 4x150uF capacitances between analogue power supply and ground.
Performance at MIP Level I

- **RE-TRIGGERS** (Many triggers in “unnaturally” short time interval (compared with beam frequency):
  - Before adding the capas. Lots of retriggers in the nearby of the SLBoard !!
  - After adding the capas, we have a maximum of 80 retriggers over 3500 good hits, in the beam spot! So they may not even be retriggers, but just rejected good signals.

  - Adding the capacitances improve performance of COB
  - Note that, especially after adding the capacitances the retrigger levels of COB vs FEV11 vs FEV13 are of the same order → improvable but not competing with the signal.
Pedestal analysis

Distribution of pedestal widths

... and as a function of buffer depth
(remember ROC Chips have a buffer to store evens during spill/bunch train)

- Pedestals recorded with FEV_COB comparable to BGA version
- Stable throughout buffer depth
Performance at MIP Level II

Details of MIP Calibration see backup

SLB_0, run_32015

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COB-c, better light and em shielding

SLB_2, run_32015

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<tr>
<td>GSigma</td>
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COB-a, extra AVDD dec. capacitances

- Comparable spectrums.
- Few noisy channels in the COB-a (peak at 0)
  - Optimizable
- Capacitance “beats” light tightness
Track/Event reconstruction

SL-Board based readout only (FEV_COB, FEV12_BGA)

32014 (MIPs, 3 GeV, only SLB in the reconstruction)

- Clean MIP tracks reconstructed
- Detailed analysis of efficiencies ongoing

Track finding by internship student J. Marchioro
Common events and “Particle separation”

- Signals in all nine layers (FEV12, FEV_COB, FEV13)
- Reconstruction of common events
- Here, two electrons cross the detector, one as track the second starts to shower
- Clear particle separation
Encapsulation of ASICs

ASICs on Chip-on-Board version of PCB need to be protected

- Catastrophy during encapsulation with GlobTop at private company
  - Curing at 160° over several hours
  - => Deformation of boards, delamination of wafers

- Successful “in house” application of Epoxy (Loctite Hysol) on several boards

- No degradation of performance observed
  - e.g. no ASIC damage, all ASICs fully operational after encapsulation

- Cooperation with Henkel/Loctite on hold due to pandemic
  - No access to French site since October
  - Plan is still to produce boards encapsulated at home and at Henkel/Loctite
  - NDA ready on CNRS side (thanks to services at IJCLab and CNRS-DR4)
Summary and outlook

- **Successful beam test 2019**
  - Smooth operation of readout

- **First systematic study of Chip-on-Board PCB in beam**
  - Flatness good enough for wafers gluing (critical item of R&D)
  - Encouraging results
  - No serious issues discovered
  - Good MIPs w/o additional capacitances
  - Additional capacitances improve performance

- **Still a number of tests to be done**
  - 1 wafer -> 4 wafers
    - Note first attempt delayed after damage during encapsulation process at company
  - Tests with power pulsing
  - Considerable slowdown due to pandemic

- **Towards new design**
  - Integration of stabilising capacitances
  - Discussions with EOS (Korea) interrupted due to pandemic
Backup
Details of MIP Calibration

- Pedestal subtraction
- **MIP spectrum integrating all cells** in ASIC 2 (SLB systems) or ASIC 13 (FEV13 systems)
  - FEV11 TB2017:
    - 320um, MIP at ~ 63ADC
  - If 500um → MIP is expected at 98ADC
    - Is the ASIC hold value well optimized? To be checked in the laboratory.
    - The gain is correct, i.e. 1.2pF?
  - If Ped_width ~ 3.2 ADC (previous slides) → S/N ~ 24.5
Details on commissioning - 1st week

- FEV13Jp system had the leading role.
  - Several interventions to reset DIF or check connectors.
- SLboard slabs entered in the stack on wednesday (during machine works)
  - 1 COB + 1 FEV12
- Debugging and commissioning (find noisy channels + thresholds) done at a moderated gain, 3.6pF instead of 1.2pF since the noise levels are still high due to the “fresh glue” and the short time with HV on.

- Very first beam MIPs seen with a COB (after very sort debugging)

- 2 boards synchronization
Details on commissioning - 2\textsuperscript{nd} week

- All four SLB-slabs in the box, together with the FEV13Jp.
- One day of commissioning/debugging/single-cell-calibration with the “standard” gain, 1.2pF.
  - Reasonable thresholds set (estimated from previous experiences to be around ~0.5 MIP but not measured)
  - 2-8% per chip of masked channels... as in 2017 (FEV11).
  - Channel 37... only noisy in the FEV12 and FEV13.
• FEV13Jp system had the leading role.
  – Several interventions to reset DIF or check connectors.
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- Very first beam MIPs seen with a COB (after very sort debugging)
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Wafer gluing

• Current aspiration setup of the gluing robot and the current COB version are not fully compatible
  – in fact, the FEV12 also needs some manual work before starting the process
• This was fixed by fabricating a simple aluminum (or even a 3D printed) mask to transport the vacuum from the pipes to the COB.
  – Close collaboration between LAL & LPNHE. Very useful input for the next COB generation.