The CMS High Granularity Calorimeter Scintillator/SiPM Tileboards

Status and Outlook

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Outline

• Introduction
• Scintillator Tileboards in Detail
• Tile Wrapping and Assembly
• Results from the Lab and Testbeam Campaigns.

SiPMs and LEDs, Scintillator Tiles (wrapped and unwrapped) on Tileboard
CMS High Granularity Calorimeter (HGCAL) - Endcaps

- For HL-LHC Phase 2 upgrade, the CMS endcaps will be replaced.
- Electromagnetic calorimeter (CE-E) based on hexagonal silicon sensor modules
- Hadronic calorimeter (CE-H) based on silicon sensor modules and trapezoidal scintillator tileboards.

Detector Properties – per endcap:
- ~230t weight
- ~620m² of Silicon modules (6M channels)
- ~400m² of Scintillator Modules (~3700 boards, 240k channels).
- CE-E: 26 (2x13) layers, CE-H: 21 layers
- ~120kW power
- More details: See talk from Thorben Quast (prev. talk)

Focus in this talk: Scintillator Tileboards.
Challenging Requirements to the Tileboard Electronics

- Harsh radiation environment (Scintillator detector)
  - Neutron Flux up to $5 \times 10^{13}$ n/cm²
  - Total ionizing dose (TID) up to 200 krad
- Scintillator detector where radiation levels allow operation of SiPMs.
- Operation at $-30°C$.
- Magnetic fields of up to 4T.
- Long lifetime, at least till 2040 with very restricted access to the inner electronics for repair.

- In radial direction, depending on detector layer:
  - between 2 and 5 ‘trapezoidal’ tileboards build up a basic $10°$ detector unit.
  - with hexagonal silicon modules at the inner part.
- Half-Cassette: $30°$ (three $10°$ units). 6 full cassettes form ring around beampipe.

Neutron fluence - scintillator detector [neq/cm²]. Ramanpreet Singh, NIU
Scintillator Tileboards with SiPMs, LEDs and Tiles on top are mounted on copper heatsink (-30°C).
All other active components are on the backside in cutouts of the copper heatsink.
Polyimide isolation foil (50µm) under tileboards, FR4 protective cover (200µm) on top.
Twinax cable + power wires as only connection to the tileboard.
Scintillator and silicon modules installed in common (mixed) cassettes.
Scintillator Tileboard – Component Side

- 8 major geometries, ranging from 21x15cm² to 45x42cm².
- 64 channels typically (48min, 96 max).
- Analogue/Digital ASIC HGCROC (SiPM version):
  - Readout the SiPMs
  - 30fC..300pC signal charge, adjustable gain
  - 6x 1.28GBit/s data outputs
  - 10b-ADC for small signal charges
  - 12b time-over-threshold (TOT) for large signal charges
  - 10b time-of-arrival (TOA) for timing measurements
  - HGCROC details, see talk from Damien Thienpond on Friday.
- Power and Slow Control:
  - 2x bPOL12: DC/DC converters
  - 2x ALDOv2: lin. regulator for SiPM Bias voltage and LV
  - new ASIC design: 2x LDO for HGCROC supply
  - 1x GBT_SCA: Slow control
- Active components grouped together – cutout in heatsink.
Scintillator Tileboard – SiPM/Tile Side

- Typically 64 SiPMs.
- Individually wrapped plastic scintillator tiles.
  - 3mm thick
  - Trapezoidal shape
  - 21 different sizes in detector
  - different materials and production techniques under study
- LED system with one LED per SiPM for calibration.
- The tileboards are in prototyping phase.
  - Final SiPMs and components (HGCRO Cv3, LDOs, DC/DCs) expected 2nd half of this year.
  - Tiles and –wrapping procedure in final optimization.
- Example from tileboard tests: SiPM Test-PCBs: Connect irradiated SiPMs or other SiPM types to tileboards.
Tile Wrapping

- Automatic wrapping station for the 21 different tile sizes between 23x23mm² and 55x55mm².
- Update: Translational moves for better position reproducibility.
- Air-pressure induced wrapping operations with valve-control by programmable unit.
- Ion gun to overcome static friction of reflector foils: 17kV observed.
- Not shown: Interlock for safety.

- 3-4 tiles per minute for wrapping aimed.
- ~240000 tiles required - Two tile wrapping centers foreseen: NIU + DESY.
Tile Assembly

• Standard Pick&Place station for tile assembly.
• Glue dispensing (Araldit) with special dispenser head. Amount of glue and different shapes of glue deposit under test.
• Tile assembly onto the tileboards and 24h glue curing at room temperature in metal frame to keep tiles in place.
• Aimed assembly rate: Up to 20 tileboards per day.
• Followed by: QC of fully assembled Tilemodules.
• Two assembly centers foreseen: NIU + DESY.
Results from Testbench / Testbeam

- Tileboards have been tested extensively in the lab for ~1 year.
- Four 1-week tileboard testing periods at the 3GeV-electron testbeam facility at DESY in 2020 and 2021.
- A tileboard is in operation at Fermilab (FNAL), including a test period at the FNAL 120GeV proton test beam facility.
- Intermediate DAQs realized based on commercial FPGA boards (KCU105, Trenz Zynq-based MPSoC) by our collaboration partners.
- DAQ asynchronous to testbeam:
  - Trigger generation by two external trigger scintillators.
  - Pulse reconstruction by recording 6 consecutive samples in 25ns distances.
**Noise**

**Detection Limit (Scintillator Electronics)**

- Noise (pedestal RMS) performance depends on:
  - Gain setting (low gain: red / high-gain: black dots)
  - connected capacitance at the HGCROC inputs.
- Noise analysis of the tileboard electronics shows a noise < 2 ADC counts for the aimed smaller SiPMs of 2mm² and 4mm² sizes (III and IV).
- In physics data taking and low gain (red dots), the noise is around 1.2 ADC counts.
- Good S/N in physics operation expected.

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**Detection Limit (Scintillator Electronics)**

![Graph showing noise analysis](image)

- SiPMs off
- Noise (pedestal RMS)
  - Gain-Conv=4
  - Gain-Conv=12

**aimed type of SiPMs**

- I: SiPM 9mm², 10μm pitch, C=530pF
- II: SiPM 4mm², 10μm pitch, C=240pF
- III: SiPM 4mm², 15μm pitch, C=240pF
- IV: SiPM 2mm², 15μm pitch, C=115pF
- V: unconnected channels
- VI: no SiPMs assembled
SiPMs and Single Pixel Spectra (SPS)

Smallest Signals to be measured

• Dedicated LED system with one UV-LED per channel. Pulse shape as short as possible, similar to a particle in scintillator.
• Calibration of all channels and full chain (SiPM+HGROC ASIC) by excitation of single pixels of the SiPMs at low light intensities (single-pixel spectra, SPS). Peak distances in SPS are a measure of the overall channel gain.
• Gain monitoring from repetitive SPS measurements, e.g. twice a day: Correct for gain changes by bias-voltage-, temperature-drifts and irradiation.
• Possible candidates for SiPMs with properties:
  • Gain=\(3.5 \times 10^5\) @4V overvoltage. Vbd<40V (typ.)
  • 2mm\(^2\) (~ 8500 pixels)
  • 4mm\(^2\) (~ 17500 pixels)
• Good S/N of SPS for 4V overvoltage (SiPMs) for all channels.
Dynamic Range

Largest Signals to be measured

• From Physics: Up to 300pC signal charge expected. HGCROC with low gain (Gain-conv]<=4) in physics data-taking.

• Large signals currently tested with charge injection.

• 10-bit ADC for small signals, 12-bit Time-over Threshold (TOT) for large signal charges. 10-bit Time-of-Arrival (TOA) provides timing information.

• Some non-linearity/saturation in TOT at larger signal charges, partly seen in TOT simulation as well, but electronics is suitable for required signal charge range.

• MIP spread due to tile- and SiPM sizes, scintillator type (cast/molded): ~0.3 – 3 pC at 2V overvoltage (SiPMs).

• Good resolution and S/N expected also for smallest signals (MIPs) from physics.
Results from Testbeams / Irradiation

• Results from successful 120GeV proton (@FNAL) and 3GeV electron (@DESY) testbeam campaigns, work in progress!

• Irradiation can cause complex changes of component’s characteristics, e.g. for the SiPMs (mainly from neutrons):
  • Increase of noise / dark-count rate up to few GHz => higher leakage current of up to 1mA per channel to be compensated by electronics. SiPMs do not show SPS any more for calibration.
  • Self heating from increased leakage current => increase of breakdown voltage from temperature and irradiation. Compensation required.
  • Dedicated tests of irradiated SiPMs after 2*10^12 neq/cm² at room temperature, equivalent to 5*10^13 neq/cm² @ -30°C.
  • Electronics effects to be reduced by -30°C operating temperature.
  • Reduction of SiPM bias voltage under test, e.g. 2V overvoltage.
  • First preliminary results, also for irradiated SiPMs promising!
Scintillator Tiles / Lightyield

Results from DESY 3GeV electron testbeam

- **Aim:** S/N for MIPs >5 at the end of the experiment’s lifetime for all channels, including radiation damage.
- **Critical areas:** Inner radii of detector with high irradiation levels; higher noise from SiPMs, reduced light yield from scintillator tiles.
- **Compensation for irradiation effects:**
  - Larger SiPMs (4mm² instead 2mm²): Factor ~2 in light yield.
  - Cast instead of molded scintillator tiles. Higher cost but twice as large light-yield.
- **Benefit:** In areas of higher irradiation levels, the smaller tiles (inner radii) with higher light yield are located.
- **Finally in detector:** 240k plastic scintillator tiles
  - 21 sizes: 23x23mm² to 55x55mm², trapezoidal shape
  - individually wrapped in reflector foil.
Conclusion and Outlook

• The electrical and mechanical concepts for the CMS HGCAL scintillator tileboards are well advanced.

• Results from lab and testbeam are promising and fulfil requirements.

• Final components (SiPMs, bPOL12, LDOs) to be integrated this year.

• Procedures for series production in final preparation.

• First tests from electron and proton testbeams, also with irradiated SiPMs promising.

• Next: Thermal tests at -30°C. New thermal chamber available, also for QC of series production.
Backup Slides
Mixed cassettes – Scintillator part (10° and 30° segmentation)

- In radial direction, depending on detector layer:
  - between 2 and 5 ‘trapezoidal’ tileboards build up a basic 10° detector unit.
  - with hexagonal silicon modules at the inner part.
- Half-Cassette: 30° (three 10° units). 6 full cassettes form ring around beampipe.
- Tileboards connect with twinaxial cables (322MBit/s, 1.28GBit/s) and power wires to the wingboards and motherboards below.
- Tileboards next to wingboards with direct (flexlead) connection.
- One VTRx (optical in/out) per 10° to motherboards.
- Wingboards distribute power and signals (10°).
Tileboards – Setup, Power, Ground

- Single connection via one connector to/from tileboard for signals and power.
- Two DC/DC converter form LV input, controlled externally (on/off).
- Linear regulators for the HGCROC and SiPM supply.
- LED system amplitude from external DC voltage.
- Tileboard’s GND can be connected to copper heatsink below (ground reference).
Tileboards – Layer Structure

- 8-layers, ~1.3mm thick
- Halogen-free (CERN requirement)
- IPC-A-610 class 3 aimed.
- Dedicated power-gnd system, analogue (SiPM) and fast digital signals on different layers

- HGCROCv2 in 0.6mm-pitch BGA requires use of micro- and buried vias. Known-good setup.
- In order to relax requirements for PCBs, there will be HGCROCs in 0.8mm BGAs. Performance to be tested.
- For 0.8mm BGAs, no micro- and buried vias required any more – reduced PCB costs.
Scintillator detector – Layer Overview