The CMS MIP Timing Detector

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Precision timing for HL-LHC

- HL-LHC will reach pileup of approximately 200 simultaneous interactions!
- Precision timing can help maintain detector performance

- CMS MIP Timing Detector (MTD): timestamp every track with 30 ps resolution at beginning of HL-LHC, up to 50 ps resolution after 4000 fb⁻¹
MTD impact on physics performance

- Substantial reduction in pileup mis-association
  - Improved isolation, tagging efficiency, MET resolution...
- Particle ID for heavy ion/B-physics
- Enhanced sensitivity to BSM long-lived particles

Heavy ion physics: Hadron ID from TOF

No timing
35 ps timing
Sensors for Endcap Timing Layer

- CMS Endcap: high occupancy & radiation
  → Highly granular silicon detector
- Low-Gain Avalanche detectors (LGADs): novel ultra-fast silicon detectors
  - Moderate internal gain (10-20)
  - Thin (50 micron depletion region)
- ETL: (1.3 mm)$^2$ pads, (2.1 cm)$^2$ sensors
LGAD sensor characterization

- Leverage diverse set of characterization facilities
  1. Fermilab test beam (120 GeV protons): highly detailed information; limited sensor statistics

Fermilab test beam facility with Si tracker & dedicated LGAD test stand

Good signal uniformity across 4x4 LGAD array
LGAD sensor characterization

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  2. Beta source: high volume testing with MIP signal

Deep understanding of dozens of sensors with beta source

Beta source: MIP signal available 365 days a year!
LGAD sensor characterization

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Detailed validation of beta source results with beam data.

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  3. Probe station CV: wafer-scale uniformity studies

Probe measurements for sensors across wafer

Accurately predict MIP response from probe station

Easily characterize wafer uniformity: essential for QA/QC

More results in arXiv 2104.08369
LGAD sensor characterization

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Accurately predict MIP response from probe station
LGAD radiation tolerance

- Increase bias voltage to maintain gain after irradiation
- Radiation tolerance in latest prototypes: keep 40 ps resolution to end of life.
ETROC ASIC prototyping

- Timing measurement performed by ETROC ASIC (ToA + ToT correction)
- Preliminary test beam results with LGAD and ETROC1 prototype: $\sigma = 42-46$ ps

Extract single-layer resolution from 3-layer $\Delta T$:

$$\sigma_i = \sqrt{0.5 \cdot (\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2)}$$
ETL modules

- Intense activity in module prototyping & development of assembly procedures

- Mockups for thermal & mechanical testing
- Assembly via jig or gantry
- Bump-bonding prototypes
Endcap Timing Layer

- Attach modules to service hybrids; assemble into D’s
- 2 disks at each endcap: 2 hits per track.
  - Single-hit resolution < 50 ps → track resolution < 35 ps.

ETL 2-disk stack
Endcap Timing Layer

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Barrel Timing Layer (BTL) Overview

- LYSO crystal bars read by SiPMs at both ends
- Tracker/ECAL interface: ~40 mm
- Hermetic coverage for |η| < 1.45. Surface: 38 m², 332k channels
BTL sensor prototypes

- Extensive studies of sensor prototypes using Fermilab test beam
  - Manuscript under review at JINST: arXiv 2104.07786

Single bar with 2x SiPMs

Amplitude response variation across bar

Left-right time difference

Double-ended readout → uniform response along 5.7 cm length
**BTL sensor prototypes**

- Two-channel timestamp: uniform 25 ps resolution

\[ \frac{1}{2} \sigma_{diff}^2 = \frac{1}{2} \sqrt{\sigma_{left}^2 + \sigma_{right}^2} = \sigma_{average} \]

\( \Delta T \) vs 10 ps ref. (MCP):
- Gold standard

Left vs right \( \Delta T \):
- Monitor \( \sigma \) without ext. reference
- Check for correlated noise

Double end readout provides rich set of information.

Many more results in paper: [arXiv 2104.07786](https://arxiv.org/abs/2104.07786)
BTL evolution with fluence

- Photostatistics dominates resolution at beginning of life

- SiPM dark rate becomes significant after irradiation—O(10 GHz)

- Key innovations to fight SiPM DCR:
  - Noise cancellation in ASIC (TOFHIR)
  - Clever thermal management
**Thermal management with TECs**

- BTL cooled by dual-phase CO2 to reach -35°C
- Post-TDR: observe SiPM radiation damage larger than anticipated
- Compensate with thermoelectric coolers (TEC): double advantage
  - SiPM operating temp: -35°C → -45°C
  - Reverse operation: anneal at +40°C without heating tracker volume!

**Dark current for -35°C vs -45°C**

- Decreasing temperature from -30°C (-35°C) to -45°C → a factor of 3 (2.1) dark current reduction after annealing. Additional advantage of annealing: dark current temperature coefficient increased from x1.88°C to x2.1°C

**Dark current after +40°C annealing**

- Periodic annealing: reduce noise by x2.5

**TECs (Peltier)**
Thermal management with TECs

- BTL cooled by dual-phase CO2 to reach -35 C
- Thermoelectric coolers (TEC): double advantage
  - SiPM operating temp: -35 C → -45 C
  - Reverse operation: anneal at +40 C during shutdowns.

![](TECs_Peltier.png)

- Phononic custom TECs of 3x4x0.9 mm
- Through via's design
- Resistors to simulate SiPM load
- TECs (Peltier)
- MTD
- TECs are now part of the baseline (*)
- BTL with TECs recover the TDR performance

Additional studies on the performance impact on physics benchmarks in progress; we prioritized the identification of a design that achieves the TDR performance goal

Note:
- Performance with TECs is similar for the two SiPMs versions (reduction of the cost risk)
- Critical areas identified: no show-stoppers emerged and associated risks manageable
- Full validation of the performance plot and of the operation scenarios in Summer/Fall 2021

Performance summary:
- TOFHIR2B simulation for nominal LYSO pulses
- DCR and PDE from SiPMs annealing/cooling studies (2020 prototypes)
- Operation: $T = -45^\circ C$
- Annealing: $T = +40^\circ C$
- Range spans plausible annealing cycles and power budget assumptions
- Technical stops

(*) CMS TDR change review passed on March 26

- Maintain $\sigma < 60$ ps at end of life.
- Provides operating margin.
**BTL modules**

Detector module (two arrays)

SiPM and LYSO array

TECs

**TEC: Bi$_2$Te$_3$ – 3x4 mm$^2$ x 0.9 mm**

Detector module: side view

- FE board (DC ground)
- Module housing (hearth ground)
- LYSO bars
- Flex cable
- 1.5 mm Spacers
- M2 threaded inserts
- Soft spacers

SiPM array backside

Cooling plate

Concentrator and power card

Part of a joint tender process for HGCAL, ECAL, ETL and BTL

Additional requirement for TEC powering: polarity reversal

Powering will follow choices for BTL LV powering

Cooling/annealing compatible with Tracker operation and power budget

Bias distribution: 8 arrays in series x 6 strings in parallel per RU

MTD

Four TECs on the backside of the SiPM arrays

Shorter LYSO bars (~0.9 mm on each side)

Critical thermal interface between copper housing and TECs

SiPMs arrays and RU proto2 boards forward compatible with TECs

8 TECs implementation

**Update on TECs/SiPMs**
BTL sensor market survey

- Massive campaigns to characterize LYSO and SiPM arrays from several vendors
- Sensor properties well understood: proceed towards procurement!

Automated LYSO scanner with Na22 source

Scan 100s of sensors w/ high reproducibility; practice QA/QC
Measure light yield, $\sigma_t$, etc. Study pre/post irradiation.

SiPM characterization setup

Cold box allows testing 12 arrays at once
Assess vendor capability for high-volume, uniform production
Summary

• CMS MTD on track to be first-of-its kind hermetic timing detector

• Mature design established through extensive prototyping and testing

• Key system tests forthcoming

• Transition towards procurements and high-volume production