Single Event Effects Testing of the RD53B chip

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On behalf of the RD53 collaboration

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Outline

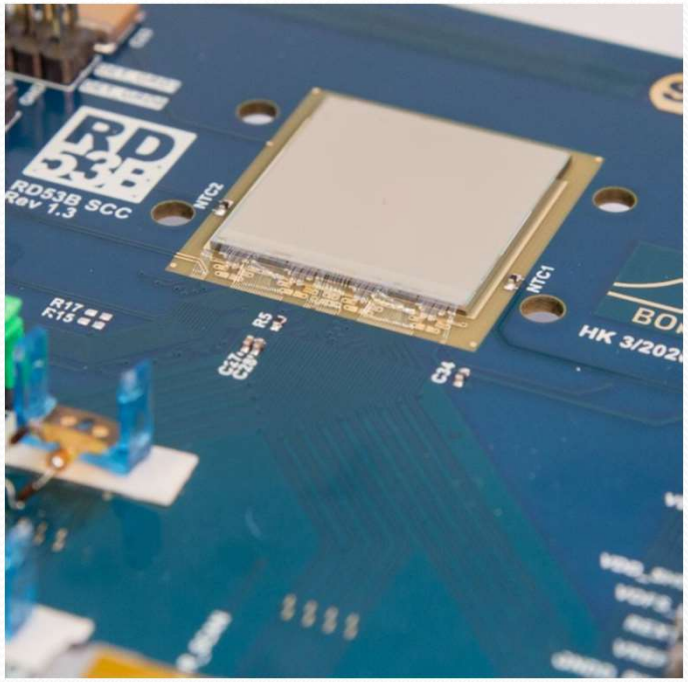
- Introduction : RD53 collaboration
- SEU mitigation strategy in the RD53B chip
- RD53B Heavy Ions Testing
- RD53B Proton Testing
- Results analysis
- Summary and Conclusion

Introduction : RD53 collaboration

See Flavio Loddo talk in this conference: RD53 pixel chips for the ATLAS and CMS Phase-2 upgrades at HL-LHC
https://indico.cern.ch/event/981823/contributions/4295328/

- 24 collaborating institutes
- Design and develop pixel chips for **ATLAS/CMS phase 2 upgrades**
- Extremely challenging requirements for HL-LHC
  - Small pixels: 50 × 50 µm²
  - Large chips : ~2cm × 2cm
  - Hit rates: up to 3 GHz/cm²
  - Data readout : up to 5.12 Gbps per FE chip
  - **Radiation : 500 Mrad and 10^{16} 1MeV neq/cm² over 5 years**
  - Serial powering
- **Baseline technology : 65nm CMOS**
- RD53A : Large scale demonstrator
  - Tested in an intense way
- RD53B chip :
  - **ATLAS chip (ITkPixV1)** submitted March 2020 and received June 2020
  - **High digital current because of an issue in the ToT latches**
  - **All the tested functionalities are working as expected**
  - The issue was solved by a patch in metal layers : ITkPixV1.1
  - CMS chip (CROC) will be submitted soon

RD53B chip

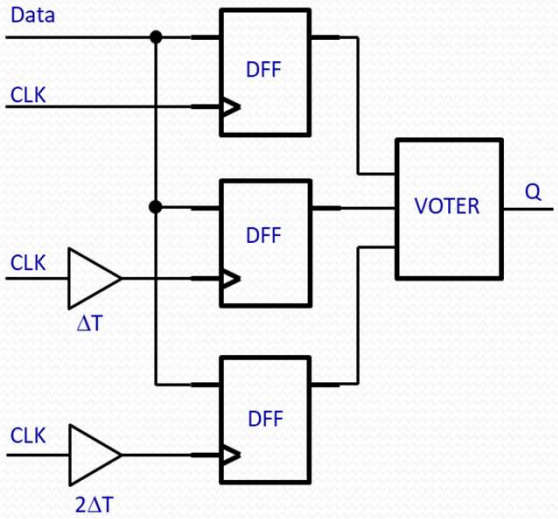


- **The test results presented were obtained from the ITkPixV1 chip**
- A strict procedure was followed to keep the current at an acceptable level (< 3A)
- **Voltage, current and temperature were monitored during all the tests**

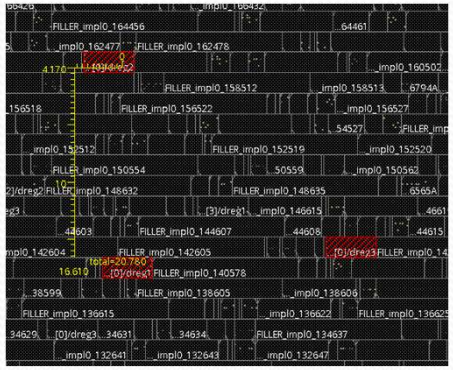
SEU mitigation in the RD53B chip

- **Single Event Effects (SEE)** are a major challenge for the RD53B chip design:
  - Should work reliably in an extremely hostile radiation environment
- Single Event Upset (**SEU**), Single Event Transient (**SET**), Single event latch-up (**SEL**)

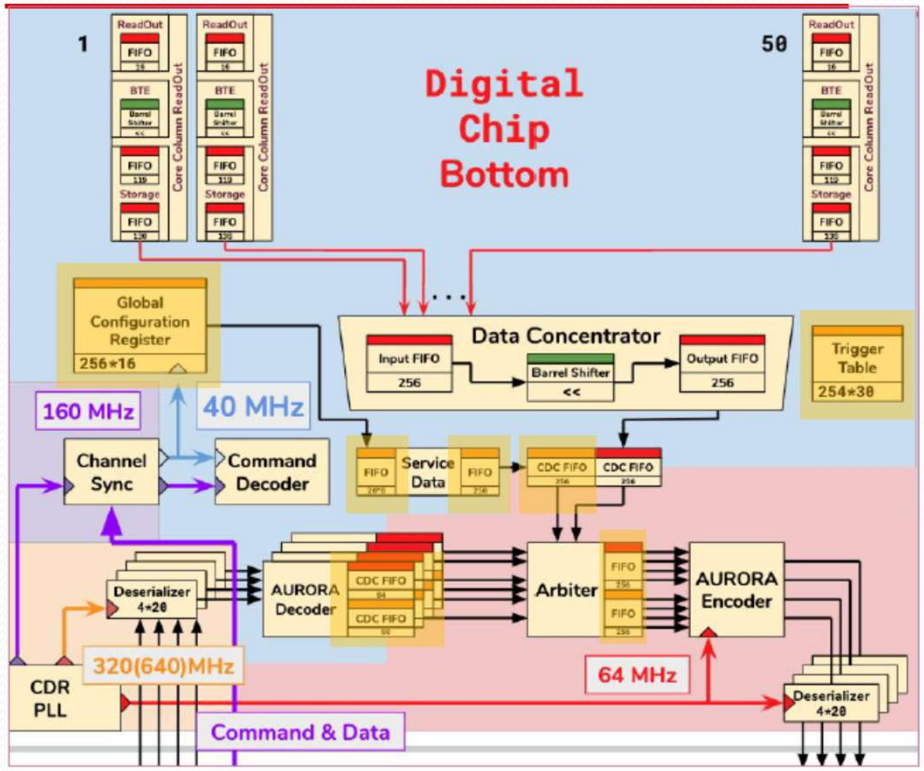
- **Triple Modular Redundancy** (TMR) associated to the **SET mitigation with clock spread** is used in the **Digital Chip Bottom** to reduce the SEU rate in the RD53B
  - Area and power consumption increase
  - Not compatible with the required small pixel size and the power dissipation constraints
- **Mitigation of SEU** concerns only **the critical parts** as the configuration memories, state machines, FiFo pointers …
- Data Paths are not protected
- **50% of the DFFs** in the chip bottom are protected
- All the reset signals are synchronous (avoid a global glitch effects)
- **TMR is implemented during synthesis**
  - Simple FF replacement with TMR version
  - TMR flip-flops are constrained to be placed with **15 µm distance**



TMR+SET mitigation with clock spread



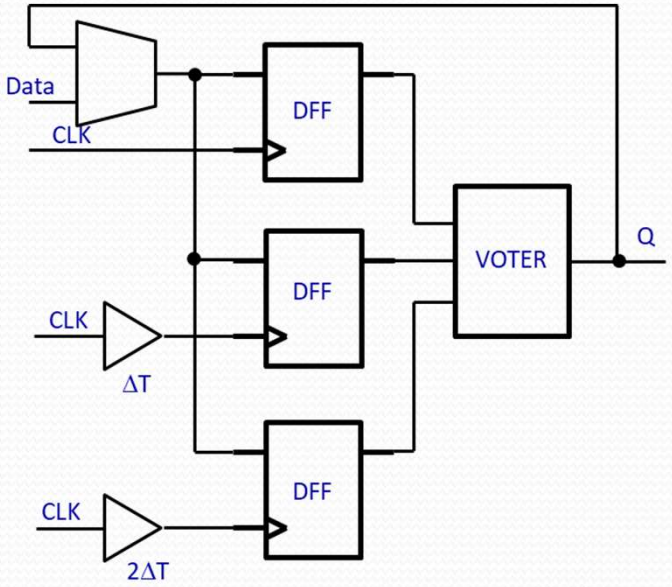
Cells Spacing in the same TMR latch



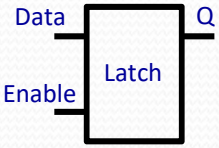
SEU mitigation in the RD53B chip

Chip Configuration

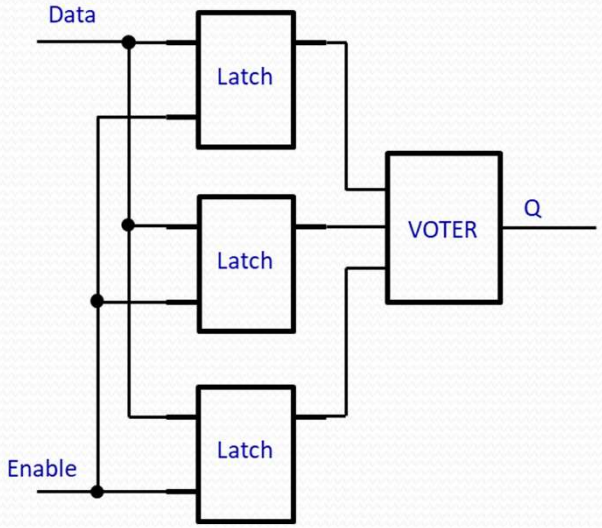
- **Pixel configuration**
  - Memory size : **8 bits per pixel** -> 1.28 Mbit per FE chip
  - **Unprotected latch (single latch)** used for 2 bits
  - **TMR latch without error** correction implemented for 6 bits
  - The small pixel area does not allow to implement the auto correction
- **Global configuration**
  - Memory size : 1.6 Kbit
  - Located in the Digital Chip Bottom
  - **TMR with clock skew and error correction**
- The configuration registers (global and pixel) do not have a reset
  - A re-configuration step is necessary to put them in a right state



TMR with correction



Unprotected single latch



TMR latch without correction

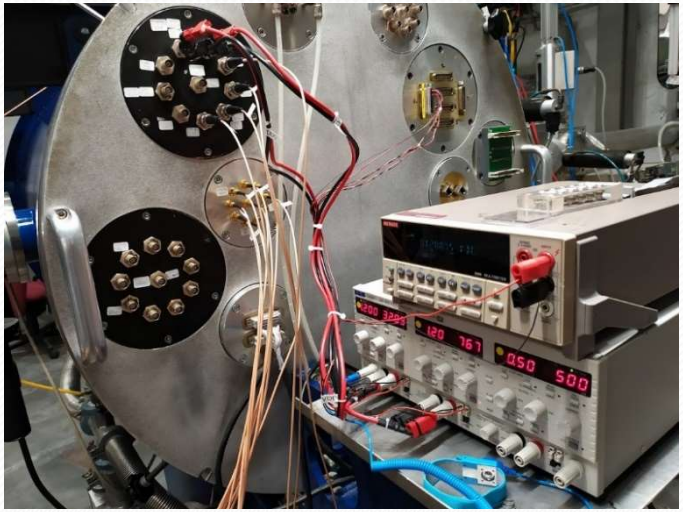
TMR with clock skew

- **ΔT is set to 200 ps**
- Filter SET glitches **shorter than 200 ps**
- **Implementation Challenges** :
  - Triplicated clock skews made by clock tree synthesis
  - Timing closure (hold time)
  - Delay variation with process, power supply, temperature and TID

RD53 Heavy Ion Test Results

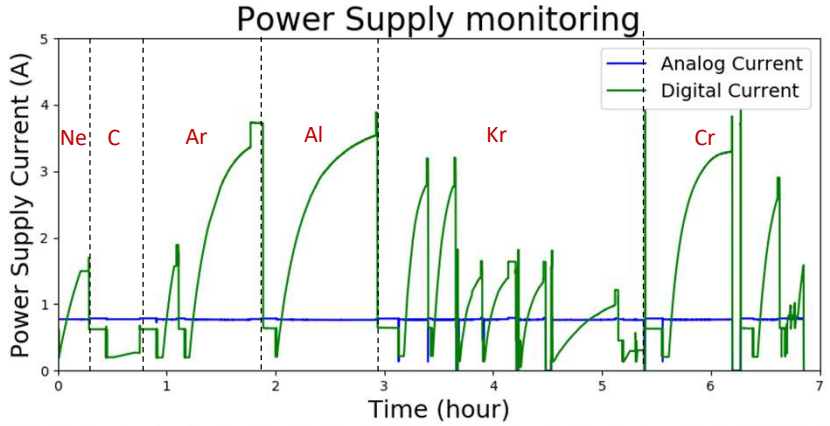
Heavy Ions SEU Tests

- **Centre de Ressources du Cyclotron (CRC) – Louvain la Neuve** , Belgium : https://uclouvain.be/en/research-institutes/irmp/crc
- Two SEU test beam campaigns: October 8, 2020 and November 17, 2020
- Test Setup based on the BDAQ test set-up developed by Bonn Univ.
- The chip irradiated in vacuum
  - the chip was mounted on an Aluminum plate for cooling
- The beam size is 2.5 cm and adjusted to irradiate the whole chip
- **Main tests performed during the 2 campaigns:**
  - **Digital scan loop and Scan loop without injection**
  - **Test of global and pixel configuration registers**



Wafer ID: 102 - Chip ID: 3A
DNW used for Analog and Digital

Chip ID: 0x12286
DNW used only for Digital

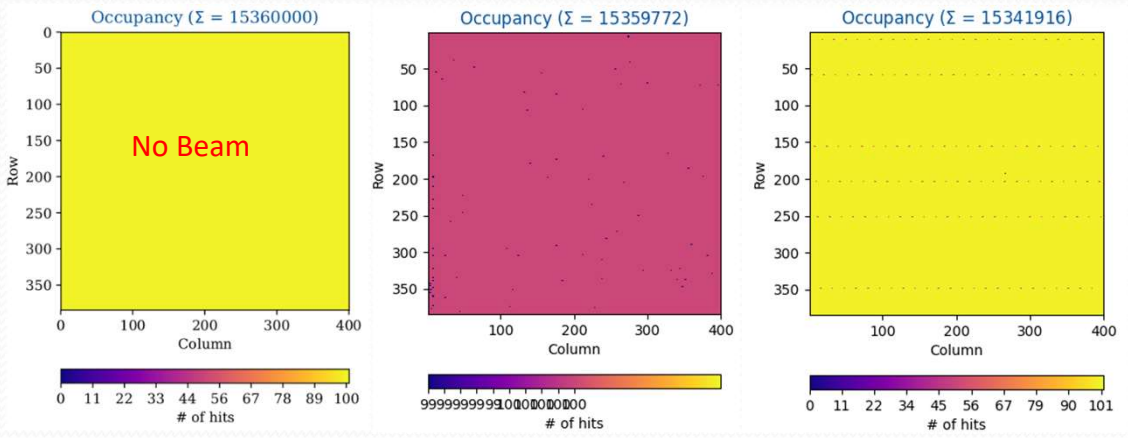


- **Current increase is due to issue in ToT memories in the ITkPixV1 chip**
  - Effect of SEU on the ToT memories
  - The current depends on the LET and on the fluency
- Routines to decrease the current applied after each test
- The current was monitored during the entire test and no SEL effect was observed

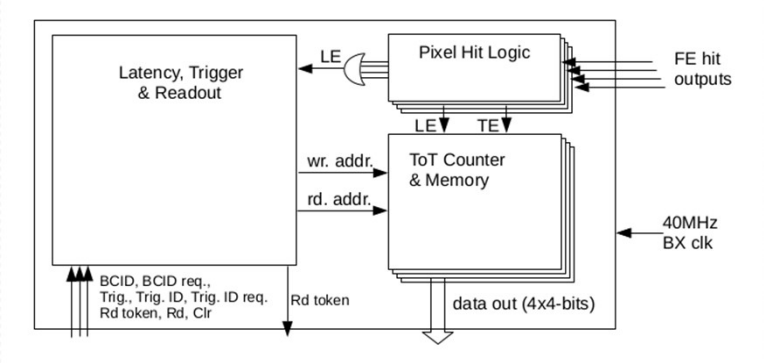
Ion	DUT Energy [MeV]	Range on device [µm Si]	LET [MeV cm² / mg]
13C4+	131	269.3	1.3
22Ne7+	238	202	3.3
27Al8+	250	131.2	5.7
36Ar11+	353	114.0	9.9
53Cr16+	505	114.0	16.1
58Ni18+	582	105.5	20.4
84Kr25+	769	94.2	32.4
103Rh31+	957	87.3	46.1
124Xe35+	995	73.1	62.5

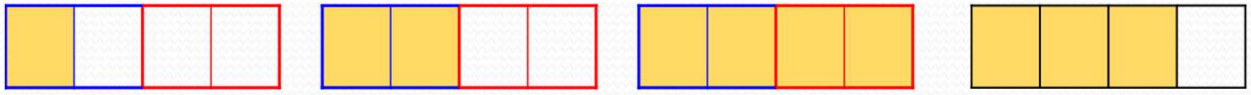
Digital scan

- **Standard procedure of digital scan:**
  - 100 digital injections per pixel
- **For the digital scan test, Individual pixels can show bigger/lower amount of hits**
- This concern **clusters of 4 pixels**
  - It is due to **SEU** in the **digital part of the pixel**
  - This is explained by the **digital architecture organized by regions of 4 pixels**
  - Fired pixels in the same cluster varies between 1 and 4
  - SET or SEU on the common logic to these 4 pixels results as if 1,2,3 or 4 pixels were touched at the same time



More/less hits are received
(100 is injected)





1 SEU affecting individual pixel (Pixel Hit logic)

1 SEU affecting 2 neighboring pixels (LTR block)

2 independent SEUs (LTR block)

This case is not present in any of the scans, but would be counted as 2 SEUs

- Tests were done with:
  - **PLL mode** : serializer and command clocks are provided by on-chip CDR
  - **Bypass mode** : both clocks are provided externally
- In PLL mode, **synchronization issues** with the BDAQ readout system have been identified
  - Map where missing hits are not random
- SEU tests of the **CDR/PLL block** of the RD53B chip are in progress

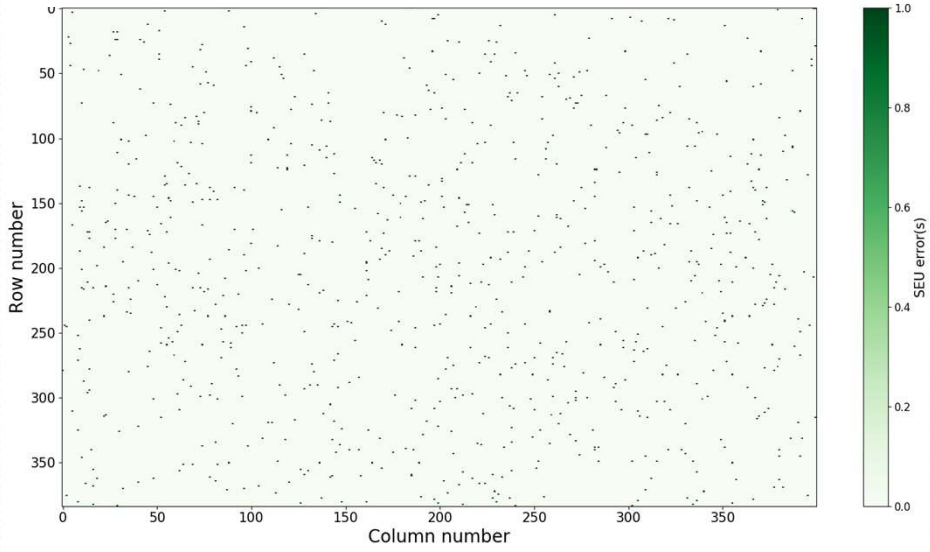
(Injection and readout is always done separately in pixels border with blue and read)

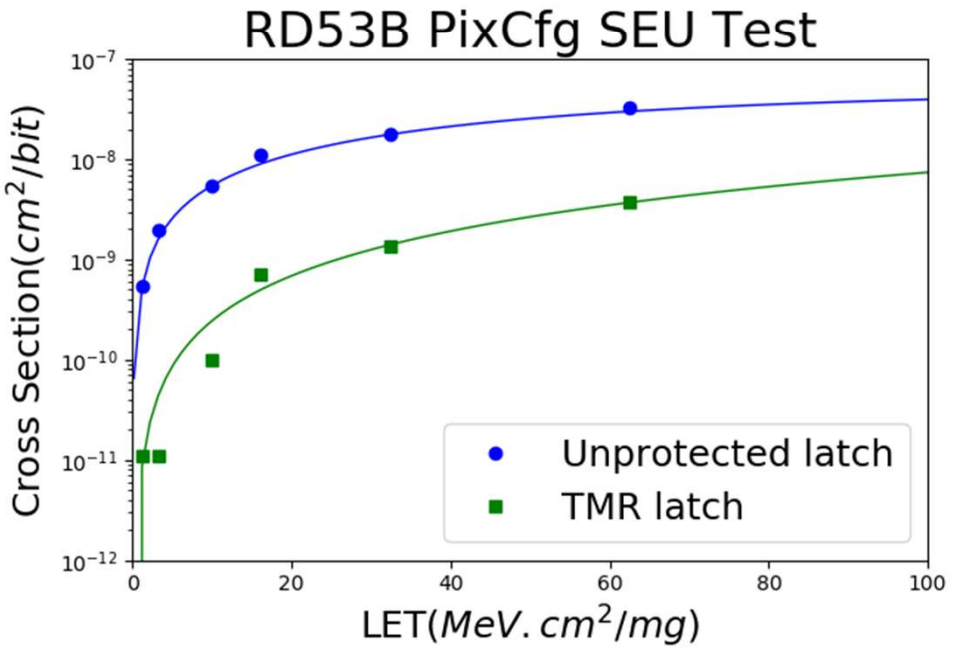
Pixel configuration tests

- Memory size : 8 bits per pixel -> 1.28 Mbit per FE chip
  - TMR without error correction implemented for 6 bits
  - Unprotected latch used for 2 bits
- The SEU errors are **randomly distributed** -> No global signal effects
- Unprotected latch :
  - **Saturation cross section : $\sigma_{SAT} = 6.0 \times 10^{-8}$ cm²**
  - **Threshold LET $LET_{th} < 1$ MeV.cm²/mg**
- TMR latch (no correction)
  - For a particle fluence of **2.0×10^5 p/cm²**, the saturation cross section is improved **by a factor 10**
  - **The TMR w/o correction is very efficient for mitigation** for low error rate
  - The cross section increases with fluence because **of errors accumulation**
- TMR without correction is useful to reduce the rate of configuration when considering a regular external re-configuration

SEU Map for Argon (LET = 9.9 MeV.cm²/mg)

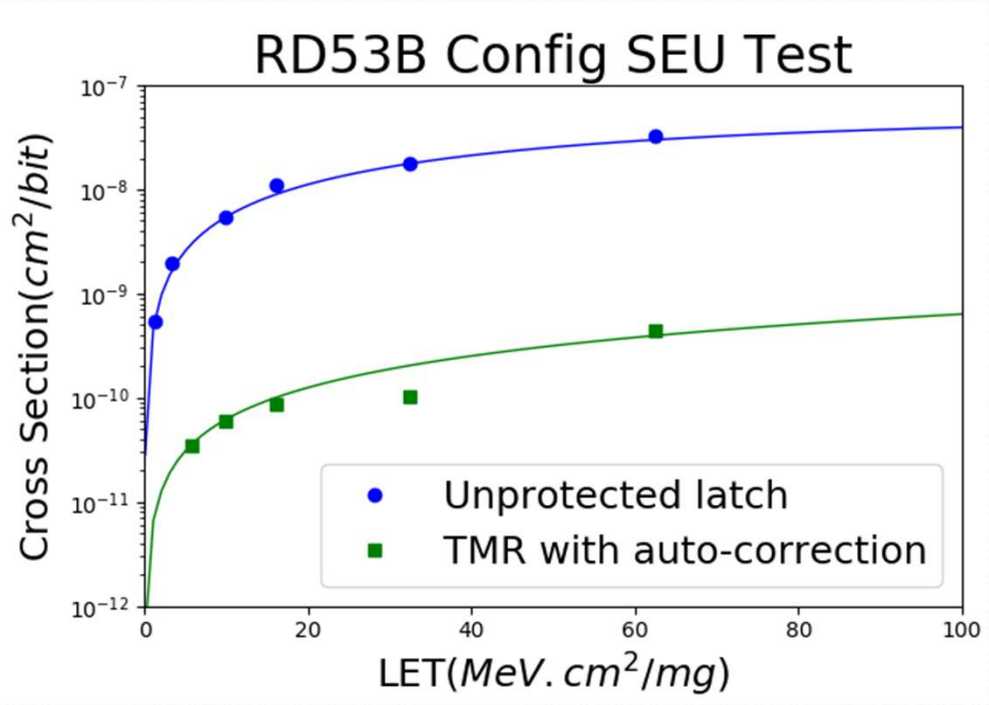
5×10^5 p/cm²





Global configuration test results

- The RD53B chip contains 209 global registers : ~3 Kbit in total where a half is reserved only for tests
  - TMR with correction
- A high ion fluence required for this test, especially for the low LET
  - More than 10^7 p/cm² -> require an exposition time of 1 hour
  - Only a few errors were observed for the low LET (5 errors for Aluminum)
  - The measurement bar error is still high
- **TMR with correction**
  - **Saturation cross section : $\sigma_{SAT} = 9.0 \times 10^{-10}$ cm²**
  - **Threshold LET : $LET_{th} < 1$ MeV.cm²/mg**
- **A ratio $\sigma_{SL}/\sigma_{GR\_TMR}$ of 100 is expected from the proton cross section calculation**
- A significant effect of self-correction was observed by testing the SEU effects with and without clock



	Single latch cross section (cm²)	Global Register cross section (cm²)
calculation for 200 MeV proton based on heavy ion testing	**8.6×10^{-15}**	**7.9×10^{-17}**

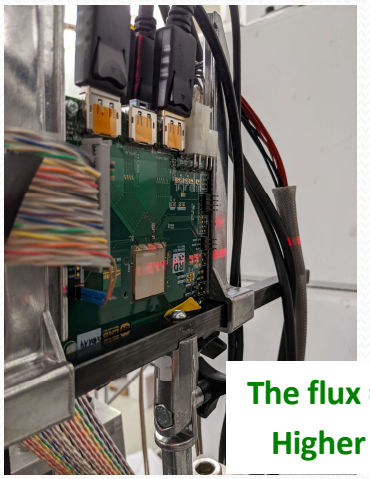
M. Huhtinen, F. Faccio : Computational method to estimate Single Event Upset rates in an accelerator environment

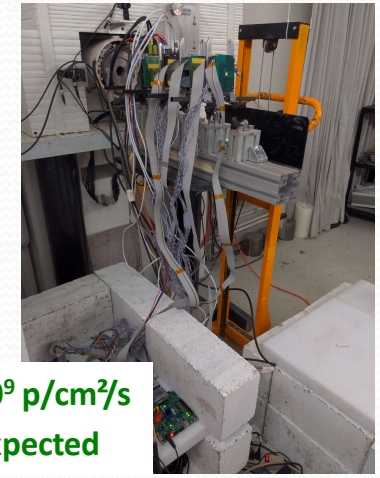
Proton Testing

480 MeV proton SEU Tests

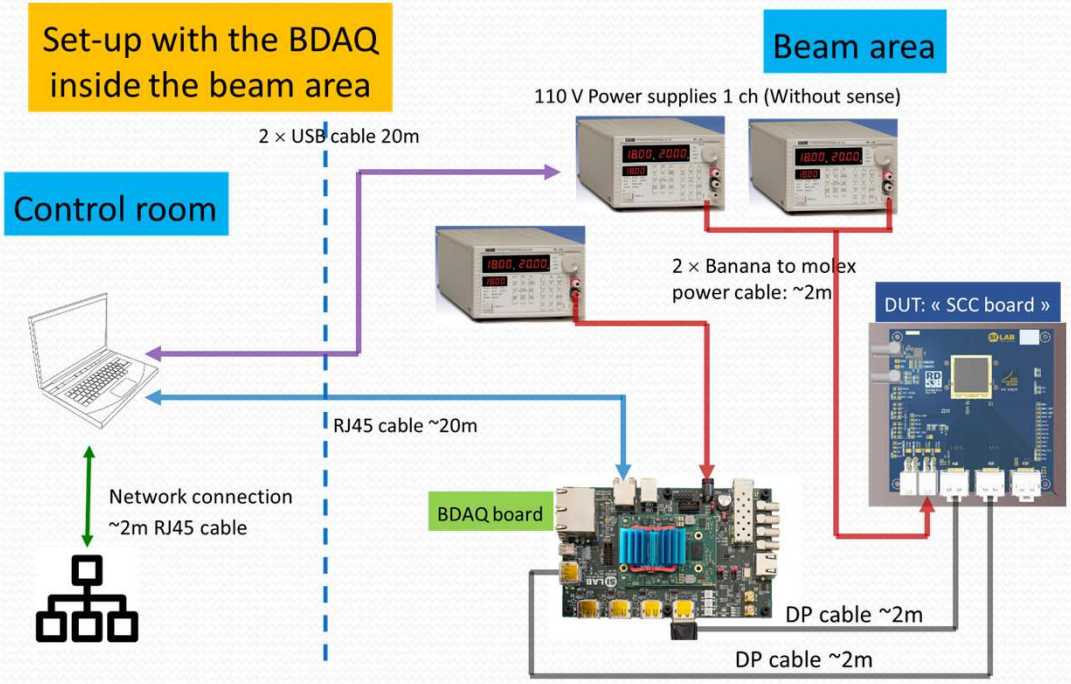
- **SEU tests done remotely** the December 19-20 2020 with **480 MeV protons in TRIUMF** facility
- One set up based on BDAQ was installed -> 1 chip tested
- The whole test set-up installed in the beam area
  - BDAQ board
  - 2 meter of DP cables for connection from BDAQ-SCC board
  - Power supplies controlled by the laptop (control room)
- Laptop controlling the set-up placed in control room, connected to the global network and reached from CERN and from Marseille
- **The chip tested under a proton flux of 1.5 10^9 p/cm²/s**
- The chip powered in LDO mode to ensure good biasing of the chip
  - V_{DDD} and V_{DDA} voltage values monitored trough the on chip ADC
  - The on chip temperature monitored with the internal temperature sensors
- V_{IND} and V_{INA} powered by 2 different power supplies (2 V – 3A)

Thanks to Luise Poely (TRIUMF) for the installation of the set-up and the assistance during tests





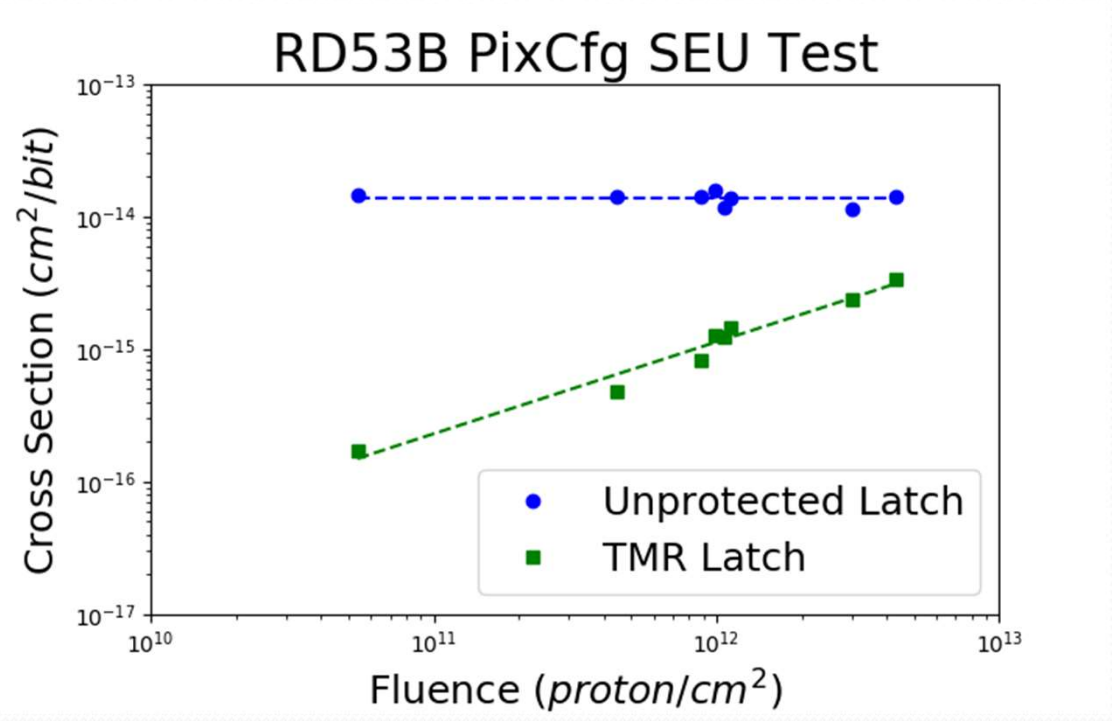
The flux = 1.5 10^9 p/cm²/s
Higher than expected



Pixel configuration test results

- Memory size : 8 bits per pixel -> 1.28 Mbit per FE chip
  - TMR without correction used for 6 bits
  - Unprotected latch used for 2 bits
- **Several pixel configuration runs**
  - The flux set to **the maximum : 1.5 × 10^9 p/cm²/s**
  - 5.4 × 10^{10} p/cm² to 4.3 × 10^{12} p/cm²
- Unprotected latch cross section σ_{SL} = 1.5 × 10^{-14} cm²
- TMR latch cross section increases with the fluence because of errors accumulation
  - **The TMR is 100 times** tolerant than the unprotected latch for low proton fluence (~5 × 10^{10} p/cm²) ,
  - **TMR is only 10 times** tolerant than the unprotected latch for moderate proton fluence (~1.0 × 10^{12} p/cm²)
- TMR without correction is useful when considering a **regular external re-configuration**
  - It helps to reduce the external re-configuration rate

1	2	3	4	5	6	7	8
TMR	STD	STD	TMR	TMR	TMR	TMR	TMR



Pixel configuration results

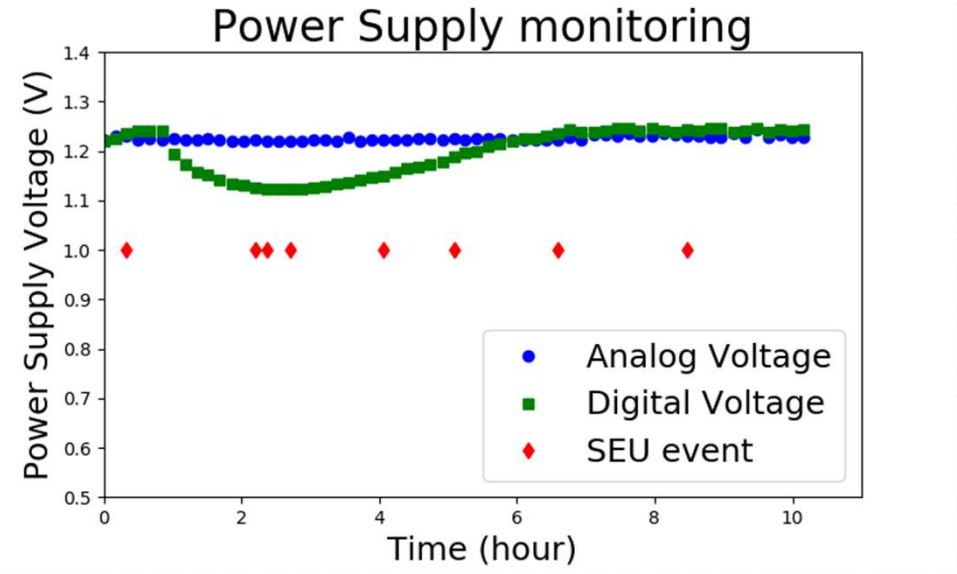
- **HL-LHC environment : SEE flux (Hadrons > 20 MeV) of 1.0 × 10^9 p/cm²/s** is assumed for the innermost layer
- The pixel TMR tolerance depends on **the fluence received** by the FE chip during **the time interval** expected between **2 successive configuration loading** from the DAQ system
- If we assume that each FE chip is re-configured every 50 sec
  - The cross section for unprotected latch is 1.5 × 10^{-14} cm² → Number of bit flips = 7.5 × 10^{-4} (230/307200)
  - The cross section for protected TMR latch = 1.5 10^{-16} cm² → Number of bit flips = 7.5 × 10^{-6} (6.9/921600)
- If we assume that the FE chip is re-configured every 1000 sec
  - The cross section for unprotected latch is 1.5 × 10^{-14} cm² → Number of bit flips = 1.5 × 10^{-2} (4600/307200)
  - The cross section for protected TMR latch = 1.5 × 10^{-15} cm² → Number of bit flips = 1.5 × 10^{-3} (1382/921600)

Layer	Location	R (cm)	Z (cm)	SEE Fluence (cm^{-2}) Hadrons> 20 MeV	SEE Flux ($cm^{-2}.s^{-1}$) Hadrons> 20 MeV	Unprotected latch	Config. Time interval **50 sec**		Config. Time interval **1000 sec**	
							Unpr. latch	TMR latch	Unpr. latch	TMR latch
0	L0 rings	3.6	114	3.26 × 10^{16}	**1.0 × 10^9**	4.6 SEU/sec	**230 flip/FE**	**7 flip/FE**	**4600 flip/FE**	**1400 flip/FE**
2	L2 rings	15.6	286	2.66 × 10^{15}	0.82 × 10^8	0.38 SEU/sec	**19 flip/FE**	**0.075 flip/FE**	**380 flip/FE**	**15 flip/FE**
4	Outer Endcap	274.6	286	1.14 × 10^{15}	0.35 × 10^8	0.16 SEU/sec	**8 flip/FE**	**0.013 flip/FE**	**160 flip/FE**	**2.6 flip/FE**

TMR latch wo correction Conf. Time Interval × 20 → Error rate × 200

Global configuration results

- Long duration global register run
  - Duration : 10h30 , Total fluency : 7.2×10^{13} p/cm²
  - SEU number : 8
- Slow increase of V_{IND} from 1.7 V to 2 V
- The internal V_{DDD} decrease limited to 8% (1.2 V to 1.1V)
- The run Stopped because of a power supply issue
  - Supply was placed inside the beam area
- **The TMR with correction show a gain of ~ 400 regarding the unprotected latch**
- Global Registers seem to be very tolerant to SEU
- Results are compatible with what expected from heavy ion testing



	Unprotected latch cross section (cm²)	Global Register cross section (cm²)
calculation for 200 MeV proton based on heavy ion testing	8.6×10^{-15}	7.9×10^{-17}
Experimental value 480 MeV proton test	**1.5×10^{-14}**	**3.6×10^{-17}**

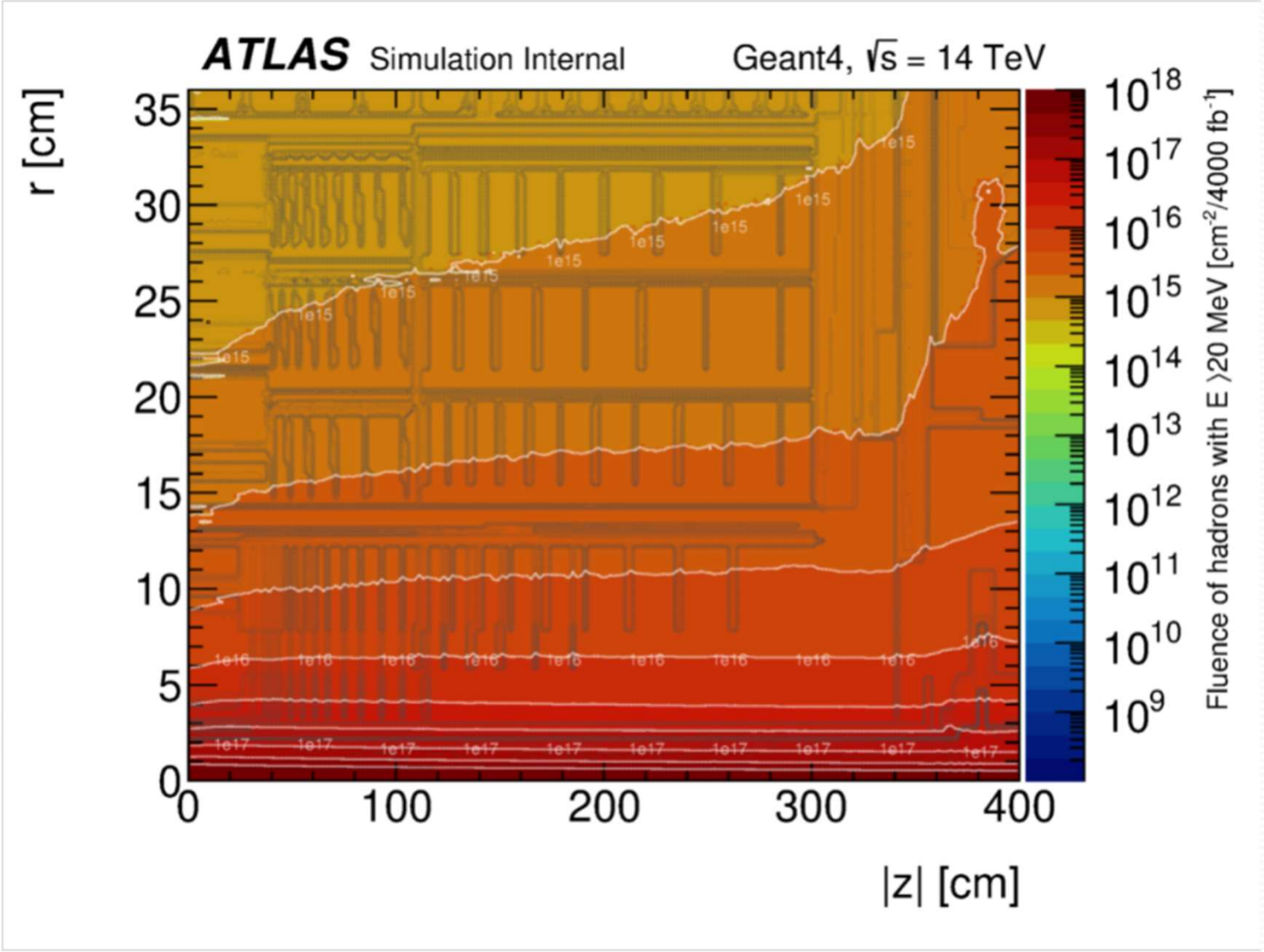
Layer	Location	R (cm)	Z(cm)	SEE-Fluence (cm^{-2}) Hadrons> 20 MeV	SEE-Flux ($cm^{-2}.s^{-1}$) Hadrons> 20 MeV	Pixel configuration Unprotected latch	Global Configuration Mean time between errors (per FE chip)
0	L0 rings	3.6	114	3.26×10^{16}	**1.0×10^{9}**	4.6 SEU/sec	**5 hours**
2	L2 rings	15.6	286	2.66×10^{15}	0.82×10^{8}	0.38 SEU/sec	58 hours
4	Outer Endcap	274.6	286	1.14×10^{15}	0.35×10^{8}	0.16 SEU/sec	138 hours

Summary and Conclusion

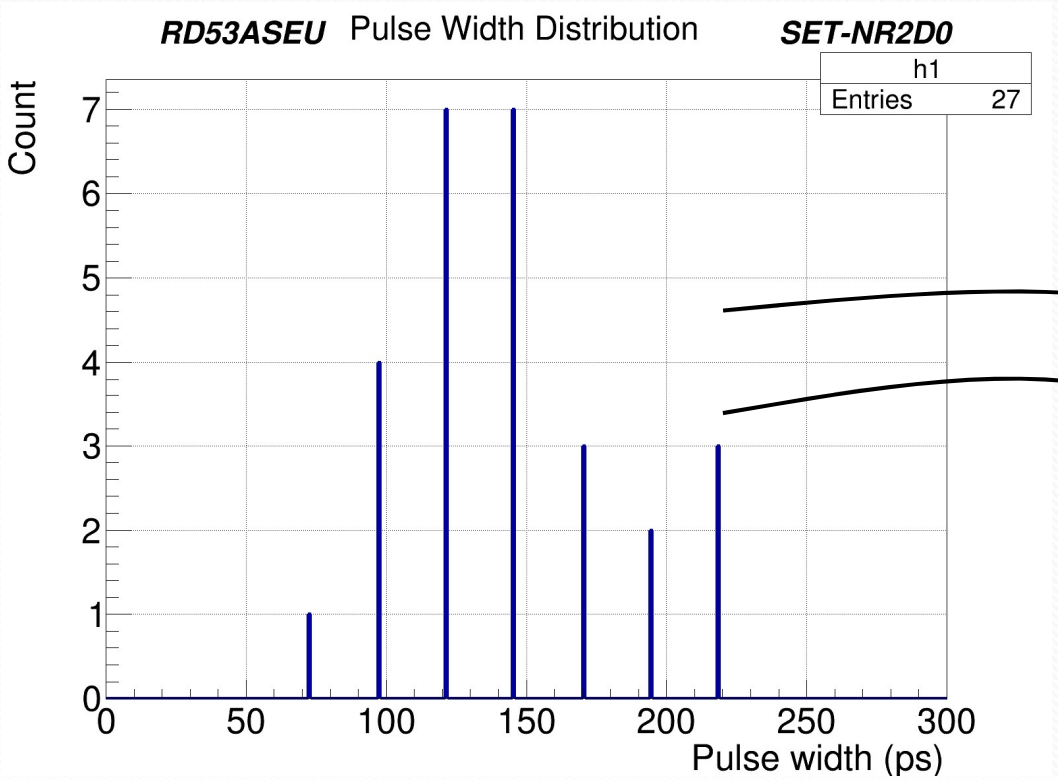
- RD53B chip exposed to a high LET ions and 480 MeV proton beam for SEU qualification
  - 2 chips tested with heavy ions and 1 tested with protons
- The results obtained with protons are in agreement with those obtained with heavy ions
- The chip is working correctly without need of resetting or power cycling
  - No issue observed with the state machines and critical paths
  - No latch-up and no chip-stuck observed during the whole SEU tests
- Configuration
  - The cross section of the unprotected latch is 1.5×10^{-14} cm^2/bit
  - The TMR latch without correction allows a gain of 10 to 100 depending on the configuration rate
  - The TMR latch with correction is 400 times tolerant than the unprotected one
- BDAQ software and firmware modifications needed to avoid the communication issue in PLL mode
- More samples should be tested for more statistics
- Tests in a real working conditions
  - Test for high trigger rate
  - Test for high hit rate
  - Test of the communication and the effect of the CDR/PLL SEU on the whole chip
- Further SEU test campaigns are scheduled for the end of the year

Thank you for your attention
Thank you for your attention

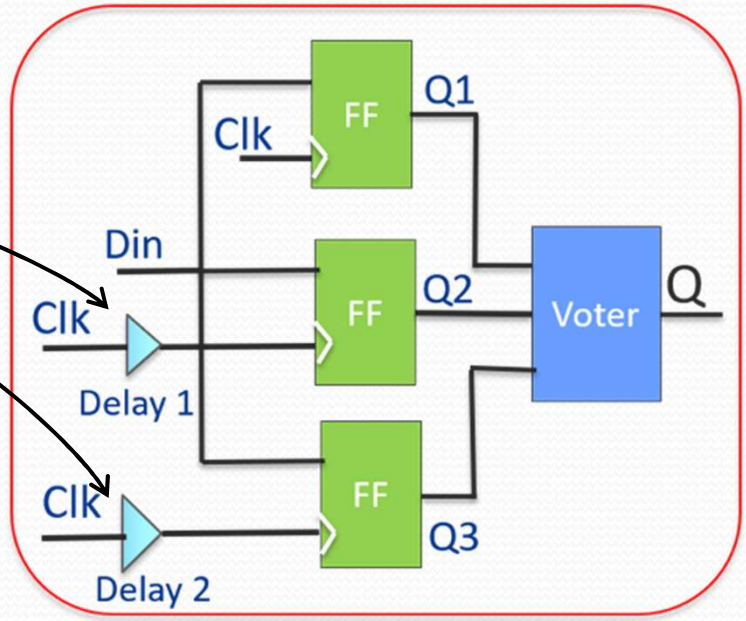
Fluence of Hadrons > 20 MeV (4000 fb-1)



SET Analysis



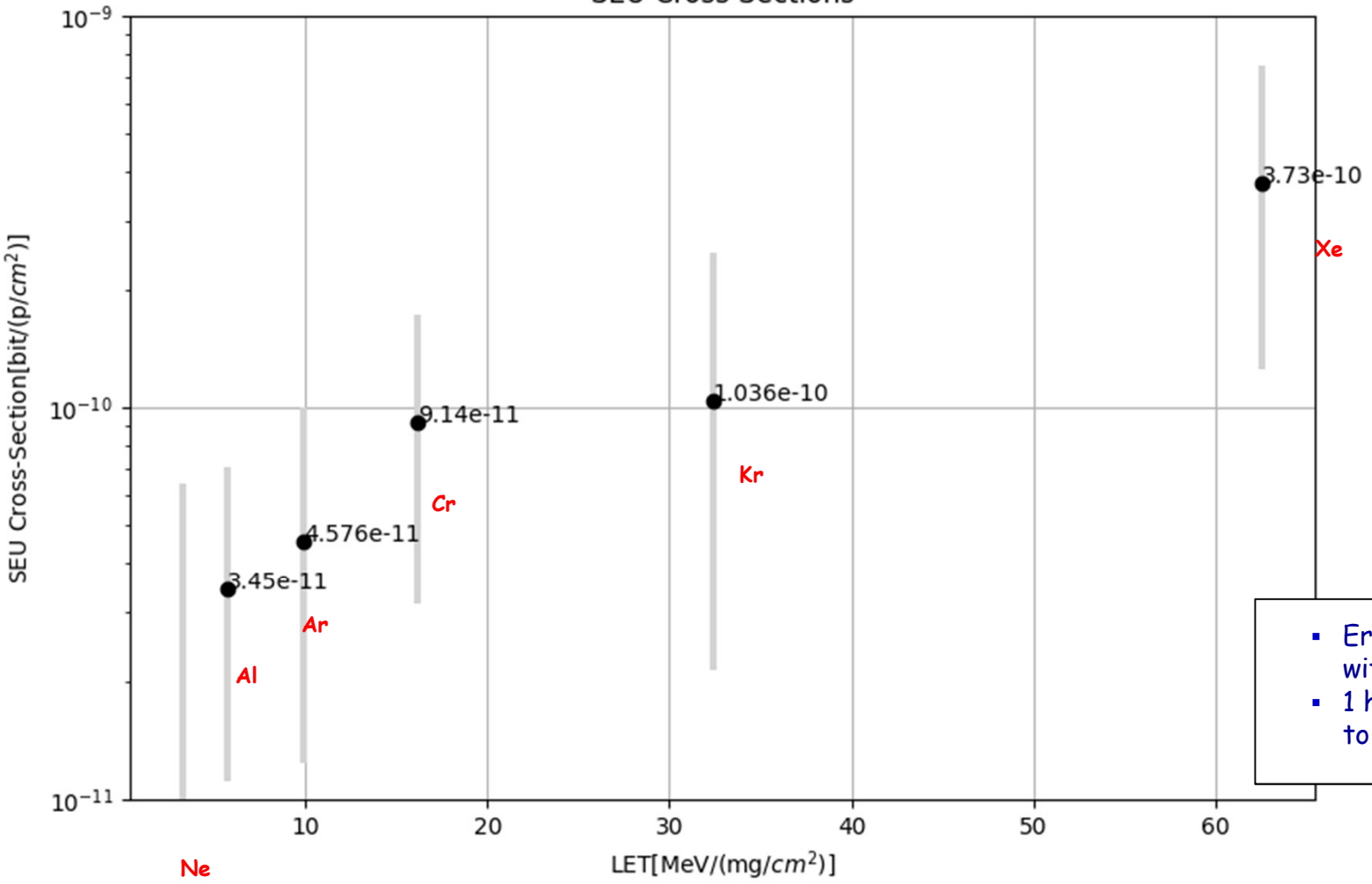
SEU tolerant design with temporal Mitigation



- SET test structures implemented in the chip
  - Measurement of pulse width > 70 ps with a resolution of 30 ps
- NOR gate: SET pulse width : **70 ps < PW < 220 ps**
- RD53B chip
  - The structure using temporal mitigation is implemented in RD53B
  - This work helped to set the optimal value for the delay

Global Register Results

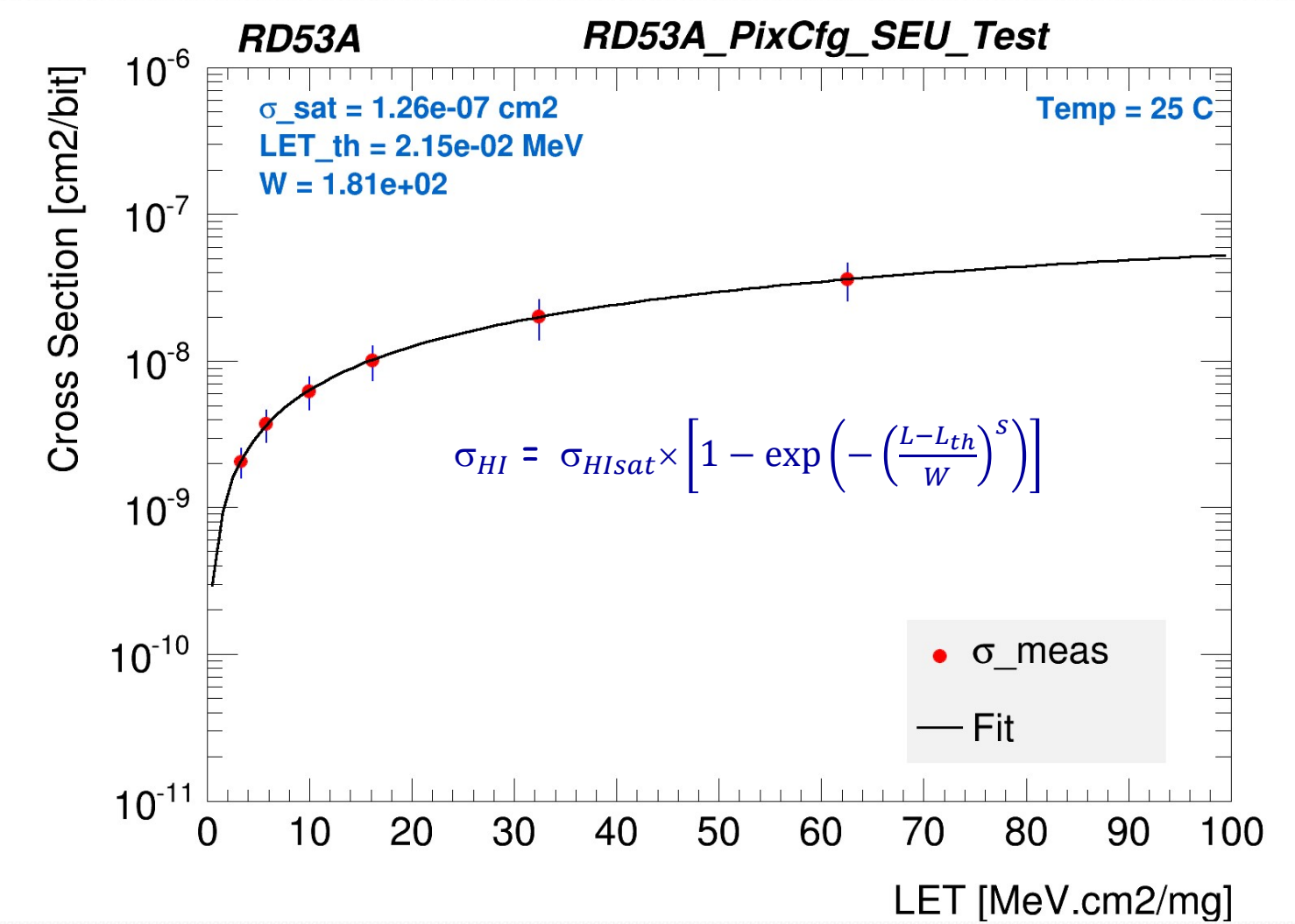
ITkPixV1: SEU Cross-Sections For Global Configuration Registers



- Error bars are estimated with 95% confidence level
- 1 hour of beam spent for Al to get 5 bit flip

- 2 order of magnitude more tolerant than the standard DFF
- The proton cross section estimated to 2-5 10^{-16} cm²
- Needs to be confirmed in proton facility

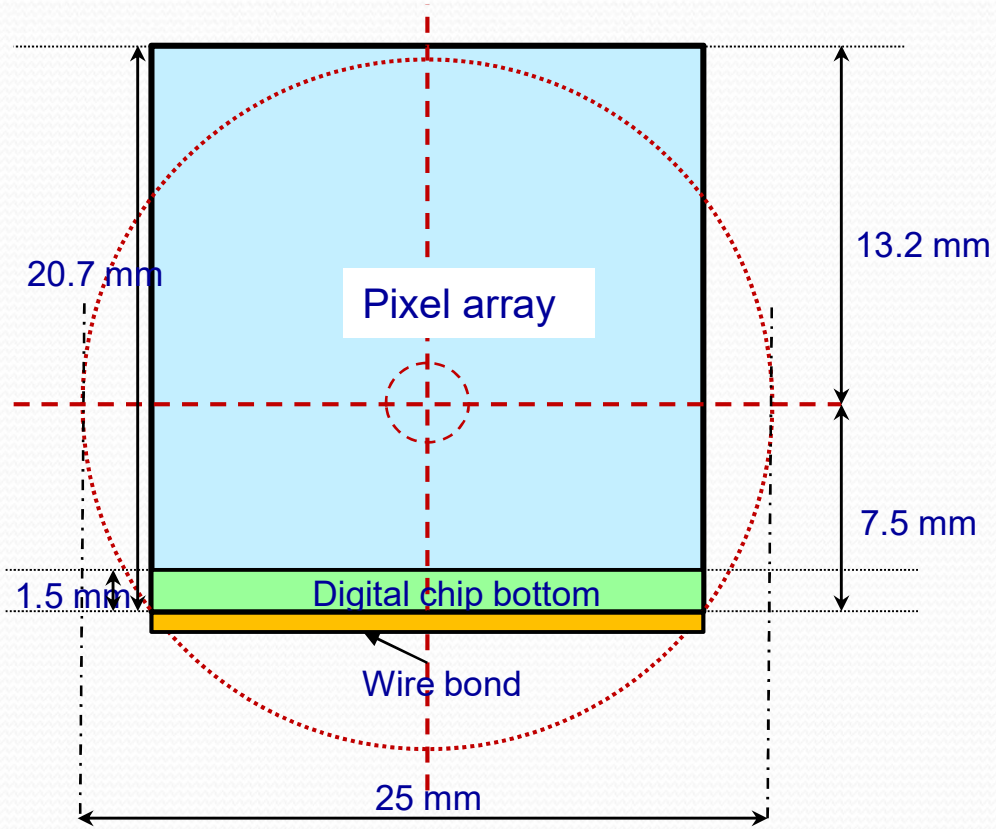
Config Register

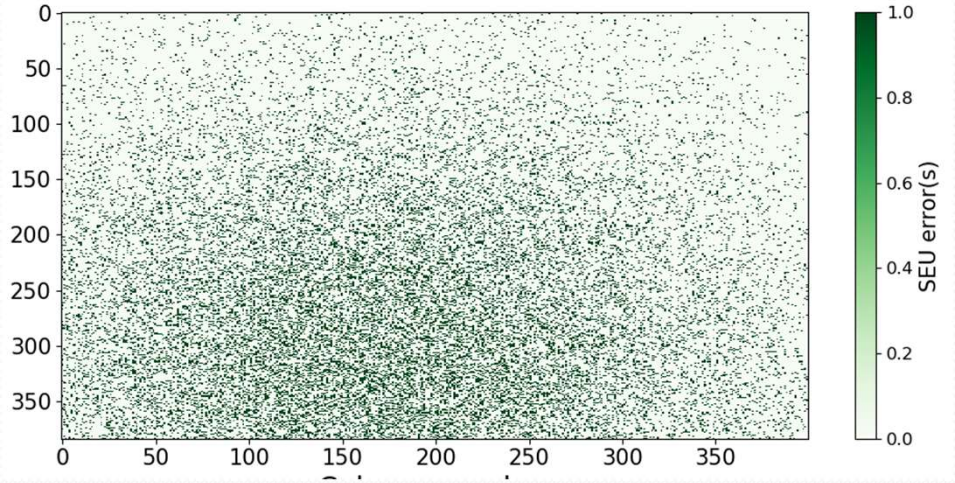


Pixel Configuration

Bits	Name	Description
[0]	Enable	Include the pixel in the DAQ data path
[1]	Cal Enable	Turn on charge injection (*)
[2]	HitOr Enable	Add the pixel to its wired OR core col. hit line
[3:6]	TDAC value	Value for in-pixel theshold trim DAC
[7]	TDAC sign	Selects differential branch set to TDAC value

Beam position





Pixel configuration SEU effects

Fluence =

- The beam diameter is 25 mm
- The entire **Digital Chip Bottom** part must be covered by the beam