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Single Event Effects Testing of the RD53B chip

Thursday, May 27, 2021 7:30 AM (18 minutes)

The RD53 collaboration has been working since 2014 on the development of pixel chips for CMS and ATLAS phase 2 upgrades. This work has recently led to the development of the RD53B full-scale readout chip which is using the 65nm CMOS process and containing 153600 pixels of 50×50 μm2.
The RD53B chip is designed to be robust against the Single Event Upset (SEU), allowing such a complex chip to operate reliably in the hostile environment of the HL-LHC. Different SEU mitigation techniques based on the Triple Modular Redundancy (TMR) have been adopted for the critical information in the RD53B chip. Furthermore, the efficiency of this mitigation scheme has been evaluated for the RD53B chip with heavy-ion beams in the CYCLONE facility and with a 480 MeV proton beam in the TRIUMF facility.
The purpose of this talk is to describe and explain all the SEU mitigation strategies used in the RD53B chip, to report and analyze the SEU test results and to estimate the expected SEU rates at the HL-LHC.

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No, this is an entirely new submission.

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